

74LV4T126FK

1. Functional Description

- Quad Bus Buffer, Non-Inverted 3-State Outputs with Level Shifting

2. General

74LV4T126 is high speed CMOS quad 3-state bus buffer gate fabricated with silicon gate CMOS technology. This product is able to allow level-up or level-down voltage translation with only one power supply.

The output level is referenced to the power supply voltage and is able to support 1.8-V, 2.5-V, 3.3-V, and 5.0-V CMOS level. The input circuit is designed with a lower threshold. So level-up translation from 1.8 V to 3.3 V or from 3.3 V to 5.0 V is possible.

All input terminals have an input protection circuit with no diode from input terminal to power supply side. All output terminals have an output circuit with no parasitic diode from output terminal to power supply side. These circuits realize an input tolerant function and output power-down protection, and ensure the voltage of input terminals up to 5.5 V without regard to the supply voltage, and the voltage of output terminals up to 5.5 V even if the output terminal is high impedance state or the power supply voltage is not applied. So level-down translation from 3.3 V to 1.8 V or from 5.0 V to 3.3 V is possible.

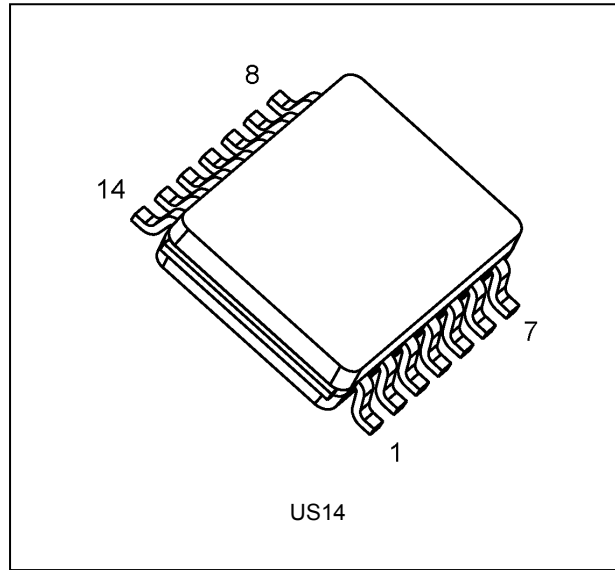
The wide power supply voltage range of 1.65 V to 5.5 V allows the generation of desired output level to connect to controllers or processors and prevents device destruction due to mismatched supply voltage and input voltage.

3. Features

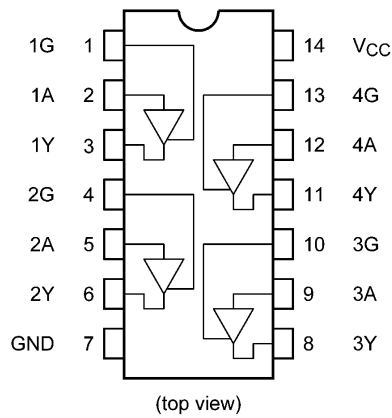
- (1) Wide operating voltage range: $V_{CC} = 1.65 \text{ V to } 5.5 \text{ V}$
- (2) Level-up voltage translation
 - 1.2 V to 1.8 V \rightarrow 1.8 V ($V_{CC} = 1.8 \text{ V}$)
 - 1.5 V to 2.5 V \rightarrow 2.5 V ($V_{CC} = 2.5 \text{ V}$)
 - 1.8 V to 3.3 V \rightarrow 3.3 V ($V_{CC} = 3.3 \text{ V}$)
 - 2.5 V to 5.0 V \rightarrow 5.0 V ($V_{CC} = 5.0 \text{ V}$)
- (3) Level-down voltage translation
 - 5.0 V to 1.8 V \rightarrow 1.8 V ($V_{CC} = 1.8 \text{ V}$)
 - 5.0 V to 2.5 V \rightarrow 2.5 V ($V_{CC} = 2.5 \text{ V}$)
 - 5.0 V to 3.3 V \rightarrow 3.3 V ($V_{CC} = 3.3 \text{ V}$)
- (4) Low power dissipation: $I_{CC} = 4.0 \mu\text{A (max)}$ at $T_a = 25 \text{ }^\circ\text{C}$
- (5) Wide operating temperature range: $T_{opr} = -40 \text{ to } 125 \text{ }^\circ\text{C}$
- (6) 5.5 V tolerant is provided on all inputs, power down protection is provided on all outputs.
- (7) Low noise: $V_{OLP} = 0.8 \text{ V (max)}$

Start of commercial production
2020-03

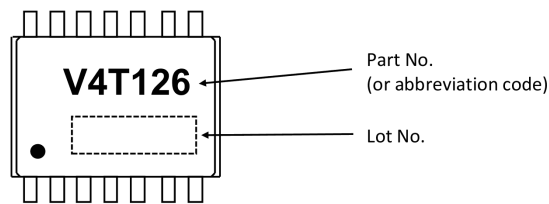
4. Packaging



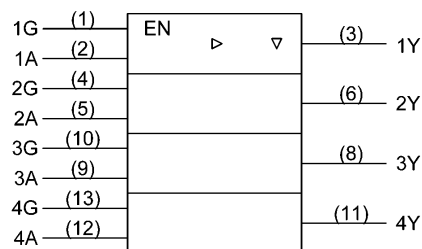
5. Pin Assignment



6. Marking



7. IEC Logic Symbol



8. Truth Table

Input G	Input A	Output Y
L	X	Z
H	L	L
H	H	H

X: Don't care

Z: High impedance

9. Absolute Maximum Ratings (Note)

Characteristics	Symbol	Note	Rating	Unit
Supply voltage	V_{CC}		-0.5 to 7.0	V
Input voltage	V_{IN}		-0.5 to 7.0	V
Output voltage	V_{OUT}	(Note 1)	-0.5 to 7.0	V
		(Note 2)	-0.5 to $V_{CC} + 0.5$	
Input diode current	I_{IK}		-20	mA
Output diode current	I_{OK}	(Note 3)	± 50	mA
Output current	I_{OUT}		± 35	mA
V_{CC} /ground current	I_{CC}		± 50	mA
Power dissipation	P_D	(Note 4)	180	mW
Storage temperature	T_{stg}		-65 to 150	$^{\circ}C$

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Output in OFF state.

Note 2: High (H) or Low (L) state. I_{OUT} absolute maximum rating must be observed.

Note 3: $V_{OUT} < GND$, $V_{OUT} > V_{CC}$

Note 4: 180 mW in the range of $T_a = -40$ to $85^{\circ}C$. From $T_a = 85$ to $125^{\circ}C$ a derating factor of -3.25 mW/ $^{\circ}C$ shall be applied until 50 mW.

10. Operating Ranges (Note)

Characteristics	Symbol	Note	Test Condition	Rating	Unit
Supply voltage	V_{CC}			1.65 to 5.5	V
Input voltage	V_{IN}			0 to 5.5	V
Output voltage	V_{OUT}	(Note 1)		0 to 5.5	V
		(Note 2)		0 to V_{CC}	
Operating temperature	T_{opr}			-40 to 125	$^{\circ}C$
Input rise and fall times	dt/dv		$V_{CC} = 1.8 \pm 0.15$ V, 2.5 ± 0.2 V	0 to 20	ns/V
			$V_{CC} = 3.3 \pm 0.3$ V	0 to 10	
			$V_{CC} = 5.0 \pm 0.5$ V	0 to 5	

Note: The operating ranges must be maintained to ensure the normal operation of the device.

Unused inputs must be tied to either V_{CC} or GND.

Note 1: Output in OFF state.

Note 2: High (H) or Low (L) state.

11. Electrical Characteristics

11.1. DC Characteristics (Unless otherwise specified, $T_a = 25\text{ }^\circ\text{C}$)

Characteristics	Symbol	Test Condition	V_{CC} (V)	Min	Typ.	Max	Unit		
High-level input voltage	V_{IH}	—	1.65 to 1.95	0.95	—	—	V		
			2.3 to 2.7	1.15	—	—			
			3.0 to 3.6	1.3	—	—			
			4.5 to 5.5	2.0	—	—			
Low-level input voltage	V_{IL}	—	1.65 to 1.95	—	—	0.4	V		
			2.3 to 2.7	—	—	0.55			
			3.0 to 3.6	—	—	0.65			
			4.5 to 5.5	—	—	0.7			
High-level output voltage	V_{OH}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -50\text{ }\mu\text{A}$	1.65 to 5.5	$V_{CC}-0.1$	—	—	V	
			$I_{OH} = -2\text{ mA}$	1.65	1.35	—	—		
			$I_{OH} = -3\text{ mA}$	2.3	2.05	—	—		
			$I_{OH} = -5\text{ mA}$	3.0	2.7	—	—		
			$I_{OH} = -8\text{ mA}$	4.5	2.6	—	—		
			$I_{OH} = -8\text{ mA}$		3.8	—	—		
			$I_{OH} = -16\text{ mA}$	5.0	3.7	—	—		
			$I_{OH} = -16\text{ mA}$		4.4	—	—		
Low-level output voltage	V_{OL}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 50\text{ }\mu\text{A}$	1.65 to 5.5	—	—	0.1	V	
			$I_{OL} = 2\text{ mA}$	1.65	—	—	0.2		
				1.8	—	—	0.2		
			$I_{OL} = 3\text{ mA}$	2.3	—	—	0.2		
				2.5	—	—	0.25		
			$I_{OL} = 5\text{ mA}$	3.0	—	—	0.35		
			$I_{OL} = 8\text{ mA}$	4.5	—	—	0.4		
			$I_{OL} = 8\text{ mA}$		3.3	—	—		0.45
			$I_{OL} = 8\text{ mA}$		4.5	—	—		0.5
			$I_{OL} = 16\text{ mA}$	5.0	—	—	0.55		
$I_{OL} = 16\text{ mA}$	5.0	—	—		0.55				
Input leakage current	I_{IN}	$V_{IN} = 0$ to 5.5 V	0 to 5.5	—	—	± 0.1	μA		
3-state output OFF-state leakage current	I_{OZ}	$V_{IN} = V_{IH}$ or V_{IL} $V_{OUT} = 0$ to 5.5 V	1.65 to 5.5	—	—	± 0.5	μA		
Power-OFF leakage current	I_{OFF}	$V_{IN} = V_{IH}$ or V_{IL} $V_{OUT} = 0$ to 5.5 V	0	—	—	1.0	μA		
Quiescent supply current	I_{CC}	$V_{IN} = V_{CC}$ or GND	1.65 to 5.5	—	—	4.0	μA		
	I_{CCT}	One input: $V_{IN} = 3.4\text{ V}$ The other inputs: V_{CC} or GND	5.5	—	—	1.35	mA		
		One input: $V_{IN} = 1.1\text{ V}$ The other inputs: V_{CC} or GND	1.8	—	—	1.35	mA		

11.2. DC Characteristics (Unless otherwise specified, $T_a = -40$ to 85 °C)

Characteristics	Symbol	Test Condition	V_{CC} (V)	Min	Max	Unit	
High-level input voltage	V_{IH}	—	1.65 to 1.95	1.0	—	V	
			2.3 to 2.7	1.2	—		
			3.0 to 3.6	1.35	—		
			4.5 to 5.5	2.0	—		
Low-level input voltage	V_{IL}	—	1.65 to 1.95	—	0.35	V	
			2.3 to 2.7	—	0.5		
			3.0 to 3.6	—	0.6		
			4.5 to 5.5	—	0.7		
High-level output voltage	V_{OH}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -50 \mu A$	1.65 to 5.5	$V_{CC}-0.1$	—	V
			$I_{OH} = -2$ mA	1.65	1.3	—	
			$I_{OH} = -3$ mA	2.3	2.0	—	
			$I_{OH} = -5$ mA	3.0	2.6	—	
			$I_{OH} = -8$ mA		2.5	—	
			$I_{OH} = -8$ mA	4.5	3.7	—	
			$I_{OH} = -16$ mA		3.6	—	
			$I_{OH} = -16$ mA	5.0	4.3	—	
Low-level output voltage	V_{OL}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 50 \mu A$	1.65 to 5.5	—	0.1	V
			$I_{OL} = 2$ mA	1.65	—	0.25	
				1.8	—	0.3	
			$I_{OL} = 3$ mA	2.3	—	0.3	
				2.5	—	0.3	
			$I_{OL} = 5$ mA	3.0	—	0.4	
			$I_{OL} = 8$ mA		—	0.45	
			$I_{OL} = 8$ mA	3.3	—	0.5	
			$I_{OL} = 8$ mA	4.5	—	0.55	
			$I_{OL} = 16$ mA		—	0.55	
$I_{OL} = 16$ mA	5.0	—	0.55				
Input leakage current	I_{IN}	$V_{IN} = 0$ to 5.5 V	0 to 5.5	—	± 2.0	μA	
3-state output OFF-state leakage current	I_{OZ}	$V_{IN} = V_{IH}$ or V_{IL} $V_{OUT} = 0$ to 5.5 V	1.65 to 5.5	—	± 5.0	μA	
Power-OFF leakage current	I_{OFF}	$V_{IN} = V_{IH}$ or V_{IL} $V_{OUT} = 0$ to 5.5 V	0	—	10.0	μA	
Quiescent supply current	I_{CC}	$V_{IN} = V_{CC}$ or GND	1.65 to 5.5	—	10.0	μA	
	I_{CCT}	One input: $V_{IN} = 3.4$ V The other inputs: V_{CC} or GND	5.5	—	1.50	mA	
		One input: $V_{IN} = 1.1$ V The other inputs: V_{CC} or GND	1.8	—	1.50	mA	

11.3. DC Characteristics (Unless otherwise specified, $T_a = -40$ to 125 °C)

Characteristics	Symbol	Test Condition	V_{CC} (V)	Min	Max	Unit	
High-level input voltage	V_{IH}	—	1.65 to 1.95	1.0	—	V	
			2.3 to 2.7	1.2	—		
			3.0 to 3.6	1.35	—		
			4.5 to 5.5	2.0	—		
Low-level input voltage	V_{IL}	—	1.65 to 1.95	—	0.35	V	
			2.3 to 2.7	—	0.5		
			3.0 to 3.6	—	0.6		
			4.5 to 5.5	—	0.7		
High-level output voltage	V_{OH}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -50 \mu A$	1.65 to 5.5	$V_{CC}-0.1$	—	V
			$I_{OH} = -2$ mA	1.65	1.3	—	
			$I_{OH} = -3$ mA	2.3	2.0	—	
			$I_{OH} = -5$ mA	3.0	2.6	—	
			$I_{OH} = -8$ mA		2.5	—	
			$I_{OH} = -8$ mA	4.5	3.7	—	
			$I_{OH} = -16$ mA		3.6	—	
			$I_{OH} = -16$ mA	5.0	4.3	—	
Low-level output voltage	V_{OL}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 50 \mu A$	1.65 to 5.5	—	0.1	V
			$I_{OL} = 2$ mA	1.65	—	0.25	
				1.8	—	0.3	
			$I_{OL} = 3$ mA	2.3	—	0.3	
				2.5	—	0.3	
			$I_{OL} = 5$ mA	3.0	—	0.4	
			$I_{OL} = 8$ mA		—	0.45	
			$I_{OL} = 8$ mA	3.3	—	0.5	
			$I_{OL} = 8$ mA	4.5	—	0.55	
				$I_{OL} = 16$ mA		—	
$I_{OL} = 16$ mA	5.0	—	0.55				
Input leakage current	I_{IN}	$V_{IN} = 0$ to 5.5 V	0 to 5.5	—	± 2.0	μA	
3-state output OFF-state leakage current	I_{OZ}	$V_{IN} = V_{IH}$ or V_{IL} $V_{OUT} = 0$ to 5.5 V	1.65 to 5.5	—	± 10.0	μA	
Power-OFF leakage current	I_{OFF}	$V_{IN} = V_{IH}$ or V_{IL} $V_{OUT} = 0$ to 5.5 V	0	—	20.0	μA	
Quiescent supply current	I_{CC}	$V_{IN} = V_{CC}$ or GND	1.65 to 5.5	—	40.0	μA	
	I_{CCT}	One input: $V_{IN} = 3.4$ V The other inputs: V_{CC} or GND	5.5	—	1.50	mA	
		One input: $V_{IN} = 1.1$ V The other inputs: V_{CC} or GND	1.8	—	1.50	mA	

11.4. AC Characteristics (Unless otherwise specified, $T_a = 25\text{ }^\circ\text{C}$, Input: $t_r = t_f = 3\text{ ns}$)

Characteristics	Symbol	Note	Test Condition	V_{CC} (V)	C_L (pF)	Min	Typ.	Max	Unit
Propagation delay time	t_{PLH}, t_{PHL}		—	1.8 ± 0.15	15	—	8.9	27.5	ns
					30	—	10.1	30.5	
				2.5 ± 0.2	15	—	5.2	10.5	ns
					30	—	5.9	11.1	
				3.3 ± 0.3	15	—	3.8	6.4	ns
					30	—	4.4	7.2	
				5.0 ± 0.5	15	—	3.1	4.1	ns
					30	—	3.4	4.7	
3-state output enable time	t_{PZL}, t_{PZH}		$R_L = 1\text{ k}\Omega$	1.8 ± 0.15	15	—	8.3	26.0	ns
					30	—	9.8	31.5	
				2.5 ± 0.2	15	—	4.4	9.3	ns
					30	—	5.3	11.5	
				3.3 ± 0.3	15	—	3.2	5.8	ns
					30	—	4.0	7.1	
				5.0 ± 0.5	15	—	2.5	3.9	ns
					30	—	3.0	4.8	
3-state output disable time	t_{PLZ}, t_{PHZ}		$R_L = 1\text{ k}\Omega$	1.8 ± 0.15	15	—	13.3	35.6	ns
					30	—	17.7	37.0	
				2.5 ± 0.2	15	—	8.0	13.7	ns
					30	—	11.1	15.8	
				3.3 ± 0.3	15	—	5.8	8.6	ns
					30	—	8.1	11.3	
				5.0 ± 0.5	15	—	4.2	6.2	ns
					30	—	4.9	7.2	
Output skew	t_{osLH}, t_{osHL}	(Note 1)	—	1.65 to 5.5	15	—	—	1.0	ns
Input capacitance	C_{IN}		—			—	4	10	pF
Output capacitance	C_{OUT}		—			—	6	—	pF
Power dissipation capacitance	C_{PD}	(Note 2)	$V_{CC} = 5.5\text{ V}$			—	14	—	pF

Note 1: Parameter guaranteed by design. ($t_{osLH} = |t_{PLHM} - t_{PLHN}|$, $t_{osHL} = |t_{PHLM} - t_{PHLN}|$)

Note 2: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation.

$$I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/4 \text{ (per gate)}$$

11.5. AC Characteristics

(Unless otherwise specified, $T_a = -40$ to 85 °C, Input: $t_r = t_f = 3$ ns)

Characteristics	Symbol	Note	Test Condition	V_{CC} (V)	C_L (pF)	Min	Max	Unit
Propagation delay time	t_{PLH}, t_{PHL}		—	1.8 ± 0.15	15	1.0	29.5	ns
					30	1.0	33.2	
				2.5 ± 0.2	15	1.0	11.2	ns
					30	1.0	12.4	
				3.3 ± 0.3	15	1.0	7.2	ns
					30	1.0	8.1	
				5.0 ± 0.5	15	1.0	4.8	ns
					30	1.0	5.6	
3-state output enable time	t_{PZL}, t_{PHZ}		$R_L = 1$ k Ω	1.8 ± 0.15	15	1.0	28.1	ns
					30	1.0	34.2	
				2.5 ± 0.2	15	1.0	10.3	ns
					30	1.0	12.7	
				3.3 ± 0.3	15	1.0	6.7	ns
					30	1.0	8.1	
				5.0 ± 0.5	15	1.0	4.7	ns
					30	1.0	5.6	
3-state output disable time	t_{PLZ}, t_{PHZ}		$R_L = 1$ k Ω	1.8 ± 0.15	15	1.0	36.9	ns
					30	1.0	38.2	
				2.5 ± 0.2	15	1.0	14.5	ns
					30	1.0	16.9	
				3.3 ± 0.3	15	1.0	9.6	ns
					30	1.0	11.8	
				5.0 ± 0.5	15	1.0	6.8	ns
					30	1.0	7.7	
Output skew	$t_{oS LH}, t_{oS HL}$	(Note 1)	—	1.65 to 5.5	15	—	1.0	ns

Note 1: Parameter guaranteed by design. ($t_{oS LH} = |t_{PLHM} - t_{PLHN}|$, $t_{oS HL} = |t_{PHLM} - t_{PHLN}|$)

11.6. AC Characteristics (Unless otherwise specified, $T_a = -40$ to 125 °C, Input: $t_r = t_f = 3$ ns)

Characteristics	Symbol	Note	Test Condition	V_{CC} (V)	C_L (pF)	Min	Max	Unit
Propagation delay time	t_{PLH}, t_{PHL}		—	1.8 ± 0.15	15	1.0	29.5	ns
					30	1.0	33.2	
				2.5 ± 0.2	15	1.0	11.7	ns
					30	1.0	13.1	
				3.3 ± 0.3	15	1.0	7.8	ns
					30	1.0	8.8	
5.0 ± 0.5	15	1.0	5.4	ns				
	30	1.0	6.2					
3-state output enable time	t_{PZL}, t_{PHZ}		$R_L = 1$ k Ω	1.8 ± 0.15	15	1.0	28.1	ns
					30	1.0	34.2	
				2.5 ± 0.2	15	1.0	10.8	ns
					30	1.0	13.4	
				3.3 ± 0.3	15	1.0	7.3	ns
					30	1.0	8.9	
5.0 ± 0.5	15	1.0	5.1	ns				
	30	1.0	6.2					
3-state output disable time	t_{PLZ}, t_{PHZ}		$R_L = 1$ k Ω	1.8 ± 0.15	15	1.0	36.9	ns
					30	1.0	38.2	
				2.5 ± 0.2	15	1.0	14.9	ns
					30	1.0	17.3	
				3.3 ± 0.3	15	1.0	10.1	ns
					30	1.0	12.0	
5.0 ± 0.5	15	1.0	7.1	ns				
	30	1.0	8.0					
Output skew	$t_{oS LH}, t_{oS HL}$	(Note 1)	—	1.65 to 5.5	15	—	1.0	ns

Note 1: Parameter guaranteed by design. ($t_{oS LH} = |t_{PLHM} - t_{PLHN}|$, $t_{oS HL} = |t_{PHLM} - t_{PHLN}|$)

11.7. Noise Characteristics (Unless otherwise specified, $T_a = 25$ °C, Input: $t_r = t_f = 3$ ns)

Characteristics	Symbol	Test Condition	V_{CC} (V)	Typ.	Limit	Unit
Quiet output maximum dynamic V_{OL}	V_{OLP}	$C_L = 50$ pF	3.3	0.5	0.8	V
Quiet output minimum dynamic V_{OL}	V_{OLV}	$C_L = 50$ pF	3.3	-0.5	-0.8	V

11.8. AC Test Circuit

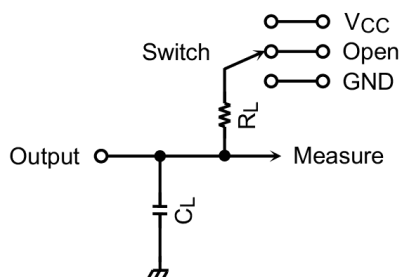


Table 11.8.1 Parameter for AC Test Circuit

Characteristics	Switch
t_{PLH} , t_{PHL}	Open
t_{PLZ} , t_{PZL}	V_{CC}
t_{PHZ} , t_{PZH}	GND

11.9. AC Waveform

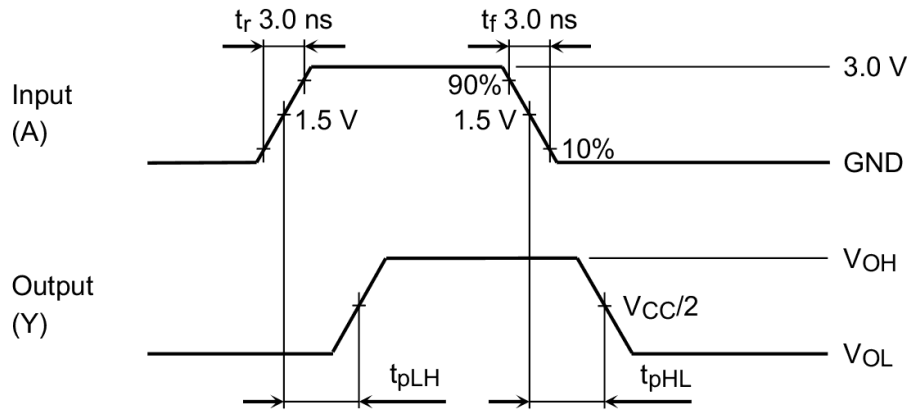


Fig. 11.9.1 t_{pLH} , t_{pHL}

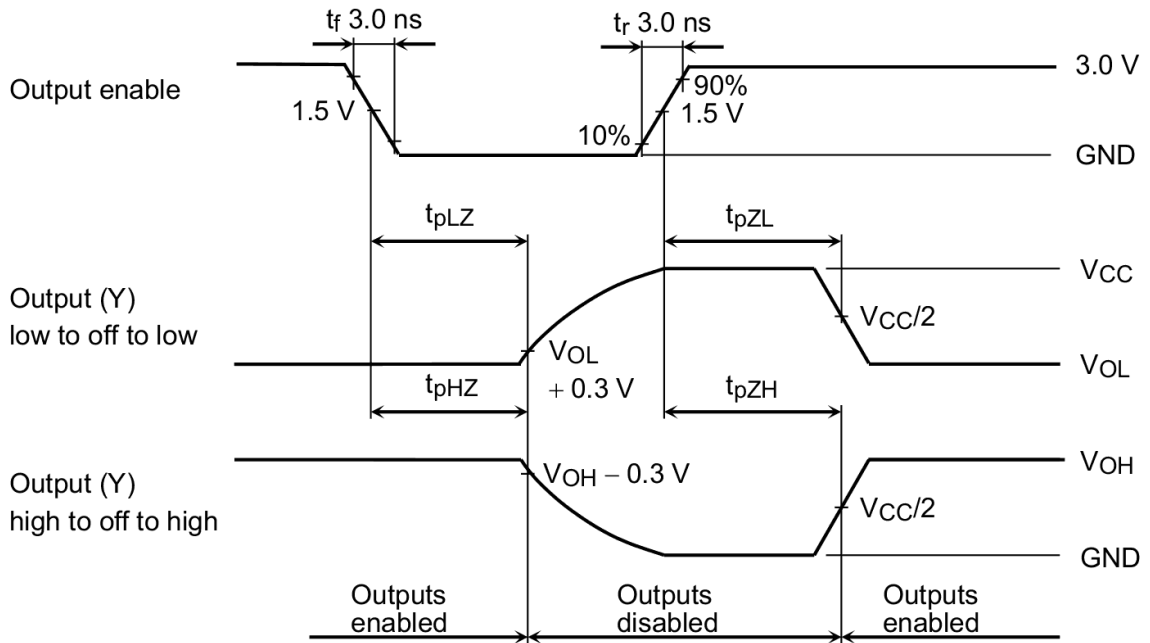


Fig. 11.9.2 t_{pLZ} , t_{pHZ} , t_{pZL} , t_{pZH}

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