Outline:

This document explains the operation, electrical characteristics (on-voltage, breakdown voltage of each pin, switching time, etc.) during switch operation, type, and selection method of the built-in resistor transistor (also known as BRT, digital transistor).
Table of Contents

Outline: .............................................................................................................................................. 1
Table of Contents ............................................................................................................................. 2
1. Introduction .................................................................................................................................. 4
2. Operation of the BRT ................................................................................................................... 6
3. Electrical characteristics as a switch ............................................................................................ 7
   3.1. Voltage across switch terminals at turn-on (V_{CE(sat)}) ...................................................... 7
   3.2. Withstand voltages ................................................................................................................ 9
      3.2.1. Maximum voltage across switch terminals at switch-off (collector-emitter withstand voltage) ....................................................................................................................... 9
      3.2.2. Control voltage (maximum and minimum emitter-base voltages, V_{EBO}) .................. 10
   3.3. Control voltages (input voltage (ON) (V_{I(ON)}) and input voltage (OFF) (V_{I(OFF)})) . . . 12
   3.4. Switching times .................................................................................................................... 13
4. Types of BRTs ................................................................................................................................ 15
5. Selection guidelines ....................................................................................................................... 16
   5.1. Matching with the control circuit at the previous stage (selection of an NPN or PNP BRT) ........................................................................................................................................... 17
   5.2. Turning on and off the BRT without fail via a control signal (V_{I(ON)} and V_{I(OFF)} voltages) . 18
   5.3. Obtaining necessary output voltage when the BRT is on ...................................................... 18
   5.4. Reducing the turn-on or turn-off time .................................................................................... 18
6. Calculating the power dissipation of a BRT .................................................................................. 19
7. Application circuit examples ......................................................................................................... 20
8. Related Links ................................................................................................................................ 21
9. RESTRICTIONS ON PRODUCT USE ....................................................................................... 22
List of Figures

Figure 1-1 Switching circuit ........................................................................................................ 4
Figure 1-2 Static characteristics of the BRT (Ic ~ VCE curves) ...................................................... 5
Figure 2-1 Circuit used for the explanation of BRT operation .......................................................... 6
Figure 2-2 VBE(sat) ~ IC curves (2SC2712) ................................................................................. 7
Figure 2-3 Operating locus of the BRT .......................................................................................... 7
Figure 3-1 Voltage across switch terminals .................................................................................. 7
Figure 3-2 Reducing the collector-emitter saturation voltage, VCE(sat) ........................................... 8
Figure 3-3 VBE(sat) ~ IC curves (2SC2712) .................................................................................. 9
Figure 3-4 VCE(sat) ~ IC curves (RN1102) .................................................................................. 9
Figure 3-5 Forward control voltage .............................................................................................. 10
Figure 3-6 Collector current (IC) vs. input voltage (VI) (left: hFE=10, right: hFE=20) ............... 11
Figure 3-7 Reverse control voltage .............................................................................................. 11
Figure 3-8 VEO vs. R1/R2 ............................................................................................................. 11
Figure 3-9 Effects of bias resistors on V(ON) .............................................................................. 12
Figure 3-10 Test circuit for and definitions of switching times .................................................... 13
Figure 3-11 Collector current ...................................................................................................... 14
Figure 4-1 2-in-1 BRTs ............................................................................................................... 15
Figure 5-1 Basic circuit ................................................................................................................. 16
Figure 5-2 Selection of electrical characteristics ........................................................................ 16
Figure 5-3 Circuit with a high-Z state preceding a BRT ................................................................. 17
Figure 5-4 BRT preceded by pull-up resistor .............................................................................. 17
Figure 5-5 Connecting NPN and PNP BRTs in parallel .............................................................. 17
Figure 6-1 Basic circuit ............................................................................................................... 19
Figure 7-1 BRT application circuit examples .............................................................................. 20
1. Introduction

Semiconductor switches come in many types, including simple on-off switches and those for the selection of a signal and electrical power. This application note discusses bias resistor built-in transistors (BRTs) used as simple on-off switches as shown in Figure 1-1. Available in a single-chip implementation, a BRT is composed of a bipolar transistor and two bias resistors for switching. In Figure 1-1(b), a BRT is enclosed in a dashed box.

On-off switches should switch on and off within a specified time at a specified control voltage, have low turn-on and high turn-off resistance, and provide sufficient ruggedness. The following shows the four characteristics required for BRTs in comparison with general-purpose 60-V MOSFETs used for similar applications.

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>BRT</th>
<th>MOSFETs</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. Voltage across switch terminals at turn-on</td>
<td>★★★★</td>
<td>★★</td>
</tr>
<tr>
<td>2. Withstand voltage across switch terminals at turn-off</td>
<td>★★★</td>
<td>★★★★</td>
</tr>
<tr>
<td>3. Control voltage</td>
<td>★★★★</td>
<td>★★</td>
</tr>
<tr>
<td>4. Switching time</td>
<td>★★</td>
<td>★★★★</td>
</tr>
</tbody>
</table>

The greater the number of ★, the better.

The advantages of MOSFETs also include ease of device selection (i.e., ease of circuit design) and zero reactive current (i.e., power-saving). However, BRTs can also be used to configure switches at low cost if you understand selection guidelines for BRTs.

In the case of an NPN BRT like the one shown in Figure 1-1(b), R1 converts the control voltage applied to the base (B) terminal into current in order to stabilize the switching operation. In the off
state, the control signal preceding the BRT might assume the high-impedance state. In that case, $R_2$ acts as a pull-down resistor, pulling the base voltage to the GND level.

Without $R_2$, the leakage current or the collector cut-off current ($I_{CBO}$) flowing from the input at turn-off might cause the BRT to malfunction because of the charge accumulated in the base region. $R_2$ helps prevent malfunction by passing leakage current to GND.

In the case of a PNP BRT, $R_2$ acts as a pull-up resistor. There is no difference in the effects of $R_1$ and $R_2$ between NPN and PNP BRTs.

The bipolar transistor in the BRT has three distinct regions of operation: saturation, active, and cut-off regions. In the active region, the collector current is basically the base current times a given current gain. It is a current-driven device since the collector current is controlled via the base current. The ratio of the collector current to the base current in the active region (called the DC current gain) is represented by $h_{FE}$, which is 70 to 700 in the case of general-purpose bipolar transistors. As the base current is increased along the load line as shown by the arrow in Figure 1-2, the collector current increases proportionally according to $h_{FE}$. When the base current is further increased, $h_{FE}$ decreases as the gaps between collector-emitter voltage curves become narrower. If the base current is increased further on the load line, the collector current will no longer increase. This region is called the saturation region. The BRT, which is used as a switch, is operated in the saturation region as well as in the cut-off region in which the bipolar transistor is off.

![Figure 1-2 Static characteristics of the BRT (I<sub>C</sub> – V<sub>CE</sub> curves)](image-url)
2. Operation of the BRT

This section describes how a BRT incorporating an NPN bipolar transistor turns on in the saturation region when the control voltage (VI) applied to the B terminal is increased from the off state.

For the sake of simplicity, let’s consider the operation of a simple circuit shown in Figure 2-1.

1. The bipolar transistor, Q, is off.

   VI is gradually increased. Since Q is initially off, the current due to VI flows only to R1 and R2. Therefore, VI is divided by R1 and R2, and Vb is applied to the base (b) of Q.

   \[ V_b = \left\{ \frac{R_2}{R_1 + R_2} \right\} \times VI \]

   **Figure 2-1 Circuit used for the explanation of BRT operation**

2. Q turns from off to on.

   When Vb reaches roughly 0.6 V, the base current (Ib) begins to flow, turning on Q, as indicated by the V_{BE(sat)} - IC curve shown in Figure 2-2. This causes the collector current, which is Ib times hFE, to flow. At this point in time, Q is still in the active region, not in the saturation region. Therefore, its hFE is 120 to 700, as is the case with the hFE of general-purpose bipolar transistors (such as the 2SC2712).

3. Q is on. (Transition from the active region to the saturation region)

   As VI increases further, V_{BE} increases. When the base voltage (Vb) of the internal bipolar transistor is higher than 0.6 V, a slight increase in Vb causes an exponential increase in the collector current (IC) as shown in the V_{BE(sat)} - IC curves of Figure 2-2.

   Therefore, once Q turns on, Vb remains almost constant without being affected by the division of VI by R1 and R2. All the excessive current (IB - IR2) flowing through R1 flows as the base current (Ib) to the bipolar transistor. When the bipolar transistor turns on, it is still in the active region where the collector current (IC) is IB \times hFE. However, since the collector-emitter voltage (V_{CE}) is equal to VCC – RL \times IC, V_{CE} decreases suddenly because of an increase in IC, causing the bipolar transistor to enter the saturation region.

   In this region, both the base-emitter and base-collector pn junctions are forward-biased. Therefore, a large number of minority carriers are accumulated in the base region.

4. Q turns from on to off.

   The voltage on VI is reduced. However, reducing VI below the voltage specified as “input voltage (OFF)” does not cause the bipolar transistor to turn off immediately. This is because the collector current continues flowing until all the minority carriers in the base region are discharged through R2 or disappear as a result of recombination with majority carriers. The time required for this operation is called the storage time, t_{stg}. Q turns off after the minority carriers disappear.
3. Electrical characteristics as a switch

The electrical characteristics of a BRT depend on the values of the internal resistors used. As mentioned in the comparison between BRTs and 60-V MOSFETs in Section 1, it is necessary to select the optimum BRTs. This section describes major electrical characteristics of BRTs and basic guidelines for BRT selection.

3.1. Voltage across switch terminals at turn-on ($V_{CE(sat)}$)

$V_{CE(sat)}$ is the collector-emitter voltage ($V_{CE}$) when the BRT turns on. It is desirable to select BRTs with low $V_{CE(sat)}$.
The resistance between the terminals of a mechanical switch becomes almost zero when it is closed. However, for a BRT, it is necessary to use it in the saturation region where the collector-emitter resistance is low (i.e., the collector-emitter voltage is low). In the active region, the collector current increases proportionally with the base current according to $h_{FE}$. In contrast, in the saturation region, $h_{FE}$ decreases as the saturation level increases (i.e., $V_{CE}$ decreases). Figure 3-2 shows the $I_C$–$V_{CE}$ curves of a BRT, in which a load line at a $V_{CC}$ of 5 V is highlighted in red. The load line intersects the $I_B = 0.2$ mA curve at a $V_{CE}$ of 3.8 V, which means $h_{FE} = 160$ when $I_B = 0.2$ mA. However, the load line intersects the $I_B = 6$ mA curve at a $V_{CE}$ of 0.2 V, meaning $h_{FE} = 20$. Therefore, there are two ways to reduce the collector-emitter voltage ($V_{CE}$):

1. **Reducing the collector current (Increasing the load resistance, $R_L$).**
   (Red load line ⇒ blue load line)
2. **Increasing the base current $I_B$.**

Since the first way of reducing $V_{CE(sat)}$ by increasing $R_L$ affects the load current ($I_C$), the collector current can only be reduced to the extent permitted by the design requirements. Here, let’s see how increasing the base current helps reduce $V_{CE(sat)}$. Look at the circuit shown in Figure 3-1(b). The assumption is that we are changing the control voltage ($V_I$) for the RN1102 BRT (with $R_1=R_2=10$ kΩ) from 0 V to 5 V.
Without the bipolar transistor, increasing $V_I$ from 0 V to 5 V would obviously cause the voltage at $b$ ($V_b$) to change from 0 V to 2.5 V because of the ratio of the $R_1$ and $R_2$ values. In reality, however, $V_{BE}$ increases only up to roughly 1 V as shown in Figure 3-3 because of the presence of the bipolar transistor. The remaining current flows to the base terminal as $I_b$:

$$I_b = I_B - I_{R2} = (V_I - V_{BE}) / R_1 - V_{BE} / R_2$$

As indicated by this equation, $I_b$ can be increased by increasing $I_B$ and reducing $I_{R2}$ using a BRT with:

- Small $R_1$ value
- Large $R_2$ value

What is important here are the absolute values of $R_1$ and $R_2$, not the ratio of $R_1$ to $R_2$.

The collector-emitter saturation voltage increases as temperature increases, as shown in Figure 3-4. Take the above characteristics into consideration to achieve the optimum design.

3.2. Withstand voltages

The withstand voltages that should be considered are the maximum voltage applied across the switch terminals at switch-off as well as the maximum and minimum control voltages.

3.2.1. Maximum voltage across switch terminals at switch-off (collector-emitter withstand voltage)

This is defined as the collector-emitter voltage ($V_{CEO}$) with the base ($B$) open. Toshiba’s BRTs incorporate a general-purpose bipolar transistor similar to the 2SC2712 and 2SA1162 with a collector-emitter voltage of 50 V.
3.2.2. Control voltage (maximum and minimum emitter-base voltages, \( V_{EBO} \))

**Forward direction:**

As the control voltage increases, the BRT transitions from the off state to the on state.

In the case of a general bipolar transistor without resistance, as the control voltage is increased after turn-on, its collector current or collector power dissipation reaches the maximum rated value if it is in the active region, making it impossible to increase the control voltage any further. If the bipolar transistor is in the saturation region, its operation is often constrained by the rated base or collector current.

Since BRTs are usually operated in the saturation region, care should be exercised as to the base and collector currents. The allowable power dissipation of the bias resistors of a BRT is specified as 1/8 W. Accordingly, the maximum control voltage \( (V_I) \) is basically determined as described below:

1. When \( R_1 \) is large: Power dissipation of \( R_1 \)
2. When \( R_1 \) is small: Maximum collector current \( (I_C) \)

1. Power dissipation of \( R_1 \)

Let the base-emitter voltage of the internal bipolar transistor at turn-on be \( V_{be} \).

Then, the current flowing through \( R_1 \) \((I_B)\) is expressed as follows. For the sake of simplicity, the assumption is \( V_{be} = 0.7 \) V.

\[
I_B = \frac{(V_I - V_{be})}{R_1} = \frac{(V_I - 0.7)}{R_1}
\]

The power dissipation of \( R_1 \) due to \( I_B \) must not exceed 1/8 W. Hence:

\[
1/8 \text{ W} > R_1 \cdot \left(\frac{(V_I - 0.7)}{R_1}\right)^2
\]

\[
V_I < \left(\frac{R_1}{8}\right)^{1/2} + 0.7 \quad (1)
\]

2. Maximum collector current \( (I_C) \)

The current flowing to the base \((b)\) of the internal bipolar transistor \((I_B)\) can be calculated by subtracting the current flowing to \( R_2 \) \((I_{R2})\) from \( I_B \):

\[
I_b = I_B - I_{R2} = \frac{(V_I - V_{be})}{R_1} - \frac{V_{be}}{R_2} = \frac{(V_I - 0.7)}{R_1} - 0.7 \cdot \frac{1}{R_2}
\]

Since the collector current \((I_C)\) is equal to \( I_b \) times \( h_{FE} \) under operating conditions, the following equation must be satisfied:

\[
I_C(\text{max}) > I_C = h_{FE} \cdot I_b = h_{FE} \cdot \left(\frac{(V_I - 0.7)}{R_1} - 0.7 \cdot \frac{1}{R_2}\right)
\]

\[
V_I < R_1 \cdot I_C(\text{max}) \cdot h_{FE} + \left(\frac{R_1}{R_2}\right) \cdot 0.7 \cdot \frac{1}{R_2} \quad (2)
\]

The lower of the \( V_I \) values calculated based on the following two factors is the maximum allowable \( V_I \) value.

Figure 3-6 indicates the tendency of the maximum \( V_I \) value, although it should be considered merely as a guide. Basically, \( V_I \) is determined by the allowable power dissipation of bias resistor \( R_1 \) (1/8 W). However, the maximum \( V_I \) value depends on the rated collector current \((I_C)\) when \( R_1 \) is small and \( h_{FE} \) is relatively large.
Reverse direction:
Let’s consider the emitter-base voltage of the internal bipolar transistor (which is equivalent to the general-purpose bipolar transistors of the 2SC2712/2SA1162 class). The emitter is the positive side of the transistor. In the case of bipolar transistors without bias resistors, the emitter-base voltage is represented by $V_{EBO}$. In the case of BRTs, the internal bipolar transistor is off when the emitter-base voltage is applied. Therefore, the emitter-base voltage is determined by $R_2 / (R_1 + R_2)$. And therefore, BRTs with a higher resistor ratio ($R_1/R_2$) provide higher $V_{EBO}$ as shown in Figure 3-6.

The reverse voltage is the overshoot / undershoot (negative voltage) that occurs when the control input voltage $V_I$ reverses, and the voltage at the emitter terminal may become higher than the voltage at the base terminal. Care should be exercised to prevent such a situation.

**Figure 3-6** Collector current ($I_C$) vs. input voltage ($V_I$) (left: $h_{FE}=10$, right: $h_{FE}=20$)

**Figure 3-7** Reverse control voltage

**Figure 3-8** $V_{EBO}$ vs. $R_1/R_2$
3.3. Control voltages (input voltage (ON) \(V_{I(ON)}\) and input voltage (OFF) \(V_{I(OFF)}\))

In the case of a bipolar transistor, the base current begins to flow at the threshold voltage \(V_b\) of roughly 0.6 V, causing the transistor to switch on or off. When a switch circuit is configured using a BRT as shown in Figure 3-1, the input voltage \(V_I\) at which Q begins to turn on is inversely proportional to \(R_2\) and proportional to \(R_1\), as indicated by the following equations:

\[
V_{be} = \frac{R_2}{R_1+R_2} \cdot V_I \\
V_I = \frac{(R_1+R_2) \cdot V_{be}}{R_2} = \frac{(R_1/R_2 + 1) \cdot V_{be}}{R_2}
\]

The input voltage (ON) and input voltage (OFF) of a BRT are defined as follows: (\(T_a=25^\circ C\))

- Input voltage (ON), \(V_{IN(ON)}\): Voltage required to obtain the collector current equal to or higher than the prescribed value (e.g., \(I_C = 5\ mA\)) at \(V_{CE} = 0.2\ V\)
- Input voltage (OFF), \(V_{IN(OFF)}\): Voltage required to keep the collector current equal to or lower than the prescribed value (e.g., \(I_C = 0.1\ mA\)) at \(V_{CE} = 5\ V\)

Since BRTs are used in the saturation region as described above, minority carriers accumulate in the base region after the internal bipolar transistor turns on before they enter the saturation region. BRTs do not switch off until the accumulated minority carriers are swept out of the base region.

The current to charge and discharge the base is constrained by \(R_1\) at turn-on. \(R_1\) and \(R_2\) have different effects on even BRTs with the same resistor ratio \((R_1/R_2)\). Figure 3-9 plots the maximum \(V_{I(ON)}\) values shown in datasheets.

![Figure 3-9 Effects of bias resistors on \(V_{I(ON)}\)](image-url)
### 3.4. Switching times

The switching times of the bipolar transistor are defined as shown in Figure 3-10.

**Turn-on time = delay time \( t_d \) + rise time \( t_r \)**

**Turn-off time = storage time \( t_{stg} \) + fall time \( t_f \)**

In the case of bipolar transistors, the accumulation of charge \( Q_B \) in the base region begins immediately upon turn-on. BRTs, which are operated in the saturation region, continue accumulating excessive charge even after they turn on. Charge accumulation lasts until \( (\tau_n * I_B) \), a value that is determined by the lifetime \( (\tau_n) \) and base current \( (I_B) \) of the internal bipolar transistor.

At turn-off, BRTs remain on for a period of \( t_{stg} \) until the excessive charge accumulated after turn-on is swept out of the base region. Thereafter, \( I_B \) decreases exponentially.

Table 1 shows examples of the results of measurements of these BRT characteristics. The measurements were taken at a \( V_{CC} \) of 5 V, switching the input voltage from 0 V to 5 V and vice versa. The load resistance \( (R_L) \) is 1 k\( \Omega \). As indicated in Table 3-1, \( t_{stg} \) constitutes a dominant portion of the switching time.

**Table 3-1 Examples of the results of measurements of BRT switching times**

<table>
<thead>
<tr>
<th>Type</th>
<th>( R_1 ) (k( \Omega ))</th>
<th>( R_2 ) (k( \Omega ))</th>
<th>( t_r ) (ns)</th>
<th>( t_{stg} ) (( \mu )s)</th>
<th>( t_f ) (( \mu )s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>RN1401</td>
<td>4.7</td>
<td>4.7</td>
<td>38</td>
<td>1.89</td>
<td>0.11</td>
</tr>
<tr>
<td>RN1402</td>
<td>10</td>
<td>10</td>
<td>60</td>
<td>2.25</td>
<td>0.13</td>
</tr>
<tr>
<td>RN1403</td>
<td>22</td>
<td>22</td>
<td>118</td>
<td>2.41</td>
<td>0.21</td>
</tr>
</tbody>
</table>

There are two considerations for reducing \( t_{stg} \):

1. Minimize the accumulation of excess carriers.

This helps reduce the saturation depth of the BRT while it is on. Shallow saturation means high \( h_{FE} \). As can be seen from Figure 3-11, the collector current of a BRT depends mainly on supply voltage \( (V_{CC}) \) and load resistance \( (R_L) \). \( V_{CE(sat)} \) contributes less to the collector current. Therefore, even if \( I_B \) is decreased and \( h_{FE} \) is increased, the effect on the output voltage can often be ignored.

When priority is given to switching time, it is advantageous to select a BRT with a large \( R_1 \).

**Table 3-2 Effects of \( R_1 \) on \( t_{stg} \)**

<table>
<thead>
<tr>
<th>( t_{stg} ) (( \mu )s)</th>
<th>( R_1 ) (k( \Omega ))</th>
<th>( R_2 ) (k( \Omega ))</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.84</td>
<td>47</td>
<td>47</td>
</tr>
<tr>
<td>2.81</td>
<td>22</td>
<td>47</td>
</tr>
<tr>
<td>3.36</td>
<td>10</td>
<td>47</td>
</tr>
</tbody>
</table>
2. Remove excess carriers quickly.

Excess carriers accumulated in the base region are removed mainly through $R_2$ although the carrier removal path slightly differs depending on the configuration of the preceding circuit. ($R_1$ has a great influence on the saturation depth as described in 1. When $R_1$ is large, there are few excess carriers, which is advantageous for the emission time.). Therefore, BRTs with a low $R_2$ value are suitable for increasing the switching speed.

<table>
<thead>
<tr>
<th>$t_{stg}$ (μs)</th>
<th>$R_1$ (kΩ)</th>
<th>$R_2$ (kΩ)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.34</td>
<td>47</td>
<td>22</td>
</tr>
<tr>
<td>1.84</td>
<td>47</td>
<td>47</td>
</tr>
<tr>
<td>2.25</td>
<td>10</td>
<td>10</td>
</tr>
<tr>
<td>3.36</td>
<td>10</td>
<td>47</td>
</tr>
</tbody>
</table>

$IC = (V_{CC} - V_{CE(sat)}) / RL$

$V_{CE(sat)}$ is negligibly smaller than $V_{CC}$ and does not affect $IC$. 

Figure 3-11 Collector current
4. Types of BRTs

Table 4-1 shows the lineup of single BRTs. Toshiba offers BRTs with many resistor combinations so that you can find one that satisfies your electrical characteristics requirements.

Toshiba also offers 2-in-1 BRTs shown in Figure 4-1.

Table 4-1 Lineup of single BRTs

<table>
<thead>
<tr>
<th>Package dimensions (unit: mm)</th>
<th>S-Mini (SOT-346)</th>
<th>USM (SOT-623)</th>
<th>LSM (SOT-146)</th>
<th>VCH (SOT-223)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>R1 (typ) (kΩ)</td>
<td>R2 (typ) (kΩ)</td>
<td>NPN</td>
<td>PNP</td>
</tr>
<tr>
<td>50 100</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>50 800</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

The 2-in-1 BRTs are available in five-pin common-emitter, six-pin point-symmetrical, and parallel configurations.

Most 2-in-1 BRTs consist of an NPN or PNP pair, and parallel 2-in-1 BRTs also have the NPN/PNP configuration.
5. Selection guidelines

In most cases, BRTs are used as switches. Therefore, let’s assume the use of BRTs as switches. Considerations for BRTs include the following:

1. Compatibility with the control circuit at the previous stage (selection of an NPN or PNP BRT)
2. Turning on and off the transistor without fail via a control signal ($V_{i(ON)}$ and $V_{i(OFF)}$ voltages)
3. Obtaining necessary voltage when the transistor is on (i.e., reducing a drop in the collector-emitter voltage in the “on” state)
4. Reducing the turn-on or turn-off time (i.e., increasing the switching speed)

These considerations are explained below using the basic circuit with an NPN BRT shown in Figure 5-1 (which is the same as the one shown in Figure 2-1). The BRT is enclosed in the dashed box. $V_i$ is the control signal, $V_{CC}$ is the supply voltage, and $R_L$ is the load, including a pull-up resistor.

Each guideline for the selection of BRTs is discussed in the following subsections. Figure 5-2 shows the concepts of the electrical characteristics of BRTs.
5.1. Matching with the control circuit at the previous stage (selection of an NPN or PNP BRT)

Select either an NPN or PNP BRT according to the preceding control circuit. BRTs are often preceded by a circuit that can assume a high-Z state as shown in Figure 5-3. Use an NPN BRT if the output of the preceding circuit has a pull-down resistor. Use a PNP BRT if it has a pull-up resistor. Using the wrong type of BRT might, as shown in Figure 5-4, cause a BRT to malfunction at the midpoint potential between the pull-up resistor and the built-in bias resistors when the output of the preceding circuit is in the high-Z state.

Do not connect multiple NPN and PNP BRTs in parallel as shown in Figure 5-5 because the midpoint potential generated by each built-in bias resistor causes a malfunction.

Figure 5-3 Circuit with a high-Z state preceding a BRT

Figure 5-4 BRT preceded by pull-up resistor

\[ V_I = \frac{R_{n1} + R_{n2}}{R_{p1} + R_{p2} + R_{n1} + R_{n2}} \]

Figure 5-5 Connecting NPN and PNP BRTs in parallel
5.2. Turning on and off the BRT without fail via a control signal \( (V_{I(ON)} \text{ and } V_{I(OFF)}) \) voltages

Input voltage (ON) \( (V_{I(ON)}) \) and input voltage (OFF) \( (V_{I(OFF)}) \) are specified at 25°C in the datasheet. When designing a circuit, it is necessary to select BRTs that provide high-level \( V_I \) voltage of the control circuit at the previous stage higher than the maximum \( V_{I(ON)} \) voltage and low-level \( V_I \) voltage lower than the minimum \( V_{I(OFF)} \) voltage. Allow sufficient design margins according to the usage environment.

See Section 3.3, “Control voltages,” for collector current \( (I_C) \) vs. input voltage \( (V_I) \) curves.

- BRTs with higher \( R_1/R_2 \) provide higher \( V_{I(ON)} \).
- BRTs with higher \( R_1 \) provide higher \( V_{I(ON)} \) if they have equal \( R_1/R_2 \).

5.3. Obtaining necessary output voltage when the BRT is on

(Reducing a drop in the collector-emitter voltage in the “on” state)

For example, when the NPN BJT turns on in the saturation region, the collector voltage drops to the GND level because of an external resistor \( (R_L) \) and the collector current \( (I_C) \). In practice, however, there is a voltage level called collector-emitter saturation voltage \( (V_{CE(sat)}) \) between the collector and GND (emitter) potentials. \( V_{CE(sat)} \) can be reduced to some extent by increasing the base current \( (I_B) \).

\[ I_B = I_B - I_{R2} = (V_I - V_{be}) / R_1 - V_{be} / R_2 \]

- Small \( R_1 \) value
- Large \( R_2 \) value

Such BRTs pass a greater current to the base at a given input voltage \( (V_I) \). For details on the input voltage, see Section 3.1, “Voltage across switch terminals at turn-on \( (V_{CE(sat)}) \).”

5.4. Reducing the turn-on or turn-off time

(Increasing the switching speed)

Storage time \( (t_{stg}) \) constitutes a dominant portion of the switching time because of the charge accumulated in the base region. Therefore, switching speed can be reduced by reducing the amount of charge accumulated in the base region and increasing the speed at which it is discharged. Select BRTs, taking the following points into consideration. For details, see Section 3.4, “Switching times.” This requirement contradicts the description in Section 5.3.

- Do not bring a BRT into a deeper saturation level than is necessary.
  \( \Rightarrow \) Large \( R_1 \) value
- Reduce the impedance of the path through which excess carriers are removed.
  \( \Rightarrow \) Small \( R_2 \) value

Select a BRT with a small \( R_2 \) value because excess carriers are removed mainly through \( R_2 \). Excess carriers also disappear as a result of carrier recombination in the base region. There is a limit to a reduction in \( t_{stg} \) through carrier discharging.
6. Calculating the power dissipation of a BRT

For example, in amplifiers, bipolar transistors are used at high \( h_{FE} \), causing the collector power dissipation \( (V_{CE} \times I_C) \) to be dominant. In contrast, BRTs are commonly used at an \( h_{FE} \) of 10 to 20. Therefore, other sources of power dissipation cannot be ignored. It is necessary to consider the sum of the power dissipation of the internal bipolar transistor (Q) and bias resistors (R1 and R2) of a BRT.

The following shows a simple calculation example. Notice that bias resistor \( R_1 \) causes the greatest power dissipation.

Suppose that the BRT is the RN1402 \( (R_1=R_2=10 \, k\Omega) \), the input voltage \( (V_I) \) is 10 V, the collector-emitter voltage \( (V_{CE}) \) is 0.2 V, the base-emitter voltage \( (V_{be}) \) is 0.7 V, and the operating current gain \( (h_{FE}) \) of the internal bipolar transistor is 10.

The BRT is enclosed by a dashed box in Figure 6-1. Let’s calculate the amounts of currents indicated in the dashed box.

\[
\begin{align*}
I_B &= (V_I - V_{be}) / R_1 = (10 \, V - 0.7 \, V) / 10 \, k\Omega = 0.93 \, mA \\
I_{R2} &= V_{be} / R_2 = 0.7 \, V / 10 \, k\Omega = 0.07 \, mA \\
I_b &= I_B - I_{R2} = 0.93 \, mA - 0.07 \, mA = 0.86 \, mA \\
I_C &= I_b \times h_{FE} = 0.86 \, mA \times 10 = 8.60 \, mA
\end{align*}
\]

Let the power dissipation of \( R_1 \) and \( R_2 \) be \( P_{R1} \) and \( P_{R2} \) respectively and the collector-emitter and base-emitter power dissipation of the bipolar transistor be \( P_{CE} \) and \( P_{be} \) respectively.

\[
\begin{align*}
R_1 : P_{R1} &= (V_I - V_{be}) \times I_{R1} = (10 \, V - 0.7 \, V) \times 0.93 \, mA = 8.65 \, mW \\
R_2 : P_{R2} &= V_{be} \times I_{R2} = 0.7 \, V \times 0.07 \, mA = 0.05 \, mW \\
V_{CE} : P_{CE} &= V_{CE} \times I_C = 0.2 \, V \times 8.6 \, mA = 1.72 \, mW \\
V_{be} : P_{be} &= V_{be} \times I_b = 0.7 \, V \times 0.86 \, mA = 0.60 \, mW
\end{align*}
\]

Hence, the power dissipation \( (P) \) of the BRT is calculated as:

\[
P = P_{R1} + P_{R2} + P_{CE} + P_{be} = 11.02 \, mW
\]

![Figure 6-1 Basic circuit](image)
7. Application circuit examples

(a) Inverter circuit

(b) Load switch

(c) LED driver circuit

(d) Relay driver circuit
   (Plunger control circuit)

Figure 7-1 BRT application circuit examples

For the lineup of BRTs → [Click Here]
8. Related Links

- Product Line Ups (Catalog)  
  [Click]

- Product Line Ups (Parametric Search)  
  [Click]

- Stock Check & Purchase  

- FAQ of Logic ICs  
  [Click]

- Application Note  
  [Click]
9. RESTRICTIONS ON PRODUCT USE

Toshiba Corporation and its subsidiaries and affiliates are collectively referred to as "TOSHIBA". Hardware, software and systems described in this document are collectively referred to as "Product".

- TOSHIBA reserves the right to make changes to the information in this document and related Product without notice.
- This document and any information herein may not be reproduced without prior written permission from TOSHIBA. Even with TOSHIBA's written permission, reproduction is permissible only if reproduction is without alteration/omission.

- Though TOSHIBA works continually to improve Product's quality and reliability, Product can malfunction or fail. Customers are responsible for complying with safety standards and for providing adequate designs and safeguards for their hardware, software and systems which minimize risk and avoid situations in which a malfunction or failure of Product could cause loss of human life, bodily injury or damage to property, including data loss or corruption. Before customers use the Product, create designs including the Product, or incorporate the Product into their own applications, customers must also refer to and comply with (a) the latest versions of all relevant TOSHIBA information, including without limitation, this document, the specifications, the data sheets and application notes for Product and the precautions and conditions set forth in the "TOSHIBA Semiconductor Reliability Handbook" and (b) the instructions for the application with which the Product will be used with or for. Customers are solely responsible for all aspects of their own product design or applications, including but not limited to (a) determining the appropriateness of the use of this Product in such design or applications; (b) evaluating and determining the applicability of any information contained in this document, or in charts, diagrams, programs, algorithms, sample application circuits, or any other referenced documents; and (c) validating all operating parameters for such designs and applications. TOSHIBA ASSUMES NO LIABILITY FOR CUSTOMERS' PRODUCT DESIGN OR APPLICATIONS.

- PRODUCT IS NEITHER INTENDED NOR WARRANTED FOR USE IN EQUIPMENTS OR SYSTEMS THAT REQUIRE EXTRAORDINARILY HIGH LEVELS OF QUALITY AND/OR RELIABILITY, AND/OR A MALFUNCTION OR FAILURE OF WHICH MAY CAUSE LOSS OF HUMAN LIFE, BODILY INJURY, SERIOUS PROPERTY DAMAGE AND/OR SERIOUS PUBLIC IMPACT ("UNINTENDED USE"). Except for specific applications as expressly stated in this document, Unintended Use includes, without limitation, equipment used in nuclear facilities, equipment used in the aerospace industry, lifesaving and/or life supporting medical equipment, equipment used for automobiles, trains, ships and other transportation, traffic signaling equipment, equipment used to control combustions or explosions, safety devices, elevators and escalators, and devices related to power plant. IF YOU USE PRODUCT FOR UNINTENDED USE, TOSHIBA ASSUMES NO LIABILITY FOR PRODUCT. For details, please contact your TOSHIBA sales representative or contact us via our website.

- Do not disassemble, analyze, reverse-engineer, alter, modify, translate or copy Product, whether in whole or in part.
- Product shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable laws or regulations.
- The information contained herein is presented only as guidance for Product use. No responsibility is assumed by TOSHIBA for any infringement of patents or any other intellectual property rights of third parties that may result from the use of Product. No license to any intellectual property right is granted by this document, whether express or implied, by estoppel or otherwise.

- ABSENT A WRITTEN SIGNED AGREEMENT, EXCEPT AS PROVIDED IN THE RELEVANT TERMS AND CONDITIONS OF SALE FOR PRODUCT, AND TO THE MAXIMUM EXTENT ALLOWABLE BY LAW, TOSHIBA (1) ASSUMES NO LIABILITY WHATSOEVER, INCLUDING WITHOUT LIMITATION, INDIRECT, CONSEQUENTIAL, SPECIAL, OR INCIDENTAL DAMAGES OR LOSS, INCLUDING WITHOUT LIMITATION, LOSS OF PROFITS, LOSS OF OPPORTUNITIES, BUSINESS INTERRUPTION AND LOSS OF DATA, AND (2) DISCLAIMS ANY AND ALL EXPRESS OR IMPLIED WARRANTIES AND CONDITIONS RELATED TO SALE, USE OF PRODUCT, OR INFORMATION, INCLUDING WARRANTIES OR CONDITIONS OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, ACCURACY OF INFORMATION, OR NONINFRINGEMENT.

- Do not use or otherwise make available Product or related software or technology for any military purposes, including without limitation, for the design, development, use, stockpiling or manufacturing of nuclear, chemical, or biological weapons or missile technology products (mass destruction weapons). Product and related software and technology may be controlled under the applicable export laws and regulations including, without limitation, the Japanese Foreign Exchange and Foreign Trade Law and the U.S. Export Administration Regulations. Export and re-export of Product or related software or technology are strictly prohibited except in compliance with all applicable export laws and regulations.

- Please contact your TOSHIBA sales representative for details as to environmental matters such as the RoHS compatibility of Product. Please use Product in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. TOSHIBA ASSUMES NO LIABILITY FOR DAMAGES OR LOSSES OCCURRING AS A RESULT OF NONCOMPLIANCE WITH APPLICABLE LAWS AND REGULATIONS.