# **Basics of Bias Resistor Built-in Transistors (BRTs)**

# <span id="page-0-0"></span>**Outline:**

This document explains the operation, electrical characteristics (on-voltage, breakdown voltage of each pin, switching time, etc.) during switch operation, type, and selection method of the built-in resistor transistor (also known as BRT, digital transistor).

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# <span id="page-3-0"></span>**1. Introduction**

Semiconductor switches come in many types, including simple on-off switches and those for the selection of a signal and electrical power. This application note discusses bias resistor built-in transistors (BRTs) used as simple on-off switches as shown in Figure 1-1. Available in a single-chip implementation, a BRT is composed of a bipolar transistor and two bias resistors for switching. In Figure 1-1(b), a BRT is enclosed in a dashed box.

On-off switches should switch on and off within a specified time at a specified control voltage, have low turn-on and high turn-off resistance, and provide sufficient ruggedness. The following shows the four characteristics required for BRTs in comparison with general-purpose 60-V MOSFETs used for similar applications.



The greater the number of  $\star$ , the better.



**Figure 1-1 Switching circuit**

<span id="page-3-1"></span>The advantages of MOSFETs also include ease of device selection (i.e., ease of circuit design) and zero reactive current (i.e., power-saving). However, BRTs can also be used to configure switches at low cost if you understand selection guidelines for BRTs.

In the case of an NPN BRT like the one shown in Figure 1-1(b),  $R_1$  converts the control voltage applied to the base (B) terminal into current in order to stabilize the switching operation. In the off state, the control signal preceding the BRT might assume the high-impedance state. In that case, R<sub>2</sub> acts as a pull-down resistor, pulling the base voltage to the GND level.

Without  $R_2$ , the leakage current or the collector cut-off current ( $I_{CBO}$ ) flowing from the input at turn-off might cause the BRT to malfunction because of the charge accumulated in the base region. R2 helps prevent malfunction by passing leakage current to GND.

In the case of a PNP BRT,  $R_2$  acts as a pull-up resistor. There is no difference in the effects of  $R_1$ and R2 between NPN and PNP BRTs.

The bipolar transistor in the BRT has three distinct regions of operation: saturation, active, and cut-off regions. In the active region, the collector current is basically the base current times a given current gain. It is a current-driven device since the collector current is controlled via the base current. The ratio of the collector current to the base current in the active region (called the DC current gain) is represented by  $h_{FE}$ , which is 70 to 700 in the case of general-purpose bipolar transistors. As the base current is increased along the load line as shown by the arrow in Figure 1-2, the collector current increases proportionally according to  $h_{FE}$ . When the base current is further increased,  $h_{FE}$  decreases as the gaps between collector-emitter voltage curves become narrower. If the base current is increased further on the load line, the collector current will no longer increase. This region is called the saturation region. The BRT, which is used as a switch, is operated in the saturation region as well as in the cut-off region in which the bipolar transistor is off.



<span id="page-4-0"></span>**Figure 1-2 Static characteristics of the BRT (** $I_c$  **–**  $V_{CE}$  **curves)** 

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# <span id="page-5-0"></span>**2. Operation of the BRT**

This section describes how a BRT incorporating an NPN bipolar transistor turns on in the saturation region when the control voltage  $(V_I)$  applied to the B terminal is increased from the off state. For the sake of simplicity, let's consider the operation of a simple circuit shown in Figure 2-1.

1. The bipolar transistor, Q, is off.  $V<sub>I</sub>$  is gradually increased. Since Q is initially off, the current due to  $V_I$  flows only to  $R_1$  and  $R_2$ . Therefore,  $V_I$  is divided by  $R_1$  and  $R_2$ , and  $V_b$  is applied to the base (b) of Q.  $V_b = \{R_2 / (R_1 + R_2)\}\times V_I$ 



**Figure 2-1 Circuit used for the explanation of BRT operation**

<span id="page-5-1"></span>2. Q turns from off to on.

When  $V_b$  reaches roughly 0.6 V, the base current  $(I_b)$  begins to flow, turning on Q, as indicated by the  $V_{BE(sat)}$  - I<sub>C</sub> curve shown in Figure 2-2. This causes the collector current, which is  $I<sub>b</sub>$  times h<sub>FE</sub>, to flow. At this point in time, Q is still in the active region, not in the saturation region. Therefore, its h<sub>FE</sub> is 120 to 700, as is the case with the h<sub>FE</sub> of general-purpose bipolar transistors (such as the 2SC2712).

3. Q is on. (Transition from the active region to the saturation region)

As  $V_I$  increases further,  $V_{BE}$  increases. When the base voltage ( $V_b$ ) of the internal bipolar transistor is higher than 0.6 V, a slight increase in  $V<sub>b</sub>$  causes an exponential increase in the collector current (I<sub>C</sub>) as shown in the V<sub>BE(sat)</sub> - I<sub>C</sub> curves of Figure 2-2.

Therefore, once Q turns on,  $V_b$  remains almost constant without being affected by the division of  $V_I$  by  $R_1$  and  $R_2$ . All the excessive current (I<sub>B</sub> - I<sub>R2</sub>) flowing through  $R_1$  flows as the base current  $(I_b)$  to the bipolar transistor. When the bipolar transistor turns on, it is still in the active region where the collector current  $(I_C)$  is  $I_B * h_{FE}$ . However, since the collector-emitter voltage (V<sub>CE</sub>) is equal to V<sub>CC</sub> – R<sub>L</sub> \* I<sub>C</sub>, V<sub>CE</sub> decreases suddenly because of an increase in I<sub>C</sub>, causing the bipolar transistor to enter the saturation region.

In this region, both the base-emitter and base-collector pn junctions are forward-biased. Therefore, a large number of minority carriers are accumulated in the base region.

4. Q turns from on to off.

The voltage on VI is reduced. However, reducing  $V_I$  below the voltage specified as "input voltage (OFF)" does not cause the bipolar transistor to turn off immediately. This is because the collector current continues flowing until all the minority carriers in the base region are discharged through  $R_2$  or disappear as a result of recombination with majority carriers. The time required for this operation is called the storage time,  $t_{sta}$ . Q turns off after the minority carriers disappear.



**Figure 2-3 Operating locus of the BRT**

## <span id="page-6-3"></span><span id="page-6-2"></span><span id="page-6-0"></span>**3. Electrical characteristics as a switch**

The electrical characteristics of a BRT depend on the values of the internal resistors used. As mentioned in the comparison between BRTs and 60-V MOSFETs in Section 1, it is necessary to select the optimum BRTs. This section describes major electrical characteristics of BRTs and basic guidelines for BRT selection.

## <span id="page-6-1"></span>**3.1.** Voltage across switch terminals at turn-on (V<sub>CE(sat)</sub>)

<span id="page-6-4"></span> $V_{CE(sat)}$  is the collector-emitter voltage ( $V_{CE}$ ) when the BRT turns on.



The resistance between the terminals of a mechanical switch becomes almost zero when it is closed. However, for a BRT, it is necessary to use it in the saturation region where the collector-emitter resistance is low (i.e., the collector-emitter voltage is low). In the active region, the collector current increases proportionally with the base current according to  $h_{FE}$ . In contrast, in the saturation region,  $h_{FE}$  decreases as the saturation level increases (i.e.,  $V_{CE}$  decreases). Figure 3-2 shows the  $I_C-V_{CE}$  curves of a BRT, in which a load line at a  $V_{CC}$  of 5 V is highlighted in red. The load line intersects the I<sub>B</sub> = 0.2 mA curve at a V<sub>CE</sub> of 3.8 V, which means h<sub>FE</sub> = 160 when  $I_B = 0.2$  mA. However, the load line intersects the  $I_B = 6$  mA curve at a V<sub>CE</sub> of 0.2 V, meaning h<sub>FE</sub> = 20. Therefore, there are two ways to reduce the collector-emitter voltage ( $V_{CE}$ ):

- 1. Reducing the collector current (Increasing the load resistance,  $R_L$ ). (Red load line  $\Rightarrow$  blue load line)
- 2. Increasing the base current  $I_b$ .



**Figure 3-2 Reducing the collector-emitter saturation voltage, VCE(sat)** 

<span id="page-7-0"></span>Since the first way of reducing  $V_{CE(sat)}$  by increasing R<sub>L</sub> affects the load current (I<sub>C</sub>), the collector current can only be reduced to the extent permitted by the design requirements. Here, let's see how increasing the base current helps reduce  $V_{CE(sat)}$ . Look at the circuit shown in Figure 3-1(b). The assumption is that we are changing the control voltage  $(V<sub>I</sub>)$  for the RN1102 BRT (with  $R_1$ =R<sub>2</sub>=10 kΩ) from 0 V to 5 V.

Without the bipolar transistor, increasing  $V_I$  from 0 V to 5 V would obviously cause the voltage at b ( $V<sub>b</sub>$ ) to change from 0 V to 2.5 V because of the ratio of the R<sub>1</sub> and R<sub>2</sub> values. In reality, however,  $V_{\text{bf}}$  increases only up to roughly 1 V as shown in Figure 3-3 because of the presence of the bipolar transistor. The remaining current flows to the base terminal as  $I_b$ :

 $I_b$  =  $I_B - I_{R2}$  = ( $V_I - V_{bE}$ ) /  $R_1 - V_{bE}$  /  $R_2$ 

As indicated by this equation,  $I_b$  can be increased by increasing  $I_b$  and reducing  $I_{R2}$  using a BRT with:

- $\bullet$  Small R<sub>1</sub> value
- $\bullet$  Large R<sub>2</sub> value

What is important here are the absolute values of  $R_1$  and  $R_2$ , not the ratio of  $R_1$  to  $R_2$ .

The collector-emitter saturation voltage increases as temperature increases, as shown in Figure

3-4. Take the above characteristics into consideration to achieve the optimum design.



 $Figure 3-4$   $V_{CE(sat)} - I_C$   $I_C$  curves (RN1102)

## <span id="page-8-3"></span><span id="page-8-2"></span><span id="page-8-0"></span>**3.2. Withstand voltages**

The withstand voltages that should be considered are the maximum voltage applied across the switch terminals at switch-off as well as the maximum and minimum control voltages.

### <span id="page-8-1"></span>**3.2.1. Maximum voltage across switch terminals at switch-off (collector-emitter withstand voltage)**

This is defined as the collector-emitter voltage ( $V_{CEO}$ ) with the base (B) open. Toshiba's BRTs incorporate a general-purpose bipolar transistor similar to the 2SC2712 and 2SA1162 with a collector-emitter voltage of 50 V.

#### <span id="page-9-0"></span>**3.2.2. Control voltage (maximum and minimum emitter-base voltages, V<sub>EBO</sub>)**

#### **Forward direction:**

As the control voltage increases, the BRT transitions from the off state to the on state.

In the case of a general bipolar transistor without resistance, as the control voltage is increased after turn-on, its collector current or collector power dissipation reaches the maximum rated value if it is in the active region, making it impossible to increase the control voltage any further. If the bipolar transistor is in the saturation region, its operation is often constrained by the rated base or collector current.

Since BRTs are usually operated in the saturation region, care should be exercised as to the base and collector currents. The allowable power dissipation of the bias resistors of a BRT is specified as  $1/8$  W. Accordingly, the maximum control voltage ( $V<sub>I</sub>$ ) is basically determined as described below:

- 1. When  $R_1$  is large: Power dissipation of  $R_1$
- 2. When  $R_1$  is small: Maximum collector current (I<sub>C</sub>)
- 1. Power dissipation of  $R_1$



**Figure 3-5 Forward control voltage**

Let the base-emitter voltage of the internal bipolar transistor at turn-on be  $V_{be}$ .

Then, the current flowing through  $R_1$  (I<sub>B</sub>) is expressed as follows. For the sake of simplicity, the assumption is  $V_{be} = 0.7 V$ .

 $I_B = (V_I - V_{be}) / R_1 = (V_I - 0.7) / R_1$ 

The power dissipation of  $R_1$  due to  $I_B$  must not exceed 1/8 W. Hence:

$$
1/8 \text{ W} > R_1 * \{ (V_1 - 0.7) / R_1 \}^2
$$
  
>  $(V_1 - 0.7) ^2 / R_1$ 

 $V_I \qquad \langle (R_1 / 8)^{1/2} + 0.7 \qquad (1)$ 

2. Maximum collector current  $(I<sub>C</sub>)$ 

The current flowing to the base (b) of the internal bipolar transistor  $(I_b)$  can be calculated by subtracting the current flowing to  $R_2$  (I<sub>R2</sub>) from I<sub>B</sub>:

$$
I_b = I_B - I_{R2} = (V_I - V_{be}) / R_1 - V_{be} / R_2 = (V_I - 0.7) / R_1 - 0.7 / R_2
$$

Since the collector current (I<sub>C</sub>) is equal to I<sub>b</sub> times h<sub>FE</sub> under operating conditions, the following equation must be satisfied:

$$
I_{C}(max) > I_{C} = h_{FE} * I_{b} = h_{FE} * \{ (V_{I} - 0.7) / R_{1} - 0.7 / R_{2} \}
$$
  
\n
$$
V_{I} < R_{1} * I_{C}(max) / h_{FE} + (R_{1} + R_{2}) * 0.7 / R_{2}
$$
 (2)

The lower of the  $V_I$  values calculated based on the following two factors is the maximum allowable  $V_I$  value.

Figure 3-6 indicates the tendency of the maximum  $V_I$  value, although it should be considered merely as a guide. Basically,  $V_1$  is determined by the allowable power dissipation of bias resistor  $R_1$ (1/8 W). However, the maximum V<sub>I</sub> value depends on the rated collector current (I<sub>C</sub>) when R<sub>1</sub> is small and  $h_{FE}$  is relatively large.







#### **Reverse direction:**

Let's consider the emitter-base voltage of the internal bipolar transistor (which is equivalent to the general-purpose bipolar transistors of the 2SC2712/2SA1162 class). The emitter is the positive side of the transistor. In the case of bipolar transistors without bias resistors, the emitter-base voltage is represented by  $V_{EBO}$ . In the case of BRTs, the internal bipolar transistor is off when the emitter-base voltage is applied. Therefore, the emitter-base voltage is determined by  $R_2$  / ( $R_1+R_2$ ). And therefore, BRTs with a higher resistor ratio ( $R_1/R_2$ ) provide higher V<sub>EBO</sub> as shown in Figure 3-6.

The reverse voltage is the overshoot / undershoot (negative voltage) that occurs when the control input voltage VI reverses, and the voltage at the emitter terminal may become higher than the voltage at the base terminal. Care should be exercised to prevent such a situation.



<span id="page-10-0"></span>**Figure 3-7 Reverse control voltage**



# <span id="page-11-0"></span>**3.3.** Control voltages (input voltage (ON) (V<sub>I(ON)</sub>) and input voltage (OFF)  $(V<sub>I(OFF)</sub>)$

In the case of a bipolar transistor, the base current begins to flow at the threshold voltage  $(V_b)$ of roughly 0.6 V, causing the transistor to switch on or off. When a switch circuit is configured using a BRT as shown in Figure 3-1, the input voltage  $(V<sub>I</sub>)$  at which Q begins to turn on is inversely proportional to  $R_2$  and proportional to  $R_1$ , as indicated by the following equations:

$$
V_{be} = R_2/(R_1+R_2) * V_I
$$

 $V_1 = (R_1 + R_2) * V_{be}/R_2 = (R_1/R_2 + 1) * V_{be}$ 

The input voltage (ON) and input voltage (OFF) of a BRT are defined as follows: (Ta=25°C)

- Input voltage (ON),  $V_{IN(ON)}$ : Voltage required to obtain the collector current equal to or higher than the prescribed value (e.g.,  $I_C = 5$  mA) at  $V_{CF} = 0.2$  V
- Input voltage (OFF), V<sub>IN(OFF)</sub>: Voltage required to keep the collector current equal to or lower than the prescribed value (e.g.,  $I_c = 0.1$  mA) at  $V_{CE} = 5$  V

Since BRTs are used in the saturation region as described above, minority carriers accumulate in the base region after the internal bipolar transistor turns on before they enter the saturation region. BRTs do not switch off until the accumulated minority carriers are swept out of the base region.

The current to charge and discharge the base is constrained by  $R_1$  at turn-on.  $R_1$  and  $R_2$  have different effects on even BRTs with the same resistor ratio  $(R_1/R_2)$ . Figure 3-9 plots the maximum V<sub>I(ON)</sub> values shown in datasheets.





<span id="page-11-1"></span>

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#### <span id="page-12-0"></span>**3.4. Switching times**

The switching times of the bipolar transistor are defined as shown in Figure 3-10.

**Turn-on time = delay time**  $(t_d)$  **+ rise time**  $(t_r)$ **Turn-off time = storage time (** $t_{sta}$ **) + fall time (** $t_f$ **)** 

In the case of bipolar transistors, the accumulation of charge  $(Q_B)$  in the base region begins immediately upon turn-on. BRTs, which are operated in the saturation region, continue accumulating excessive charge even after they turn on. Charge accumulation lasts until  $(T_n * I_b)$ , a value that is determined by the lifetime ( $\tau_n$ ) and base current ( $I_b$ ) of the internal bipolar transistor.

At turn-off, BRTs remain on for a period of  $t_{\text{sta}}$  until the excessive charge accumulated after turn-on is swept out of the base region. Thereafter,  $I_B$  decreases exponentially.

Table 1 shows examples of the results of measurements of these BRT characteristics. The measurements were taken at a  $V_{CC}$  of 5 V, switching the input voltage from 0 V to 5 V and vice versa. The load resistance (RL) is 1 kΩ. As indicated in Table 3-1, t<sub>stg</sub> constitutes a dominant portion of the switching time.

**Table 3-1 Examples of the results of measurements of BRT switching times**

Type	$ R_1(k\Omega) R_2(k\Omega) t_r(ns) t_{stg}(ps) t_f(ps)$				
RN1401	4.7	4.7	38	1.89	0.11
<b>RN1402</b>	10	10	60l	2.25	0.13
<b>RN1403</b>	22	22	118	2.41	0.21





<span id="page-12-1"></span>There are two considerations for reducing  $t_{sta}$ :

1. Minimize the accumulation of excess carriers.

This helps reduce the saturation depth of the BRT while it is on. Shallow saturation means high  $h_{FE}$ . As can be seen from Figure 3-11, the collector current of a BRT depends mainly on supply voltage (V<sub>CC</sub>) and load resistance (R<sub>L</sub>). V<sub>CE(sat)</sub> contributes less to the collector current. Therefore, even if I<sub>B</sub> is decreased and  $h_{FE}$  is increased, the effect on the output voltage can often be ignored. When priority is given to switching time, it is advantageous to select a BRT with a large  $R_1$ 





#### 2. Remove excess carriers quickly.

Excess carriers accumulated in the base region are removed mainly through  $R_2$  although the carrier removal path slightly differs depending on the configuration of the preceding circuit. ( $R_1$ ) has a great influence on the saturation depth as described in  $1$ . When R<sub>1</sub> is large, there are few excess carriers, which is advantageous for the emission time.). Therefore, BRTs with a low  $R_2$ value are suitable for increasing the switching speed.

#### **Table 3-3 Effects of R<sub>2</sub> on t<sub>stg</sub>**

<span id="page-13-0"></span>



**Figure 3-11 Collector current**

# <span id="page-14-0"></span>**4. Types of BRTs**

Table 4-1 shows the lineup of single BRTs. Toshiba offers BRTs with many resistor combinations so that you can find one that satisfies your electrical characteristics requirements.

Toshiba also offers 2-in-1 BRTs shown in Figure 4-1.

#### **Table 4-1 Lineup of single BRTs**





# AEC-Q101-qualified

The 2-in-1 BRTs are available in five-pin common-emitter, six-pin point-symmetrical, and parallel configurations.

Most 2-in-1 BRTs consist of an NPN or PNP pair, and parallel 2-in-1 BRTs also have the NPN/PNP configuration.



<span id="page-14-1"></span>a) Common-emitter b) Point-symmetrical c) Parallel





**Figure 4-1 2-in-1 BRTs**

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# <span id="page-15-0"></span>**5. Selection guidelines**

In most cases, BRTs are used as switches. Therefore, let's assume the use of BRTs as switches. Considerations for BRTs include the following:

- 1. Compatibility with the control circuit at the previous stage (selection of an NPN or PNP BRT)
- 2. Turning on and off the transistor without fail via a control signal ( $V_{I(ON)}$  and  $V_{I(OFF)}$  voltages)
- 3. Obtaining necessary voltage when the transistor is on (i.e., reducing a drop in the collector-emitter voltage in the "on" state)
- <span id="page-15-1"></span>4. Reducing the turn-on or turn-off time (i.e., increasing the switching speed)



**Figure 5-1 Basic circuit**

These considerations are explained below using the basic circuit with an NPN BRT shown in Figure 5-1 (which is the same as the one shown in Figure 2-1). The BRT is enclosed in the dashed box.  $V_I$  is the control signal,  $V_{CC}$  is the supply voltage, and  $R_L$  is the load, including a pull-up resistor.

Each guideline for the selection of BRTs is discussed in the following subsections. Figure 5-2 shows the concepts of the electrical characteristics of BRTs.



<span id="page-15-2"></span>**Figure 5-2 Selection of electrical characteristics**

## <span id="page-16-0"></span>**5.1. Matching with the control circuit at the previous stage (selection of an NPN or PNP BRT)**

Select either an NPN or PNP BRT according to the preceding control circuit. BRTs are often preceded by a circuit that can assume a high-Z state as shown in Figure 5-3. Use an NPN BRT if the output of the preceding circuit has a pull-down resistor. Use a PNP BRT if it has a pull-up resistor. Using the wrong type of BRT might, as shown in Figure 5-4, cause a BRT to malfunction at the midpoint potential between the pull-up resistor and the built-in bias resistors when the output of the preceding circuit is in the high-Z state.

Do not connect multiple NPN and PNP BRTs in parallel as shown in Figure 5-5 because the midpoint potential generated by each built-in bias resistor causes a malfunction.



#### <span id="page-16-2"></span><span id="page-16-1"></span>**Figure 5-4 BRT preceded by pull-up resistor**



#### <span id="page-16-3"></span>**Figure 5-5 Connecting NPN and PNP BRTs in parallel**

## <span id="page-17-0"></span>**5.2. Turning on and off the BRT without fail via a control signal (** $V_{I(ON)}$  **and**  $V_{I(OFF)}$ **) voltages)**

Input voltage (ON) ( $V_{I(ON)}$ ) and input voltage (OFF) ( $V_{I(OFF)}$ ) are specified at 25°C in the datasheet. When designing a circuit, it is necessary to select BRTs that provide high-level  $V_I$ voltage of the control circuit at the previous stage higher than the maximum  $V_{I(ON)}$  voltage and low-level  $V_I$  voltage lower than the minimum  $V_{I(OFF)}$  voltage. Allow sufficient design margins according to the usage environment.

See Section 3.3, "Control voltages," for collector current (Ic) vs. input voltage (V<sub>I</sub>) curves.

- $\bullet$  BRTs with higher R<sub>1</sub>/R<sub>2</sub> provide higher V<sub>I(ON)</sub>.
- **•** BRTs with higher R<sub>1</sub> provide higher  $V_{I(ON)}$  if they have equal  $R_1/R_2$ .

## <span id="page-17-1"></span>**5.3. Obtaining necessary output voltage when the BRT is on**

(Reducing a drop in the collector-emitter voltage in the "on" state)

For example, when the NPN BJT turns on in the saturation region, the collector voltage drops to the GND level because of an external resistor  $(R<sub>L</sub>)$  and the collector current  $(I<sub>C</sub>)$ . In practice, however, there is a voltage level called collector-emitter saturation voltage ( $V_{CE(sat)}$ ) between the collector and GND (emitter) potentials.  $V_{CE(sat)}$  can be reduced to some extent by increasing the base current  $(I_B)$ .

 $I<sub>b</sub>$  can be expressed as follows using V<sub>I</sub>. This equation indicates that  $I<sub>b</sub>$  can be increased by using a BRT with the following two conditions.

 $I_b = I_B - I_{R2} = (V_I - V_{be}) / R_1 - V_{be} / R_2$ 

- $\bullet$  Small R<sub>1</sub> value
- $\bullet$  Large R<sub>2</sub> value

Such BRTs pass a greater current to the base at a given input voltage  $(V<sub>1</sub>)$ . For details on the input voltage, see Section 3.1, "Voltage across switch terminals at turn-on (V $_{CE(sat)}$ )."

## <span id="page-17-2"></span>**5.4. Reducing the turn-on or turn-off time**

(Increasing the switching speed)

Storage time  $(t_{sta})$  constitutes a dominant portion of the switching time because of the charge accumulated in the base region. Therefore, switching speed can be reduced by reducing the amount of charge accumulated in the base region and increasing the speed at which it is discharged. Select BRTs, taking the following points into consideration. For details, see Section 3.4, "Switching times." This requirement contradicts the description in Section 5.3.

- Do not bring a BRT into a deeper saturation level than is necessary.
	- $\Rightarrow$  Large R<sub>1</sub> value
- Reduce the impedance of the path through which excess carriers are removed.  $\Rightarrow$  Small R<sub>2</sub> value

Select a BRT with a small  $R_2$  value because excess carriers are removed mainly through  $R_2$ . Excess carriers also disappear as a result of carrier recombination in the base region. There is a limit to a reduction in  $t_{\text{stg}}$  through carrier discharging.

# <span id="page-18-0"></span>**6. Calculating the power dissipation of a BRT**

For example, in amplifiers, bipolar transistors are used at high  $h_{FE}$ , causing the collector power dissipation (V<sub>CE</sub>  $*$  I<sub>C</sub>) to be dominant. In contrast, BRTs are commonly used at an h<sub>FE</sub> of 10 to 20. Therefore, other sources of power dissipation cannot be ignored. It is necessary to consider the sum of the power dissipation of the internal bipolar transistor (Q) and bias resistors ( $R_1$  and  $R_2$ ) of a BRT.

The following shows a simple calculation example. Notice that bias resistor  $R_1$  causes the greatest power dissipation.

Suppose that the BRT is the RN1402 (R<sub>1</sub>=R<sub>2</sub>=10 kΩ), the input voltage (V<sub>I</sub>) is 10 V, the collector-emitter voltage ( $V_{CE}$ ) is 0.2 V, the base-emitter voltage ( $V_{be}$ ) is 0.7 V, and the operating current gain ( $h_{FE}$ ) of the internal bipolar transistor is 10.

The BRT is enclosed by a dashed box in Figure 6-1. Let's calculate the amounts of currents indicated in the dashed box.



Let the power dissipation of  $R_1$  and  $R_2$  be  $P_{R1}$  and  $P_{R2}$  respectively and the collector-emitter and base-emitter power dissipation of the bipolar transistor be  $P_{CE}$  and  $P_{be}$  respectively.



Hence, the power dissipation (P) of the BRT is calculated as:

 $P = P_{R1} + P_{R2} + P_{CE} + P_{be} = 11.02 \text{ mW}$ 



<span id="page-18-1"></span>**Figure 6-1 Basic circuit**

<span id="page-19-0"></span>



<span id="page-19-1"></span>For the lineup of BRTs  $\rightarrow$  [Click Here](https://toshiba.semicon-storage.com/list/index.php?code=param_307®ion=apc&lang=en)



# **Basics of Bias Resistor Built-in Transistors (BRTs) Application Note**

# <span id="page-20-0"></span>**8. Related Links**

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# <span id="page-21-0"></span>**9. RESTRICTIONS ON PRODUCT USE**

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