

## Electrical Characteristics of Bias Resistor Built-In Transistors (BRTs)

### **Outline:**

This document describes the absolute maximum rating, electrical characteristics, and product numbering methods in the datasheet of a built-in-resistor transistor (BRT, also called as a digital transistor) used as a semiconductor switches.

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### 1. Introduction

Also called digital transistors, bias resistor built-in transistors (BRTs) are used as on/off switches. BRTs incorporate a series base resistor and a base-emitter bias resistor necessary for such applications. Therefore, BRTs help reduce the parts count, size, and the time required for the assembly of electronic applications.

Toshiba provides BRTs with a wide range of resistor values to meet the requirements of various digital circuits. Toshiba's BRTs are available in single and dual (2-in-1) versions and in various packaging options.

This application note mainly describes the maximum ratings and electrical characteristics shown in the BRT datasheets. They are specified under the assumption that BRTs are used as on/off switches. Specifications as switches include control voltage, withstand voltage across a switch in the off state (off-state withstand voltage), and voltage across a switch in the on state (on-resistance).

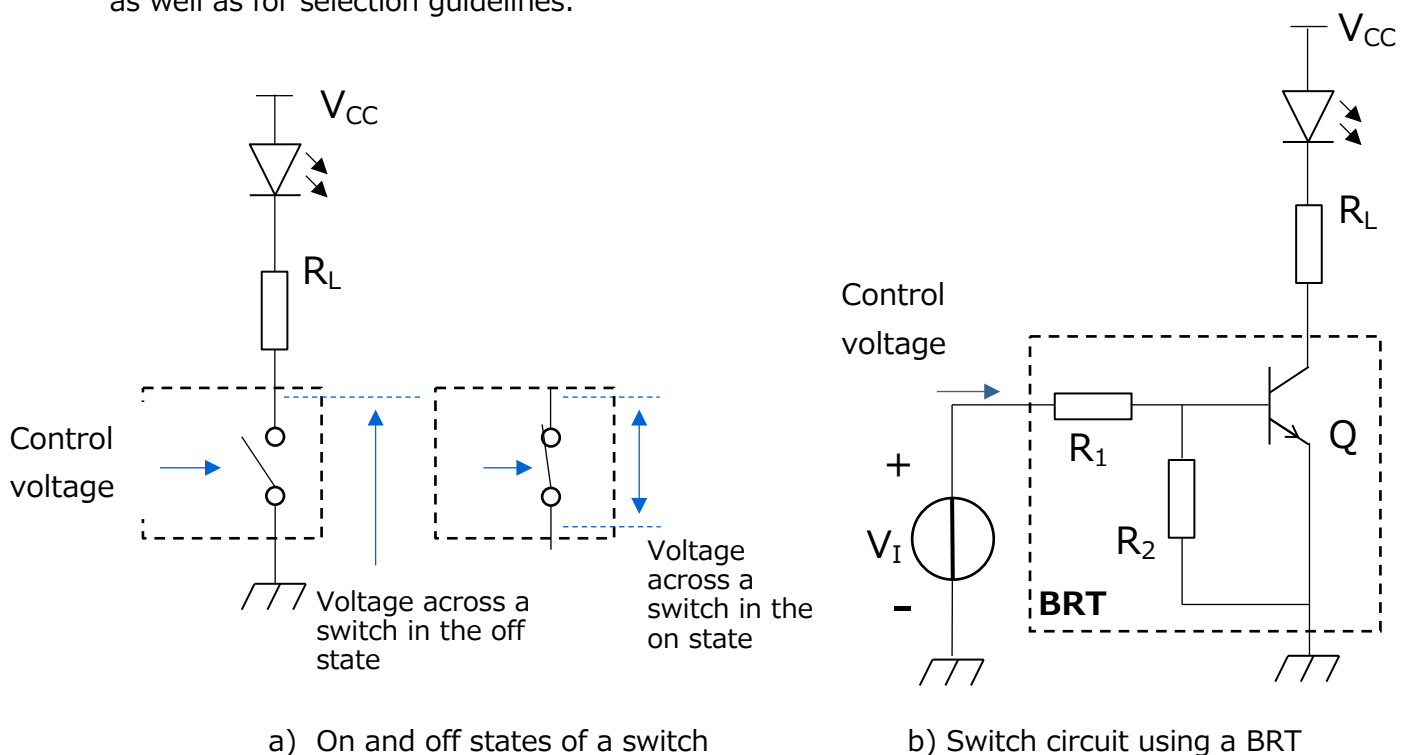
The relationships between these specifications and the BRT characteristics are as follows:

Control voltage  $\Rightarrow$  Input voltage (ON), input voltage (OFF)

Voltage across a switch in the off state  $\Rightarrow$  Collector-emitter voltage

Voltage across a switch in the on state  $\Rightarrow$  Collector-emitter saturation voltage

The requirements for these characteristics can be met by selecting BRTs with appropriate internal resistor values ( $R_1$  and  $R_2$ ). See the application note "Basics of Bias Resistor Built-in Transistors (BRTs)" for the relationships between internal resistors and electrical characteristics as well as for selection guidelines.



**Figure 1-1 On and off states of a switch and a switch circuit using a BRT**

### 2. Part naming conventions

This section shows the basic part naming conventions that Toshiba uses for its BRTs. BRTs are available in several types with different configurations as shown in Figure 2-1.

#### 2.1. Part numbers beginning with RN

Example: RN 1 3 14 JE

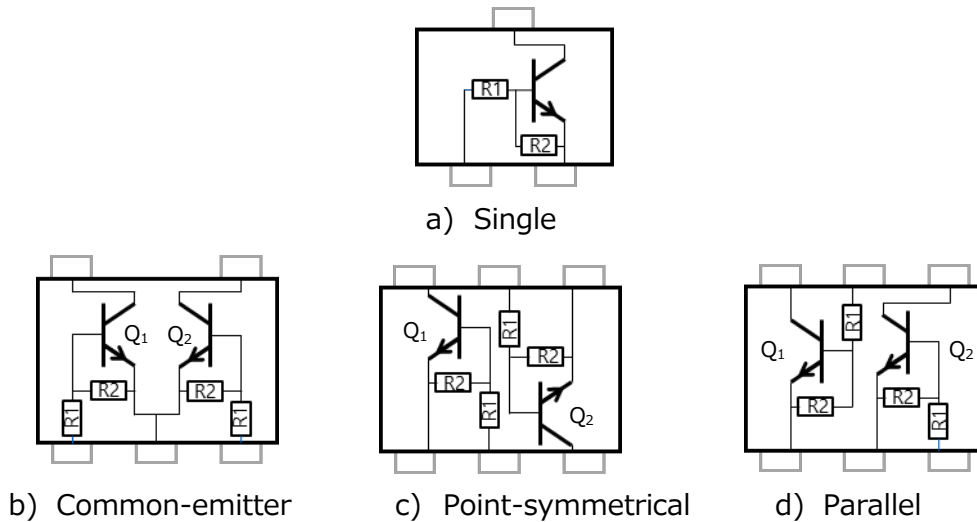
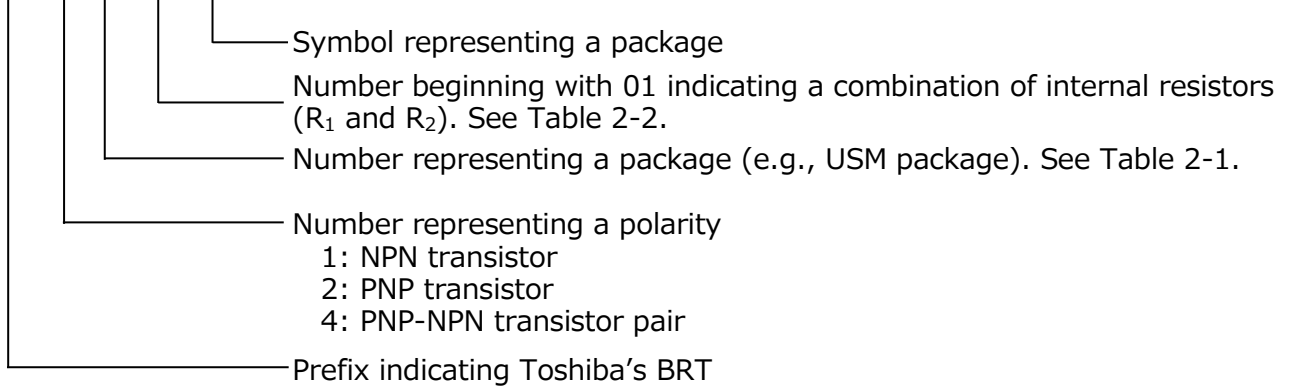


Figure 2-1 BRTs with different configurations

Table 2-1 Examples of package numbers and symbols

Package	Package code	Part number example	Number representing a package*	Symbol representing a package*	Type
VESM	SOT-723	RN1 <b>101</b> MFV	<b>1</b>	<b>MFV</b>	<b>Single</b>
SSM	SOT-416	RN1 <b>101</b>	<b>1</b>	Null	
USM	SOT-323	RN1 <b>301</b>	<b>3</b>	Null	
S-Mini	SOT-346	RN1 <b>401</b>	<b>4</b>	Null	
ESV	SOT-553	RN1 <b>701</b> JE	<b>7</b>	<b>JE</b>	<b>2-in-1 (Common-emitter)</b>
USV	SOT-353	RN1 <b>701</b>	<b>7</b>	Null	
SMV	SOT-25	RN1 <b>501</b>	<b>5</b>	Null	
ES6	SOT-563	RN1 <b>901</b> FE	<b>9</b>	<b>FE</b>	<b>2-in-1 (Point-symmetrical/parallel)</b>
US6	SOT-363	RN1 <b>901</b>	<b>9</b>	Null	
SM6	SOT-26	RN1 <b>601</b>	<b>6</b>	Null	

Table 2-2 shows the combinations of internal resistors available for single and 2-in-1 BRTs. Most 2-in-1 BRTs consist of two combinations of identical transistors ( $Q_1$  and  $Q_2$ ) with resistors ( $R_1$  and  $R_2$ ) having equal values. Table 2-2 shows only such  $R_1$ - $R_2$  combinations. Toshiba also provides 2-in-1 BRTs consisting of two transistors with different-value resistors—namely, the RN46A1, RN49A1, and RN49A2. For  $R_1$ - $R_2$  combinations available with these BRTs, see their datasheets.

**Table 2-2 Internal resistor combinations available with each type of BRT**

As shown in the table below, the part number of the RNxxxx series contains a number that represents a combination of internal resistors.

(Example: RN1101MFV  $\Rightarrow R_1 = R_2 = 4.7 \text{ k}\Omega$ )

a) Single

$R_1 \text{ (k}\Omega)$ \ $R_2 \text{ (k}\Omega)$	$I_C = 100 \text{ mA}$						$I_C = 800 \text{ mA}$			
	4.7	10	22	47	100	$\infty$	1	2.2	4.7	10
0.47										25
1		14				19	21			26
2.2		15		05				22		27
4.7	<b>01</b>	16		06		10			23	
10	17	02		07		11				24
22			03	08		12				
47		18	09	04		13				
100					30	31				
200						32				

b) 2-in-1 BRTs with a common-emitter configuration

$R_1 \text{ (k}\Omega)$ \ $R_2 \text{ (k}\Omega)$	4.7	10	22	47	$\infty$
1		14			
2.2				05	
4.7	01			06	10
10		02		07	11
22			03	08	12
47			09	04	13

c) 2-in-1 BRTs in a point-symmetrical configuration (NPN\*2, PNP\*2, PNP+NPN)

$R_1 \text{ (k}\Omega)$ \ $R_2 \text{ (k}\Omega)$	4.7	10	22	47	$\infty$
2.2				05	
4.7	01			06	10
10		02		07	11
22			03	08	12
47			09	04	

d) 2-in-1 BRTs in a parallel configuration

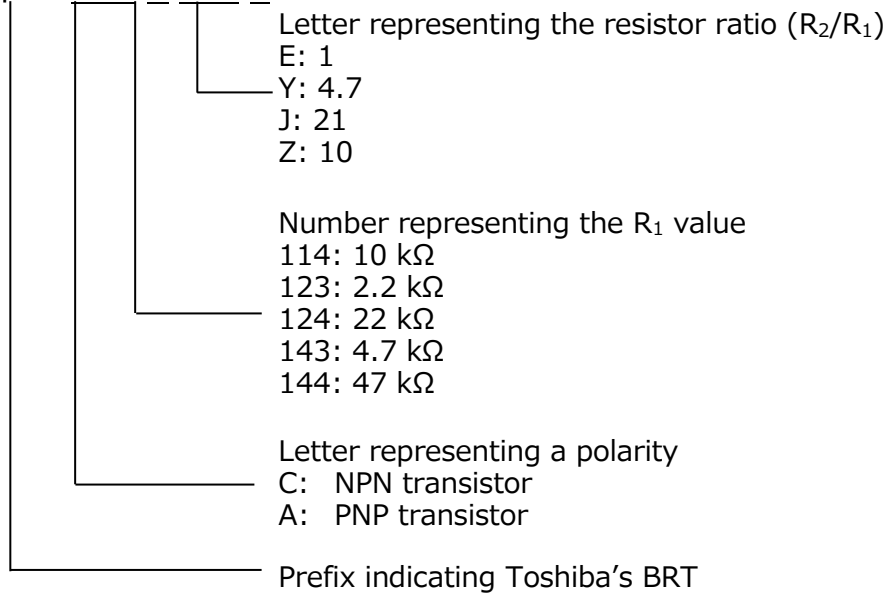
$R_1 \text{ (k}\Omega)$ \ $R_2 \text{ (k}\Omega)$	4.7	10	22	47	$\infty$
2.2				65	
4.7	61				70
10		62		67	71
22			63	68	
47			69	64	

e) 2-in-1 BRTs in a point-symmetrical configuration (NPN+PNP)

$R_1 \text{ (k}\Omega)$ \ $R_2 \text{ (k}\Omega)$	4.7	10	22	47	$\infty$
2.2				05	
4.7	01			06	10
10		02		07	11
22			03	08	12
47			09	04	

## 2.2. Part numbers beginning with TDT

Example: TDT C 114 E



### 3. Absolute maximum ratings

#### 3.1. Definition of maximum ratings

The operation and function of semiconductor devices are substantially constrained by the applied voltage, current, temperature, power dissipation, and other factors.

Maximum ratings are the permissible values that must not be exceeded in order to ensure that semiconductor devices operate properly and maintain sufficient reliability. These values are specified as absolute maximum ratings.

None of the absolute maximum ratings must be exceeded, even instantaneously. Exposure to conditions exceeding the maximum ratings may damage or degrade a device.

They are specified at an ambient temperature of 25°C unless otherwise specified.

Overvoltage and overcurrent conditions cause internal degradation of semiconductor devices. In the worst-case scenario, these conditions might lead to wire melting by internal heating or permanent damage of semiconductor chips. Excessive storage or operating temperature might not only degrade semiconductor devices but also cause an open-circuit failure of wire bonds or degradation of hermeticity owing to a difference in thermal expansion coefficient among different types of materials that constitute a semiconductor device.

Absolute maximum ratings include the permissible voltage and current at each terminal, power dissipation, junction temperature, and storage temperature. The stresses specified as absolute maximum ratings differ from device to device. When parameters are shown as maximum ratings in datasheets and other technical documents, they mean absolute maximum ratings.

#### 3.2. Collector-base voltage ( $V_{CB0}$ )

Voltage is applied with the emitter (E) open as shown in 3-1 so that the pn junction between the base (b) and collector (C) is reverse-biased.  $V_{CB0}$  is the maximum voltage that can be applied across the collector (C) and base (B) terminals. When voltage (V) is low, current does not flow because the diode formed by the pn junction is off. As voltage is increased, leakage current begins to flow, as is the case with typical diodes, eventually degrading and destroying the BRT.

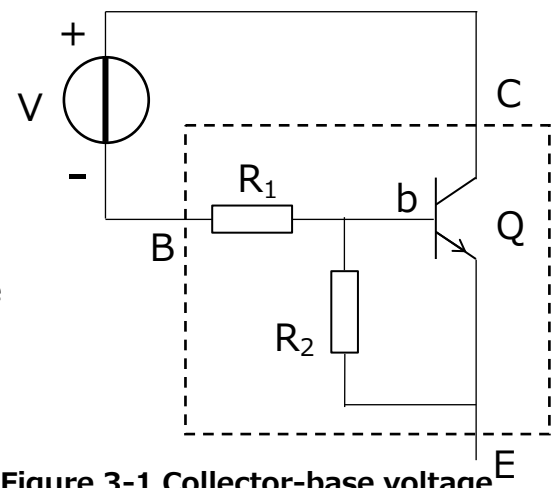


Figure 3-1 Collector-base voltage

#### 3.3. Collector-emitter voltage ( $V_{CE0}$ )

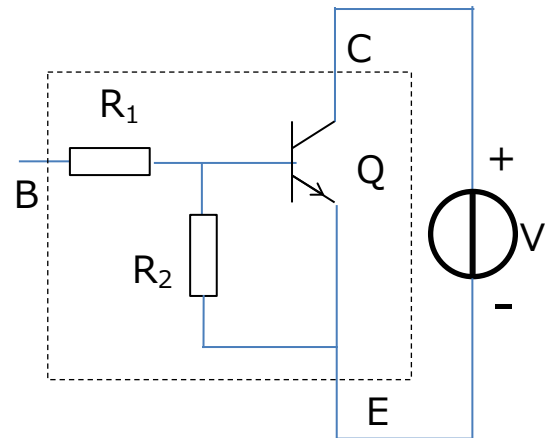
Voltage is applied across the collector (C) and emitter (E) terminals with the base (B) terminal open-circuited as shown in Figure 3-2.  $V_{CE0}$  is the maximum voltage that can be applied across the collector (C) and emitter (E) terminals. When a BRT is used as a switch,  $V_{CE0}$  is the maximum voltage that can be applied when it is off.

When voltage is applied as shown in Figure 3-2, the pn junction between the base (b) and collector (C) is



reverse-biased while the pn junction between the base (b) and emitter (E) is forward-biased, as is the case with a transistor operating in the linear region. Since the pn junctions are biased in the same direction as for a transistor in the linear region, the BRT begins to operate as a transistor as the base current flows into Q.

As described in the previous section, application of large voltage across the collector and base terminals causes collector cut-off current ( $I_{CBO}$ ) to flow from the collector to the base. When  $I_{CBO}$  flows into the base, it is amplified by the DC forward current gain ( $h_{FE}$ ) to produce the amplified collector current. Therefore,  $V_{CEO}$  depends on the collector-base voltage  $V_{CBO}$ .



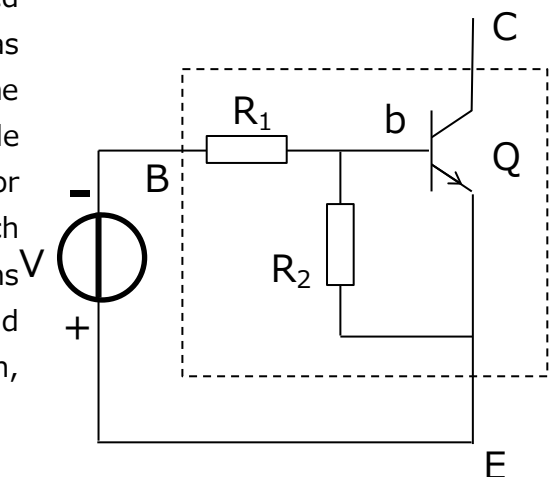
**Figure 3-2 Collector-emitter voltage (NPN BRT)**

### 3.4. Emitter-base voltage ( $V_{EBO}$ )

Voltage is applied with the collector terminal (C) open as shown in Figure 3-3 so that the pn junction between the emitter (E) and base (b) is reverse-biased.

Since it is reverse-biased, no current flows through the built-in transistor when voltage is low. Current flows when voltage rises to such a level as to cause breakdown of the pn junction.

Since BRTs contain resistors  $R_1$  and  $R_2$ , when the reverse bias voltage is low, current flows through the built-in resistors. Therefore, the voltage divided by these resistors is applied across b and E.  $V_{EBO}$  is defined as the external reverse bias voltage (V) at which this divided voltage exceeds the breakdown voltage. BRTs with a higher resistor ratio provide a higher  $V_{EBO}$ . Generally, the emitter, base, and collector regions of an internal transistor of the BRT are doped in such a manner that the relationship of their dopant concentrations becomes emitter > base > collector. Since the withstand voltage is inversely proportional to the dopant concentration,  $V_{EBO}$  is smaller than  $V_{CBO}$ .



**Figure 3-3 Emitter-base voltage (NPN BRT)**

### 3.5. Collector current ( $I_C$ ), output current ( $I_O$ )

$I_C$  and  $I_O$  are the maximum currents that can flow through the collector pn junction in the reverse direction when a transistor is operating (when its operating point (Q point) is in the linear or saturation region). Since  $I_C$  and  $I_O$  are the maximum collector currents when a BRT is operating mainly in the linear region, they might be constrained by other electrical characteristics, depending on the operating condition. When the BRT goes into deep saturation (with low  $h_{FE}$ ), ensure that the power dissipated by  $R_1$  does not exceed 1/8 W (see Section 4.8, "Internal resistors").

### 3.6. Collector power dissipation ( $P_C$ ), power dissipation ( $P_D$ )

The power dissipated in a BRT includes not only collector power dissipation ( $I_C \times V_{CE}$ ) but also the power dissipated by other elements that constitute the BRT, including the power dissipated by the internal resistors and the emitter.

In the case of a typical bipolar transistor operating in the linear region, the emitter power dissipation is related to the base current of the internal transistor ( $I_b$ ) and the base-emitter voltage ( $V_{bE}$ ) of the internal transistor to which  $I_b$  flows. Because  $I_b = I_C / h_{FE}$ , the emitter power dissipation is small with respect to the collector current ( $I_C$ ) and collector-emitter voltage ( $V_{CE}$ ). Therefore, the collector power dissipation is treated as the power dissipation of a transistor. In the case of the BRT, the total power dissipated by all the constituent elements is called the collector power dissipation, following the conventional nomenclature for bipolar transistors.

For an example of calculation of collector power dissipation, see Section 6, "Calculating the power dissipation of a BRT," of the application note *Basics of Bias Resistor Built-in Transistors (BRTs)*.

The collector power dissipation of a BRT is calculated as follows:

For the sake of simplicity,  $V_{bE} = 0.7 \text{ V}$  and  $V_{CE} = 0.2 \text{ V}$  may be used.

$$P_C = V_{CE} \times I_C + V_{bE} \times (I_B - V_{bE} / R_2) + R_1 \times I_B^2 + V_{bE}^2 / R_2$$

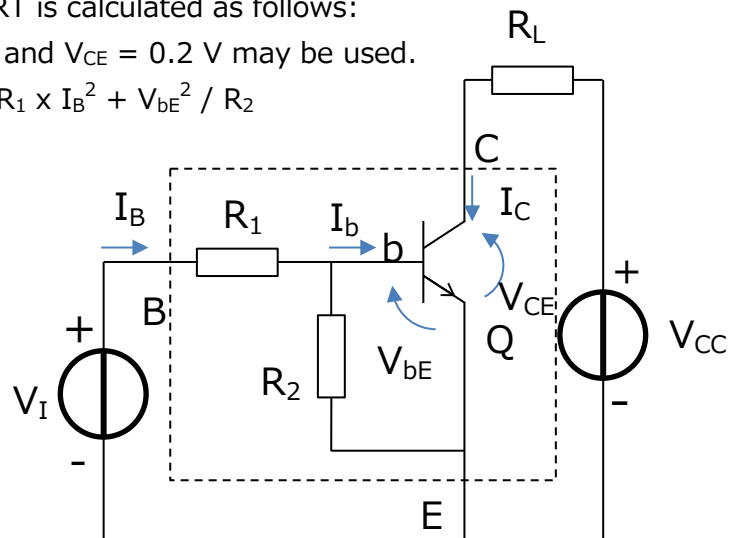


Figure 3-4 Collector power dissipation ( $P_C$ ) (NPN BRT)

### 3.7. Junction temperature ( $T_j$ )

$T_j$  is the maximum temperature at the pn junction of an internal transistor. At higher temperatures, numerous electrons and holes are generated in both the p and n regions. This reduces differences between p-type and n-type semiconductors, causing their interfaces not to function as pn junctions. Consequently, excessive current might flow in the transistor, leading to destruction. In addition, the service life of semiconductor devices is affected by temperature (see the description of the Arrhenius model in Section 3.3.3 of *Reliability Handbook*). It is therefore necessary to take not only temperature characteristics but also temperature derating into consideration.

### 3.8. Storage temperature ( $T_{stg}$ )

$T_{stg}$  is the temperature range in which BRTs should be stored without voltage application.

## 4. Electrical characteristics of BRTs

Since BRTs are generally used as switches, their use as switches is assumed in this section. The following subsections describe the electrical characteristics to be considered when using BRTs as switches.

### 4.1. Collector cut-off current ( $I_{CBO}$ , $I_{CEO}$ )

There are two definitions of collector cut-off current:  $I_{CBO}$  and  $I_{CEO}$ .  $I_{CBO}$  is related to  $V_{CBO}$  described in Section 3.2, "Collector-base voltage ( $V_{CBO}$ )," whereas  $I_{CEO}$  is related to  $V_{CEO}$  described in Section 3.3, "Collector-emitter voltage ( $V_{CEO}$ )."

#### 4.1.1. Collector cut-off current ( $I_{CBO}$ )

Voltage is applied across the collector (C) and base (B) terminals with the emitter (E) terminal open-circuited as shown in Figure 4-1 so that the pn junction between the collector and base is reverse-biased. This causes the pn-junction diode between the collector (C) and base (b) of the internal transistor (Q) to be reverse-biased. As this reverse bias increases, leakage current begins to flow. The maximum leakage current is defined as the collector cut-off current ( $I_{CBO}$ ).

$I_{CBO}$  is highly dependent on temperature. It is expressed as follows as a function of temperature:

$$I_{CBO}(T_x) = I_{CBO}(T_0) * \exp(K * (T_x - T_0))$$

$T_0$ : Reference temperature (K)

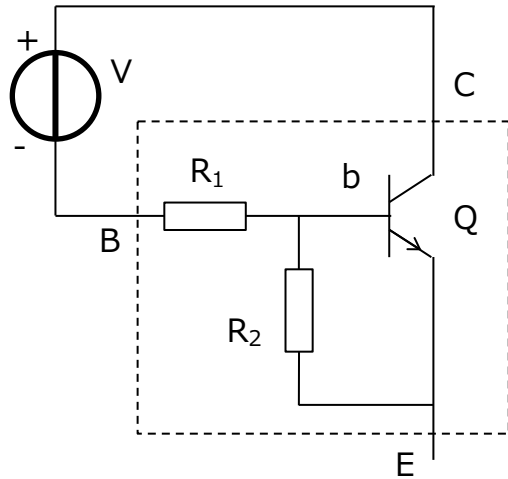
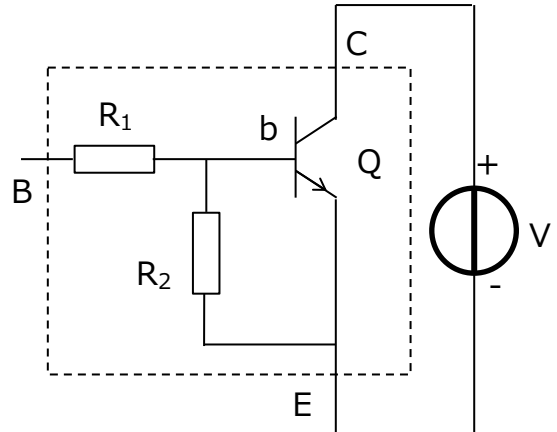
$T_x$ : Temperature at which  $I_{CBO}$  is to be calculated (K)

K: Temperature coefficient, which is generally 0.07/°C to 0.08/°C for silicon transistors

As described in Section 3.3,  $V_{CEO}$  is related to  $I_{CBO}$ , which increases as temperature increases, as indicated by the above equation. Care should be exercised in the use of BRTs particularly when the collector-emitter voltage in the off state is close to the maximum rated  $V_{CEO}$  value and the ambient temperature is high.

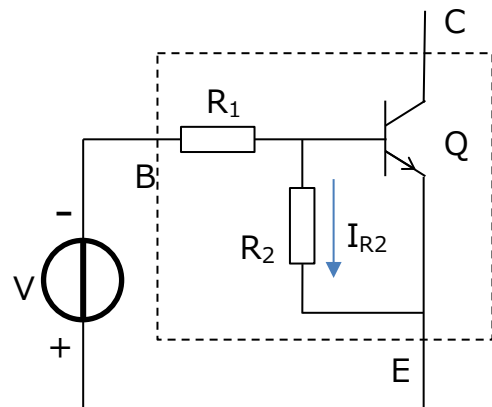
#### 4.1.2. Collector cut-off current ( $I_{CEO}$ )

Voltage is applied across the collector (C) and emitter (E) terminals with the base (B) terminal open-circuited as shown in Figure 4-2. The pn junction between the collector (C) and base (b) is reverse-biased whereas the pn junction between the base (b) and emitter (E) is forward-biased. As described in Section 3.3, "Collector-emitter voltage ( $V_{CEO}$ )," the leakage current flowing between C and b is amplified, producing collector cut-off current ( $I_{CEO}$ ).

**Figure 4-1  $I_{CBO}$** **Figure 4-2  $I_{CEO}$**

**4.2. Emitter cut-off current ( $I_{EBO}$ )**

Emitter cut-off current ( $I_{EBO}$ ) is the leakage current that flows when the pn junction between the base (b) and emitter (E) is reverse-biased with the collector (C) terminal open-circuited. A BRT incorporates resistors  $R_1$  and  $R_2$ . For example, in the case of an NPN BRT, the emitter-base voltage divided by  $R_1 / (R_1 + R_2)$  is applied across E and b in the low-voltage region, as described in Section 3.4, "Emitter-base voltage ( $V_{EBO}$ ).” As this voltage approaches the breakdown voltage of the pn junction between b and E, leakage current begins to flow. BRTs with a higher resistor ratio ( $R_1/R_2$ ) cause higher leakage current. At the same time,  $I_{R2}$  flows through  $R_2$ . BRTs with an equal resistor ratio cause lower leakage current if they contain  $R_1$  with a higher value.



**Figure 4-3  $I_{EBO}$**

**4.3. DC forward current gain ( $h_{FE}$ )**

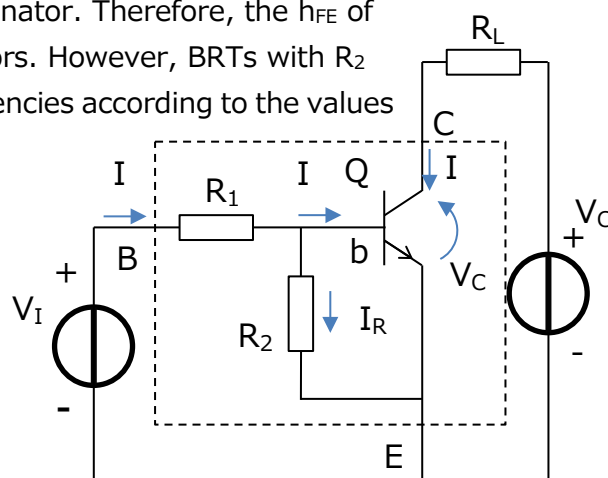
The DC forward current gain ( $h_{FE}$ ) is defined as follows:

$$h_{FE} = I_C / I_B = I_C / (I_b + I_{R2})$$

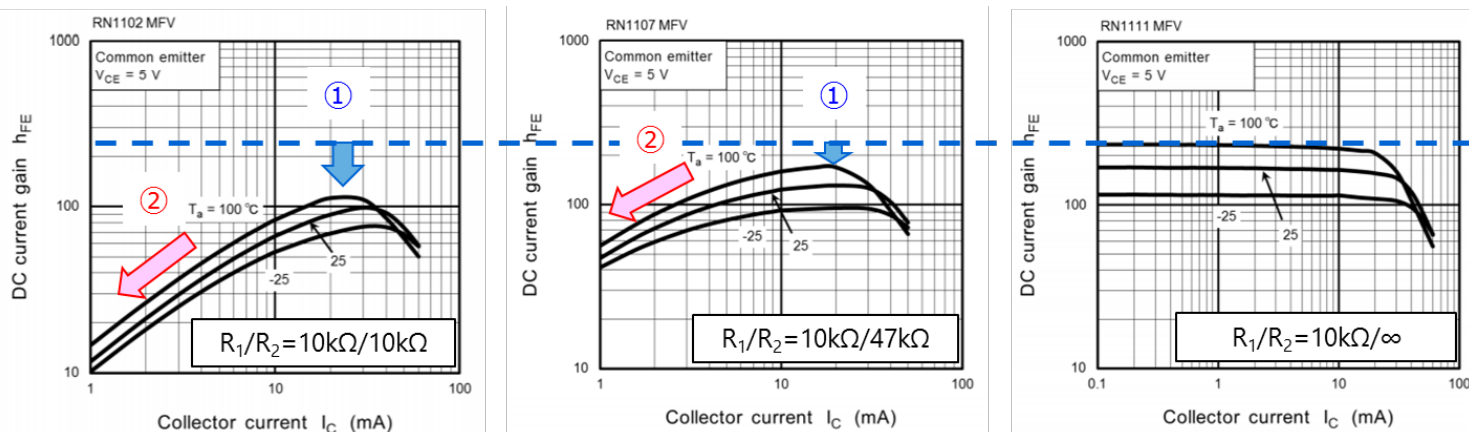
Unlike typical bipolar transistors, the  $h_{FE}$  equation of a BRT has a term of  $I_{R2}$  (i.e., current flowing through internal resistor  $R_2$ ) in the denominator. Therefore, the  $h_{FE}$  of BRTs without  $R_2$  is equal to that of typical bipolar transistors. However, BRTs with  $R_2$  provide lower  $h_{FE}$  because of  $I_{R2}$ .  $h_{FE}$  has the following tendencies according to the values of the internal resistors:

1. BRTs with higher  $R_2$  provide higher  $h_{FE}$ .
2. BRTs with low  $R_2$  exhibit a considerable decrease in  $h_{FE}$  in the low-current region.

When the internal transistor is on,  $V_{be} \approx 0.7$  V. Therefore,  $I_{R2}$  is almost constant. Therefore, BRTs with large  $I_{R2}$  (i.e., low  $R_2$ ) exhibit a decrease in  $h_{FE}$  in the low-current region because it is greatly affected by  $I_{R2}$ .



**Figure 4-4  $h_{FE}$**



**Figure 4-5 Relationships between  $h_{FE}$  and  $R_2$**

### 4.4. Collector-emitter saturation voltage ( $V_{CE(sat)}$ ), output voltage ( $V_{O(on)}$ )

The collector-emitter saturation voltage ( $V_{CE(sat)}$ ) is defined as a voltage drop across the collector (C) and emitter (E) terminals that occurs when  $I_B$  is applied to the base (B) terminal and  $I_C$  is applied to the collector (C) terminal, as shown in Figure 4-6.

This method is employed to obtain uniform measurement results. For example, under the condition  $I_C = 20 \times I_B$ ,  $V_{CE(sat)}$  equals the collector-emitter voltage in the saturation state when  $h_{FE} = 20$ .

For some BRTs, this voltage is specified as output voltage ( $V_{O(on)}$ ). In this case, replace  $I_B$  with  $I_I$  and  $I_C$  with  $I_O$  in the above paragraph.

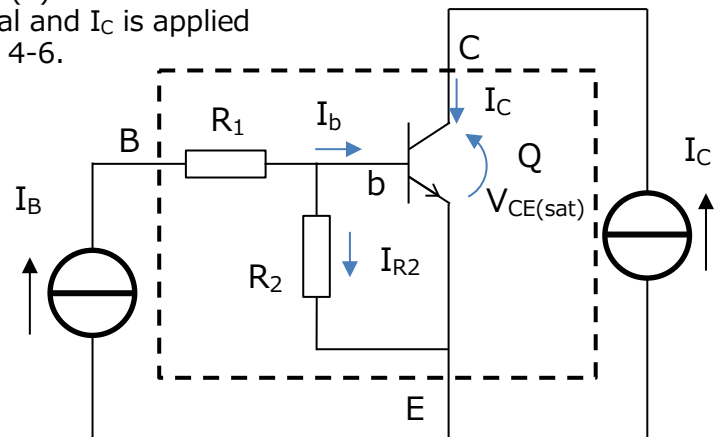


Figure 4-6  $V_{CE(sat)}$

### 4.5. Input voltage (ON) ( $V_{I(ON)}$ , $V_{I(on)}$ )

The input voltage required to turn on the internal transistor of a BRT in the saturation region is specified as  $V_{I(ON)}$  or  $V_{I(on)}$  (see Figure 4-7).

- $V_{I(ON)}$ : In the case of the RNxxxx series,  $V_{I(ON)}$  is defined as the input voltage (i.e., base-emitter (B-E) voltage) that provides the specified collector current ( $I_C$ ) and collector-emitter voltage ( $V_{CE}$ ).
- $V_{I(on)}$ : In the case of the TDTCxxx and TDTAxxx series,  $V_{I(on)}$  is defined as the input voltage (i.e., base-emitter (B-E) voltage) at which a BRT turns on at the specified output current ( $I_O$ ) and collector-emitter (C-E) voltage ( $V_O$ ).

Set the input voltage as follows to ensure that a BRT turns on in the saturation region under the test conditions shown in the datasheet:

- When  $V_{I(ON)}$  is specified, apply a voltage higher than the maximum  $V_{I(ON)}$  value.
- When  $V_{I(on)}$  is specified, apply a voltage higher than the minimum  $V_{I(on)}$  value.

When the internal transistor is on under the test conditions, the  $V_{I(ON)}$  and  $V_{I(on)}$  of BRTs are affected by the internal resistors.

All BRTs provide equal input current for the internal transistor and equal voltage at each terminal under the specified test conditions.

However,  $I_{R2}$  ( $= V_{bE} / R_2$ ) and therefore  $I_B$  ( $= I_b + I_{R2}$ ) differ from BRT to BRT.

$$V_{I(ON)} = \underline{V_{bE}} + R_1 \times (I_b + I_{R2}) = \underline{V_{bE}} + R_1 \times \underline{I_b} + R_1 \times \underline{V_{bE}} / R_2$$

The underscored parameters are equal for all BRTs. Therefore,  $V_{I(on)}$  is proportional to  $R_1$  and inversely proportional to  $R_2$ .

These relationships also apply to  $V_{I(on)}$ .

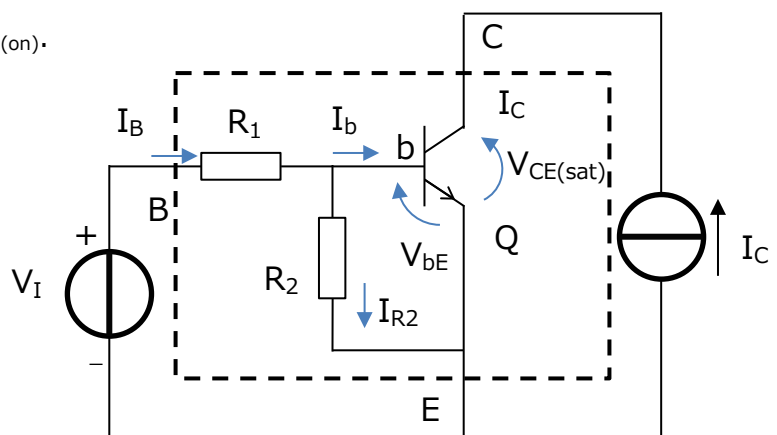


Figure 4-7  $V_{I(ON)}$

### 4.6. Input voltage (OFF) ( $V_{I(OFF)}$ , $V_{I(off)}$ )

$V_{I(OFF)}$  and  $V_{I(off)}$  are the input voltages required to turn off a BRT.

- $V_{I(OFF)}$ : In the case of the RNxxxx series,  $V_{I(OFF)}$  is defined as the input voltage (i.e., base-emitter (B-E) voltage) that provides the specified collector current ( $I_C$ ) and collector-emitter voltage ( $V_{CE}$ ).
- $V_{I(off)}$ : In the case of the TDTcxxx and TDTAxxx series,  $V_{I(off)}$  is defined as the input voltage (i.e., base-emitter (B-E) voltage) at which a BRT turns off at the specified output current ( $I_O$ ) and collector-emitter (C-E) voltage ( $V_O$ ).

Set the input voltage as follows to ensure that a BRT turns off under the test conditions shown in the datasheet:

- When  $V_{I(OFF)}$  is specified, apply a voltage lower than the minimum  $V_{I(OFF)}$  value.
- When  $V_{I(off)}$  is specified, apply a voltage lower than the maximum  $V_{I(off)}$  value.

$V_{I(OFF)}$  and  $V_{I(off)}$  are also affected by the internal resistors of BRTs.

In Figure 4-8, the internal transistor is off. The base-emitter voltage ( $V_{bE}$ ) at which the internal transistor turns off is determined by its threshold, irrespective of the internal resistors. Because the base current ( $I_b$ ) does not flow to the internal transistor in the off state,  $V_{I(OFF)}$  is expressed as follows. Since  $V_{bE}$  is a fixed value intrinsic to the internal transistor lower than its threshold,  $V_{I(OFF)}$  is proportional to the resistor ratio ( $R_1/R_2$ ).

$$V_{bE} = R_2 / (R_1 + R_2) \times V_{I(OFF)}$$

$$V_{I(OFF)} = (R_1 / R_2 + 1) \times V_{bE}$$

These relationships also apply to  $V_{I(off)}$ .

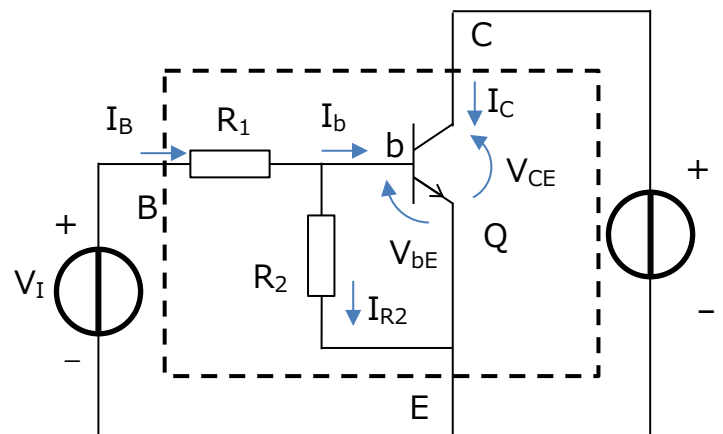


Figure 4-8  $V_{I(OFF)}$

### 4.7. Collector output capacitance ( $C_{ob}$ )

A transistor consists of two pn junctions: a base-emitter junction ( $C_{BE}$ ) and a collector-base junction ( $C_{CB}$ ). These pn junctions have parasitic capacitances (junction capacitances). In addition, discrete transistors such as BRTs, which have the collector region on the backside of a chip, have collector-emitter capacitance ( $C_{CE}$ ).

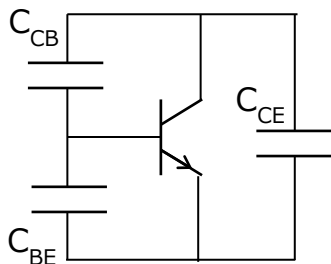
Collector output capacitance ( $C_{ob}$ ) is measured by applying  $V_C$  across the collector (C) and base (B) terminals with the emitter (E) terminal open-circuited as shown in the test circuit of Figure 4-10.

Therefore,  $C_{ob}$  can be expressed as:

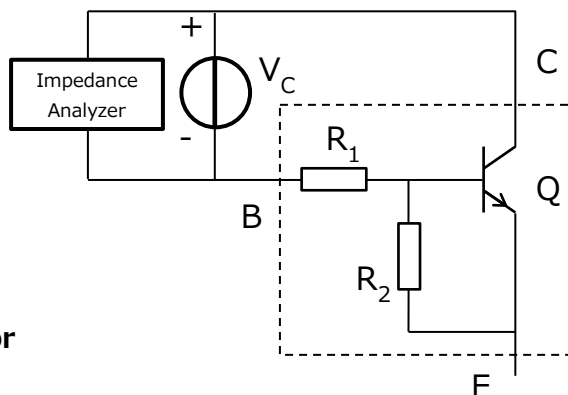
$$C_{ob} = C_{CB} + (C_{BE} \times C_{CE}) / (C_{BE} + C_{CE})$$

In the case of BRTs,  $C_{CE}$  is smaller than other capacitances. Hence,  $C_{ob}$  is almost equal to  $C_{CB}$ .

When a typical bipolar transistor operates in the linear region,  $C_{CB}$  acts as Miller capacitance, reducing a current gain. However, this hardly ever occurs in BRTs that are mainly used in the saturation region as switches.



**Figure 4-9 Capacitances in a transistor**

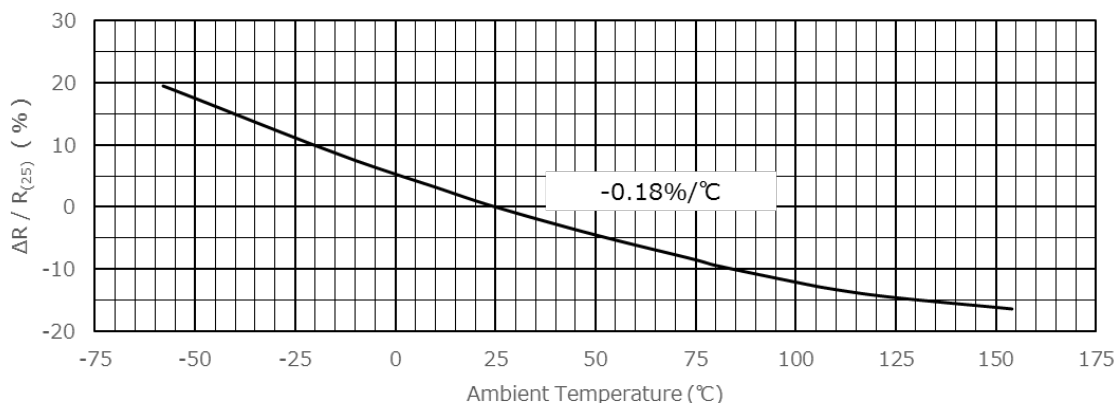


**Figure 4-10 Circuit for measuring collector output capacitance ( $C_{ob}$ )**

**4.8. Internal resistors**

The internal resistors of BRTs are polysilicon resistors whose power dissipation is specified to be 1/8 W. In most cases, the input voltage ( $V_i$ ) applied across the base (B) and emitter (E) terminals is constrained by the collector current ( $I_C$ ) and collector power dissipation ( $P_C$ ). However, in the case of applications in which BRTs go into deep saturation with low  $h_{FE}$ ,  $V_i$  might be constrained by the power dissipation of the internal resistors.

The values of the internal resistors are dependent on temperature. Figure 4-11 shows an example of their temperature characteristics curve.



**Figure 4-11 Example of temperature dependence of internal resistor values (baseline: 25°C)**

**4.9. Series base resistor ( $R_1$ )**

$R_1$  is defined as the value of the resistor connected in series between the base terminal (B) of a BRT and the base (b) of the internal transistor in it. This resistor is a polysilicon resistor. Its value decreases with temperature as shown in Section 4.8, “Internal resistors.” There is ±30% variation in  $R_1$  from the typical value shown in the datasheet. This variation is caused by the variations in the resistor width and dopant concentration in polysilicon as well as temperature.



$R_1$  converts the voltage applied to the base (B) terminal of a BRT into current. A bipolar transistor is a current-driven device. It is difficult to control a bipolar transistor with voltage because the collector current varies substantially when it is driven directly with voltage.  $R_1$  in a BRT makes it relatively easier to control the collector current.

When a BRT is on, the internal transistor operates in the saturation region where  $h_{FE} (=I_C/I_b)$  is in the range of 10 to 20, depending on the input voltage. Therefore, the base current ( $I_B$ ) that flows through  $R_1$  is relatively large—on the order of several milliamperes. Since the allowable power dissipation of  $R_1$  is 1/8 W, the maximum input voltage ( $V_I$ ) of BRTs with a high  $R_1$  value is determined by the value of  $R_1$ .

### 4.10. Resistor ratio ( $R_1/R_2$ )

The value of  $R_2$  is not specified on its own. Instead, the resistor ratio ( $R_1/R_2$ ) is specified. There is  $\pm 10\%$  variation in  $R_1/R_2$  from the typical value.

The input voltage (ON) specification ( $V_{I(ON)}$ ) is dependent on  $R_1/R_2$ . Since the base current ( $I_B$ ) does not flow immediately before the transistor turns on, the voltage applied to the B terminal ( $V_I$ ) is divided by  $R_1$  and  $R_2$ . Let the turn-on threshold voltage of the internal transistor be  $V_{bE}$ . Then,  $V_{bE}$  can be expressed as:

$$V_{bE} = R_2 / (R_1 + R_2) * V_{I(ON)}$$

The  $V_{bE}$  of BRTs is not affected by the values of  $R_1$  and  $R_2$  if they contain the same transistor:

$$V_{I(ON)} = V_{bE} * (R_1 + R_2) / R_2 = V_{bE} * (1 + R_1 / R_2)$$

Hence,  $V_{I(ON)}$  is dependent on the resistor ratio ( $R_1/R_2$ ).

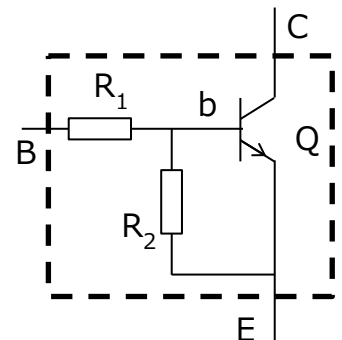
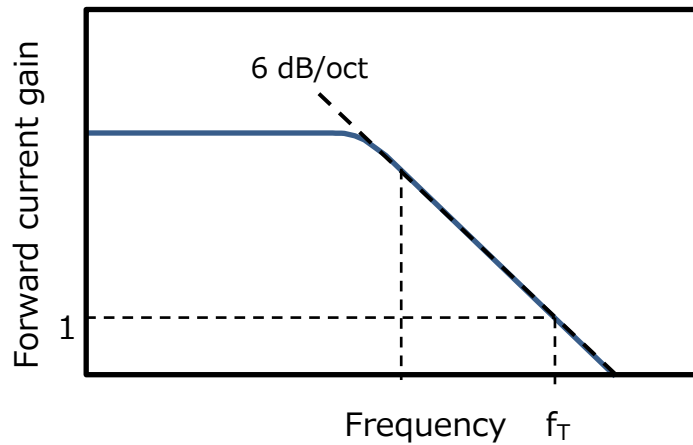


Figure 4-12 BRT equivalent circuit

### 4.11. Transition frequency ( $f_T$ )

The transition frequency ( $f_T$ ) is defined as the frequency at which the internal transistor provides a DC forward current gain ( $h_{FE}$ ) of 1. In the linear region,  $h_{FE}$  decreases at a rate of 6 dB per octave. Therefore,  $h_{FE}$  is measured at a low frequency (e.g., at 1 MHz) first, and then a straight line is drawn with a negative slope of 6 dB/octave.  $f_T$  is defined as a frequency at which  $h_{FE}$  becomes 1 on this line.

**Figure 4-13  $h_{FE}$  vs. frequency**

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