TPD7107F
Application note

Overview

The TPD7107F is an N-channel MOSFET gate driver IC for 1-channel output high-side switches. A high-current high-side switch can be easily configured by combining this product with an N-channel MOSFET with a 40V breakdown voltage. The boosting method for driving the N-channel MOSFET uses a charge pump circuit, so it can be used with 100% duty cycle. In addition, the IC has a built-in capacitor for the charge pump so that peripheral components can be reduced. Protecting and monitoring the MOSFET enables the building of highly secure systems.

Table of Contents

List of Figures

List of Tables

1. Compare products (TPD7107F, TPD7106F, TPD7104AF)

The following table shows the main differences between our 1-channel high-side N-channel MOSFET gate driver ICs. The features of our product lineup include highly safe protective functions such as reverse power connection protection and GND disconnection protection. Also, for how to control the external MOSFET during these protective operations, select the optimum products according to the necessity of the functions from the table below.

Table 1.1 Product comparison

Item	TPD7107F	TPD7106F	TPD7104AF
Wafer process	BiCD0.13	BiCD0.13	BiCD0.13
Power Supply Voltage (DC)	26 V	27 V	24 V
Power Supply Voltage (Pulse)	36 V(t≤400ms)	40 V(t≤500ms)	40 V(t≤300ms)
Output source current	100 μA	10 mA	100 μA
Output sink current	5 mA / 230mA (Note2)	0.4 A	5 mA
Reverse Battery protection method (Note1)	MOSFET ON	MOSFET OFF	MOSFET OFF
GND open protection.	✓	-	-
Package.	WSON10A	SSOP16	PS-8

Note1: Difference in external MOSFET operation when the power is reversed.

MOSFET ON: To reduce losses, the MOSFET is turned on and current flows.
MOSFET OFF: MOSFET and apply current to the MOSFET body diodes. To interrupt the current, connect an additional driver IC+ MOSFET so that the drain and drain are connected.

Note2: Refer to 4.2 Output Sink Current.

2. 1ch Output High Side Switch Outline

The high-side switch is a switch circuit in which a switching element such as a MOSFET is arranged on the power supply side, and an inductive load or a resistive load is connected to the GND side to adjust the current supplied to the load. This is a gate driver IC that drives the N-channel MOSFET that constitutes the high-side switch.
The high-side switches used in various applications are used in a wide current range of several hundred mA to several hundred A. In particular, a low on-resistance MOSFET is used for loads with large currents. We have a lineup of MOSFET that supports a variety of current ratings, so you can use this product in conjunction with them. It is also designed for automotive applications, so it has a variety of protection functions and a diagnostic function that provides feedback to the microcontroller. This guide mainly explains the basic characteristics, protection functions, and diagnostic functions, as well as their operation.

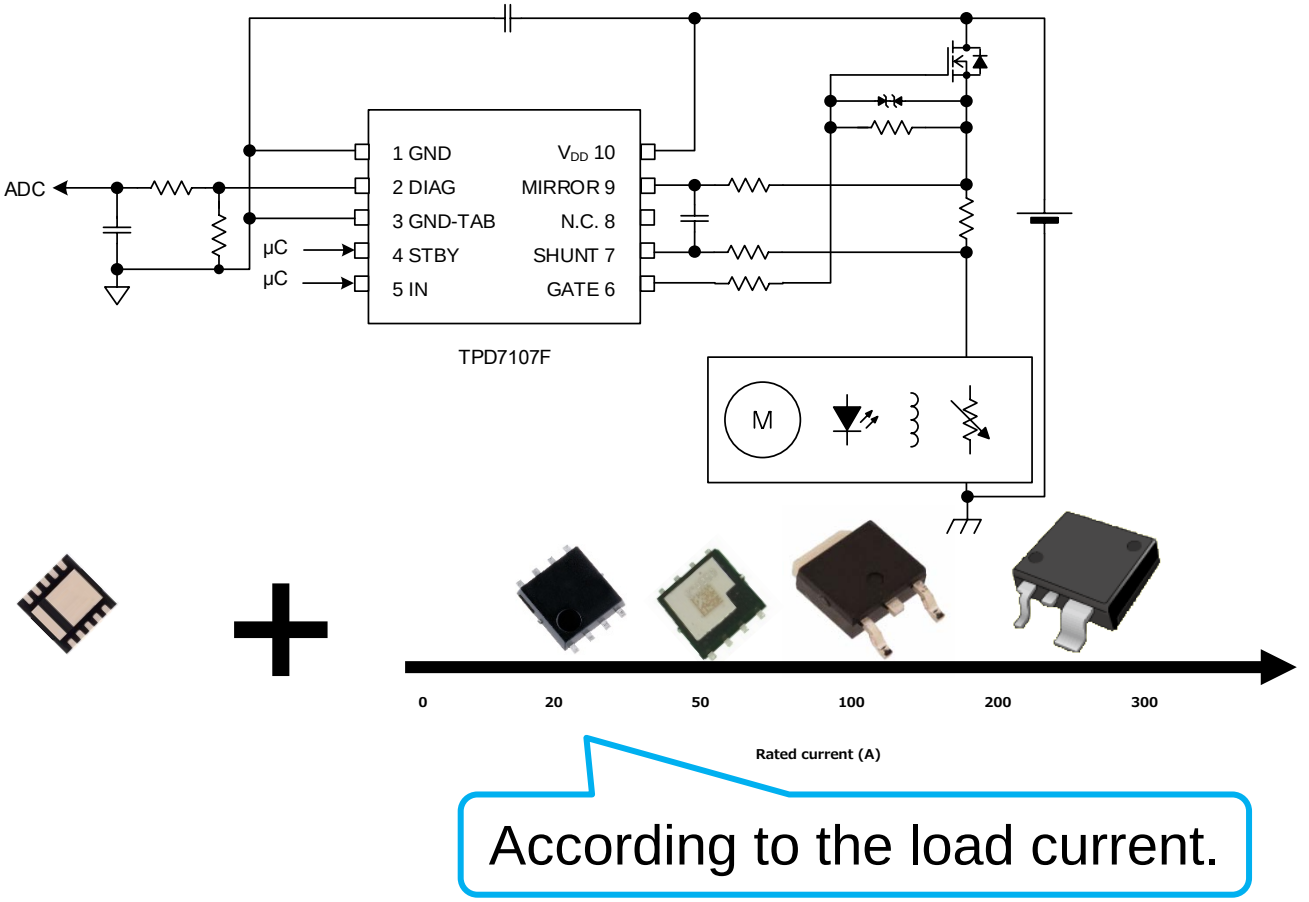


Figure 2.1 Schematic view of high-side switch

Table 2.1 List of recommended MOSFET

ID(A)	to 50A	to 100A	to 150A	to 200A	to 250A
Recommended device N-channel MOSFET 40V	TK50S04K3L XPN3R804NC TK35S04K3L	TK100S04N1L TK80S03K3L TK65S04N1L TK65S04K3L	TPWR7904PB TPHR7904PB TPW1R104PB TK1R4S04PB	TK200F04N1L TK1R4F04PB TK1R5R04PB	TKR74F04PB

3. Power supply voltage

3.1. Operation range of power supply voltage

Table 3.1 Operation range of power supply voltage

Item	Symbol	Operating ranges	Maximum Ratings	unit
Operating supply voltage	V_{DD}	5.75 to 26	40	V

The operating power supply voltage range is as shown in Table 3.1. However, to protect the external MOSFET and to protect this product from malfunction and damage, this product has a built-in protection function when the power supply voltage is abnormal.

3.2. Overvoltage protection

- When the voltage of a V_{DD} terminal is more than the over voltage detection threshold (V_{OV}), the off-driver usually operates and the external FET turns off. After that, if the V_{DD} terminal voltage is less than the over voltage threshold voltage, the external FET is driven again.
  - In the case of V_{IN}=H and V_{DD}>V_{OV}, the off-driver operates after the mask time of T_{OV} (200us max) (V_{GATE}=H to L).
  - In the case of V_{DD}>V_{OV} and V_{IN}=L to H, it keeps V_{GATE}=L.

3.3. Undervoltage protection

- When V_{DD} terminal voltage is less than V_{UV3} (2.7V (typ.)), the rapid off-driver operates, carry out latch-off of the external FET, and outputs H state to DIAG.
- In case V_{DD}<V_{UV5}, the off-driver operates and V_{DD} goes up. After that, if V_{DD} is more than V_{UV5}, the off-driver will change to normal operation (T_{DIAG}).
- Even if V_{DD} terminal voltage falls under the conditions of V_{GATE}=H, V_{GATE} keeps H state, and external FET will be ON in V_{DD}>V_{UV3}.(Low-voltage extension operation)
- There is a Latch clear standby time (T_{LATCH}) after returning to the normal operation from the low voltage.

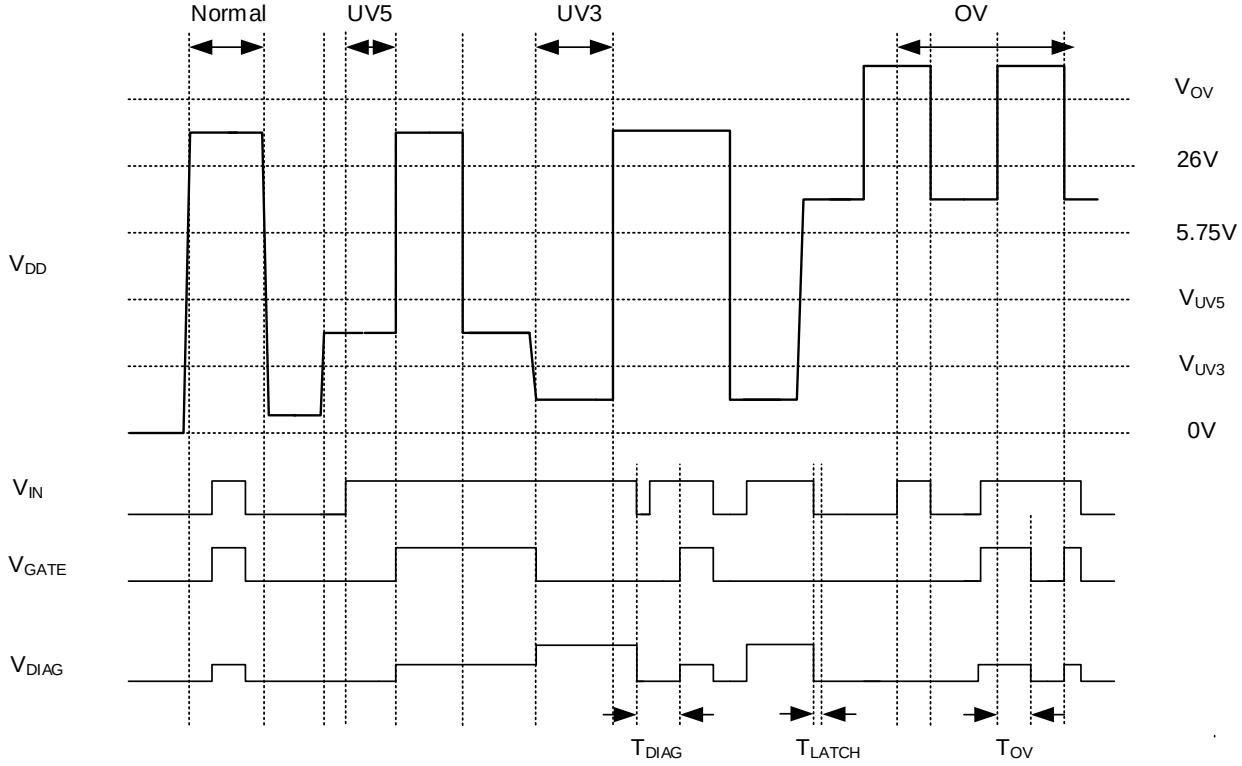


Figure 3.1 The abnormalities in power supply voltage.

3.4. The power activation method

After applying V_{DD} and reaching the predetermined voltage (5.75V) or higher, set the STBY pin to the High state. In addition, the IN pin should be in the low state at power-on. The control input sequence is shown below.

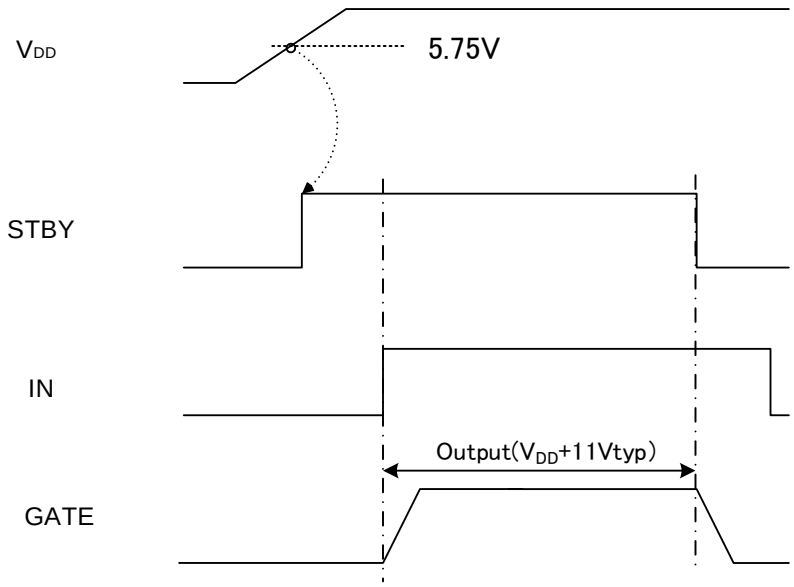


Figure 3.2 Control input sequence

4. Output current

4.1. Output source current

The source current output from the GATE pin is output from the internal charge pump circuit. Figure 4.1 shows the GATE pin voltage (red) at V_{DD}=5V and the gate-source voltage (blue) applied to the MOSFET. To ensure a gate-to-source voltage of 10V or greater, the source current must be limited to approximately 180μA or less. For ambient temperature and other design-margins, connect an external resistor of 100kΩ or more between MOSFET gate and source.

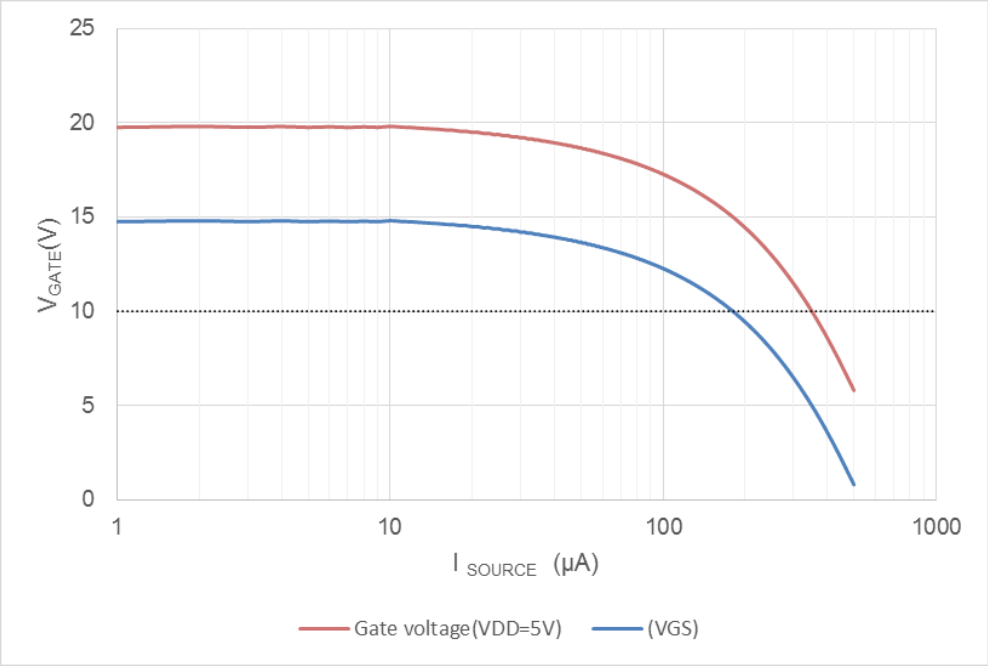


Figure 4.1 Gate voltage load regulation (V_{DD}=5V)

4.2. Output sink current

The output sink current of the GATE pin is 5mA at the absolute maximum rating. However, when an error is detected, the rapid off-driver operates and a sink current of 230mA (rapid off time 100μs) is generated and then the low state is maintained with a 5mA off-driver. Figure 4.2 shows the turn-off waveform at normal off and Figure 4.3 shows the turn-off waveform at rapid off. Excessive stress is applied to the MOSFET when overcurrent or short circuit occurs. In such an abnormal situation, the quick off driver operates to shut off the MOSFET in a short time, preventing the MOSFET from being destroyed.

Ch1: IN (5pin)
2.0V/div

Ch3: FET source
5.0V/div

Ch4: FET V_{GS}
5.0V/div (diff)

100µs/div

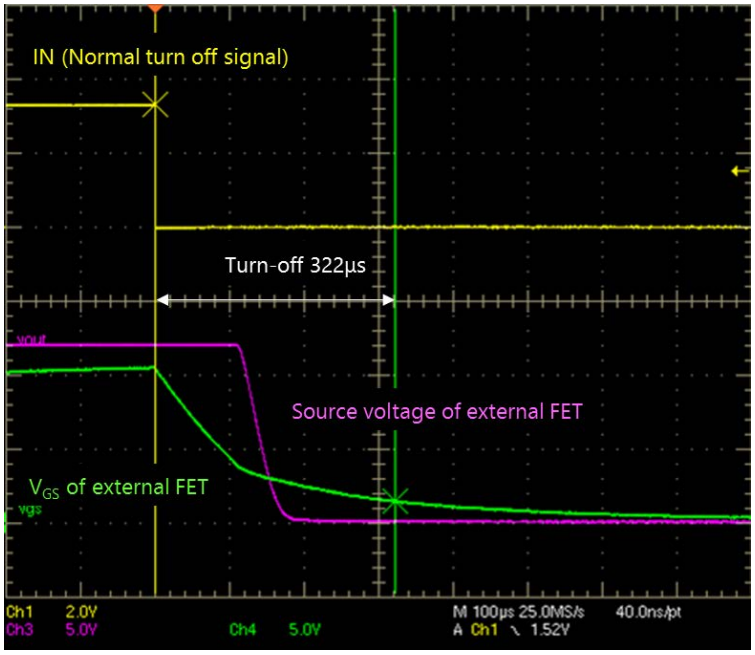


Figure 4.2 Gate voltage turn off waveforms at the time of normal operation
External MOSFET: TPWR7904PB

Ch1: Abnormal
Detection signal.
2.0V/div

Ch3: FET source
5.0V/div

Ch4: FET V_{GS}
5.0V/div (diff)

1µs/div

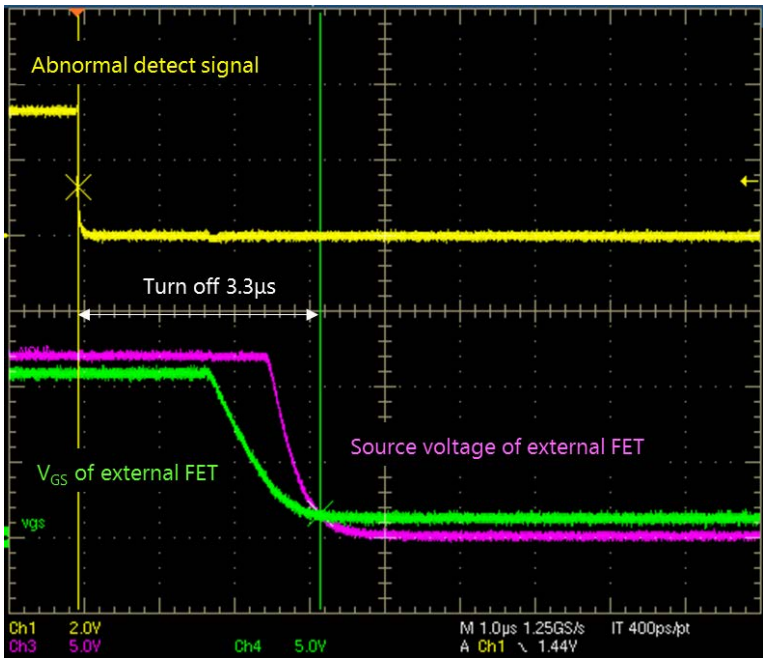


Figure 4.3 Gate voltage turn off waveforms at the time of abnormal operation
External MOSFET: TPWR7904PB

5. Control input

5.1. STBY terminal input

This terminal is used to control the product to the standby state. By setting to the Low state, the internal circuit is stopped and the mode transitions to low current consumption mode. The GATE pin and DIAG pin maintain the Low state. In the standby state, each protection function and the diagnostic output function are stopped. A pull-down resistor is incorporated, so it is in the standby state when it is open. By setting to the High state, the standby state is canceled.

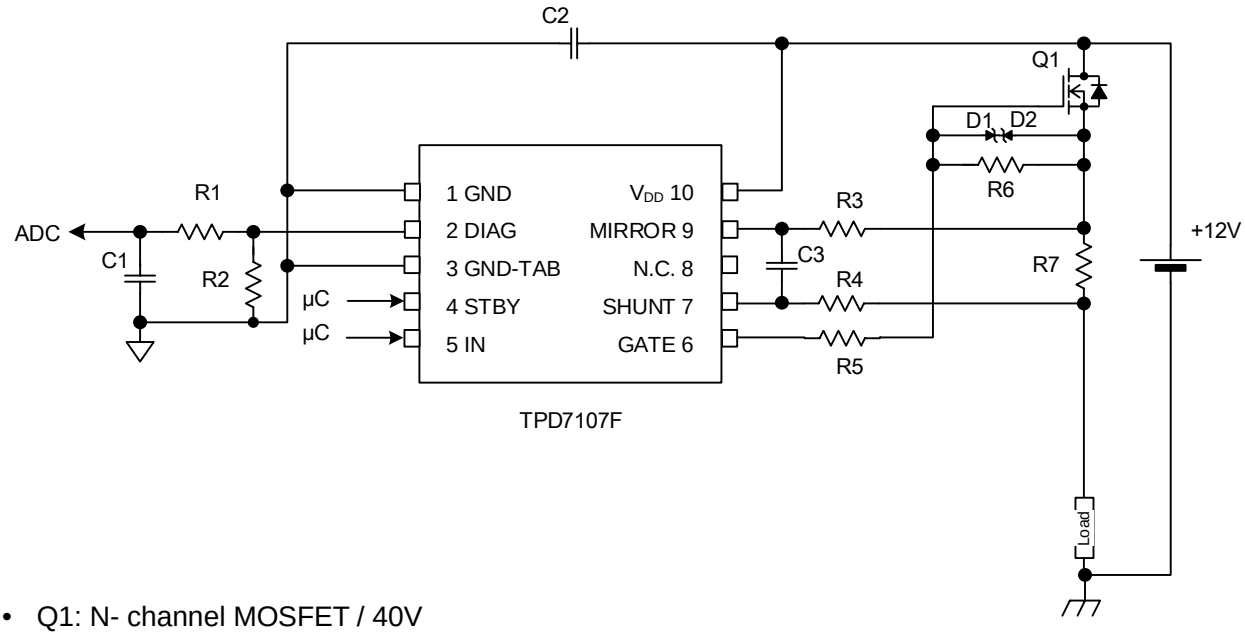
5.2. IN terminal input

By setting the IN pin to the High state, the GATE pin outputs a boosted voltage and applies a bias to the gate of the external MOSFET. In addition to the control to turn on/off the MOSFET, it is also used as a signal to reset the inside of the IC by setting the IN pin to the Low state after the protection function operates. Since a pull-down resistor is internally incorporated, the IN pin is in the Low state when it is open.

5.3. MIRROR・SHUNT terminal input

A differential amplifier for sensing the load current is built-in and its input terminal. Connect the MIRROR terminal to the source terminal of the external MOSFET. Connect the SHUNT terminal to the load-side of the outputs. Connect a shunt resistor between the MIRROR and SHUNT terminals.

6. The example of an application circuit



- Q1: N- channel MOSFET / 40V
- D1,D2: CRZ16
- R1: 47kΩ
- R2: 10kΩ
- R3,R4,R5: 100Ω
- R6: 200kΩ
- R7: 1mΩ/4W
- C1: 10nF/12V
- C2: 0.22µF/50V
- C3: 220pF/50V

Note1: Please connect the capacitor for power supplies near the IC as much as possible.

Figure 6.1 The example of an application circuit

Precautions for use

- For overvoltage protection between gate and source in Q1, connect the Zener diode in both directions (Zener voltage 16V). Connect a pull-down resistor R6, as Q1 may malfunction if the IC's GATE terminal becomes high-impedance due to a break in the circuit.
- For the shunt resistor R7 used for sensing the current, select the resistance value and power dissipation considering the maximum load current and loss. The V_{DIAG} of voltage output to the ADC can be calculated by the following equation.

$$V_{DIAG} = I_D \cdot R7 \cdot \left(\frac{R2}{R3}\right)$$

- Place capacitor C1 between V_{DD} and GND and capacitor C3 between MIRROR-SHUNT as close as possible to IC.

7. Protect function

7.1. Protection for reverse battery connection

Figure 7.1 shows the power supply reverse connection operation conditions. GND is connected to the V_{DD}, V_{DD} terminal on the load side, and evaluation is performed in the reverse connection state. The V_{GS} in Q1 was measured when V_{DD} was applied 0V to -26V. The V_{GS} rises linearly up to-16V, and the V_{GS} is about 15V when V_{DD} is around -18V, and the MOSFETQ1 is turned on sufficiently.

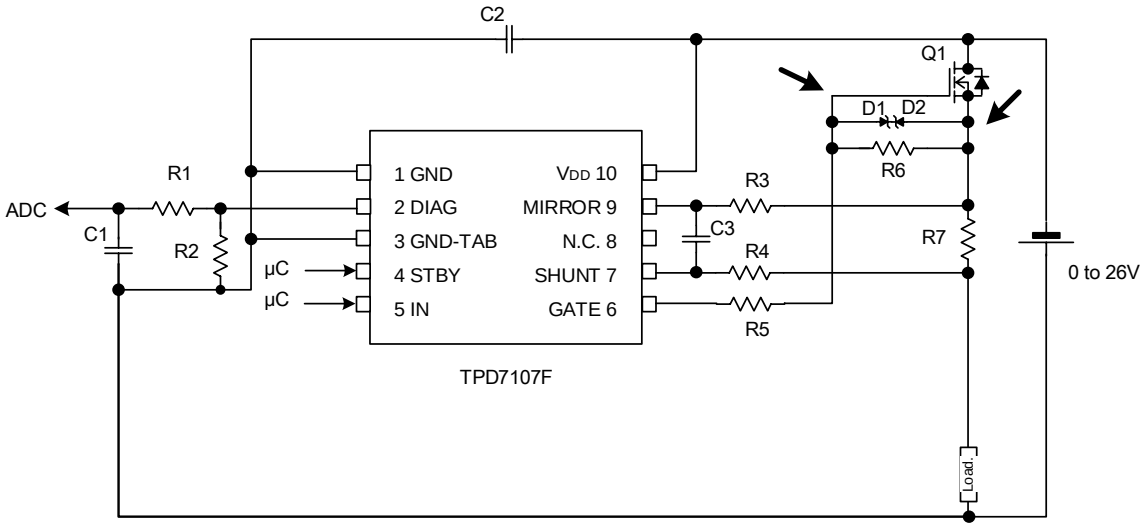


Figure 7.1 Reverse battery connection operating condition

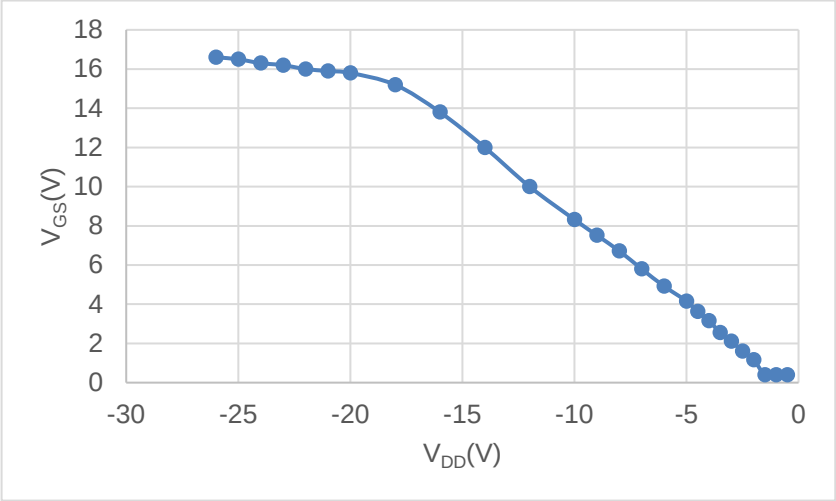


Figure 7.2 Reverse battery operation (V_{DD} vs Q1 V_{GS})

7.2. Active clamp operation

Figure 7.3 shows the active clamp check circuit conditions. Connect an inductive load of 50μH to the load and input control signals to IN (Pulse width = 300μs). Because of normal operation, analogue voltage is output to the DIAG. However, since only 50μH is connected, current increases and overcurrent protection operates. Then, the induced voltage by the inductive load of 50μH is generated, the V_{DS} of the external MOSFET rises, and it enters the active clamping operation at about 36. 4V.

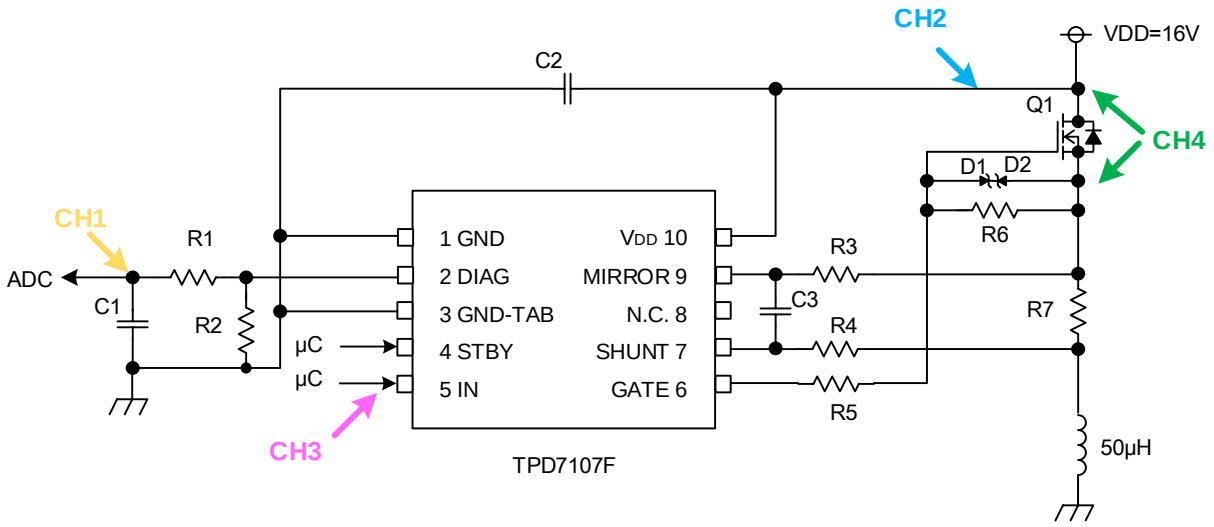


Figure 7.3 Active clamp operation

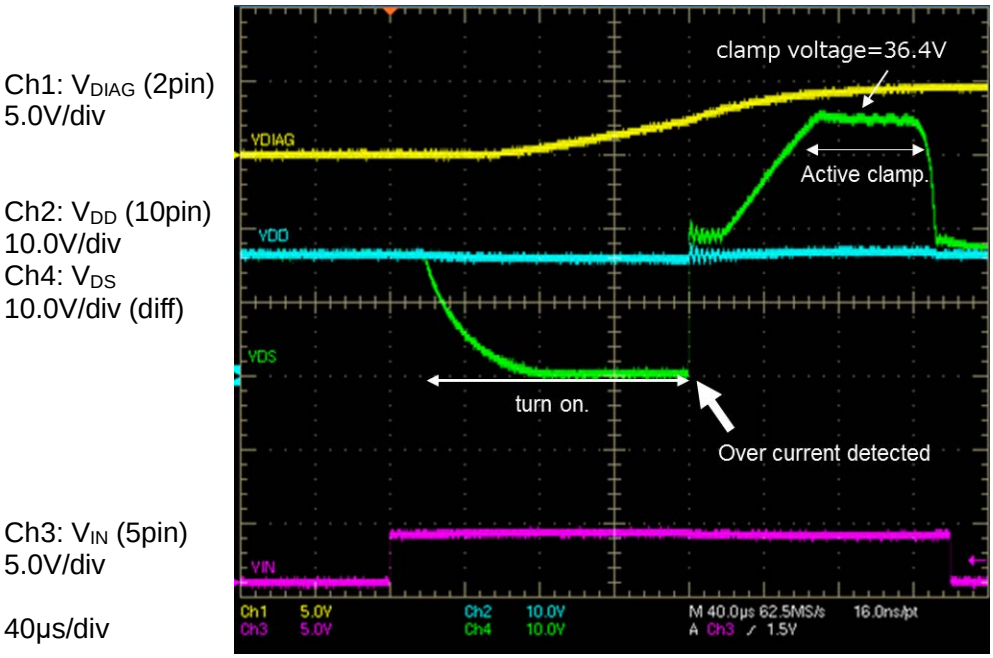


Figure 7.4 Active clamp operation (V_{DD}=16V, IN: pulse width = 300μs, L load = 50μH)

7.3. Load current sensing in normal operation

Fig. 7.5 shows the actual measured values assuming that the X-axis is the load current and the Y-axis is the analog voltage of the DIAG. In the low-current range below the 1A, the voltage across the shunt resistor is also small, so the sense amplifier input offset becomes dominant, causing a relative error. When the 1A is exceeded, it becomes 10% or less and approaches the theoretical values. The guaranteed input offset of the sense amplifier is ±2mV.

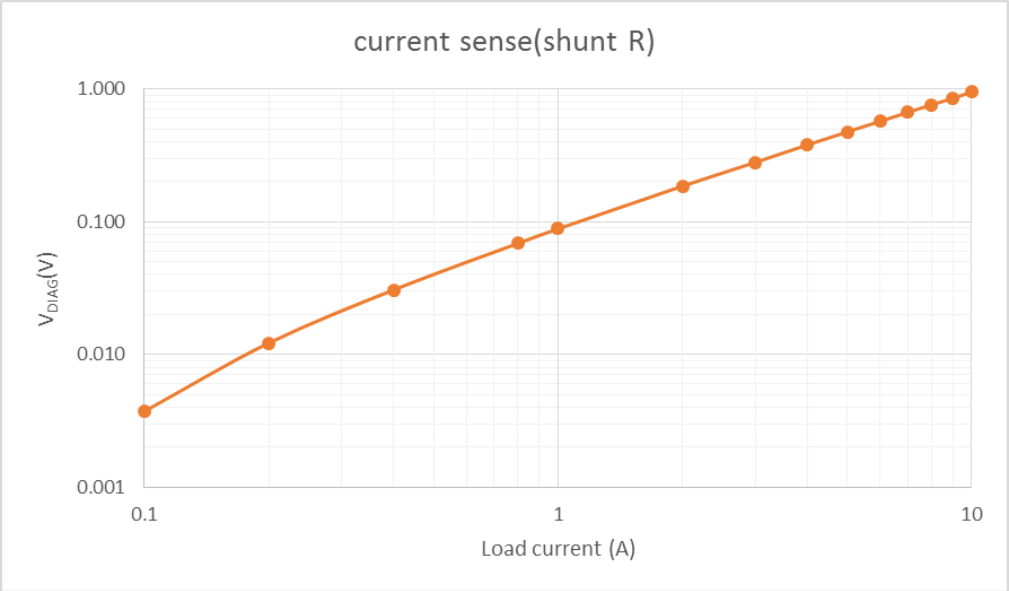


Figure 7.5 Current sense characteristic

7.4. Load opening detection

Figure 7.7 shows the output waveform when the load is disconnected (load open). The V_{DIAG} has an intermediate voltage of 2.75V and outputs the voltage at the time of detecting a load disconnection. When the IN terminal is set to L →, it shifts to the normal operation mode after 12.5ms (T_{DIAG}). When the IN terminal is set to → L, the load disconnection detecting mode is adopted again.

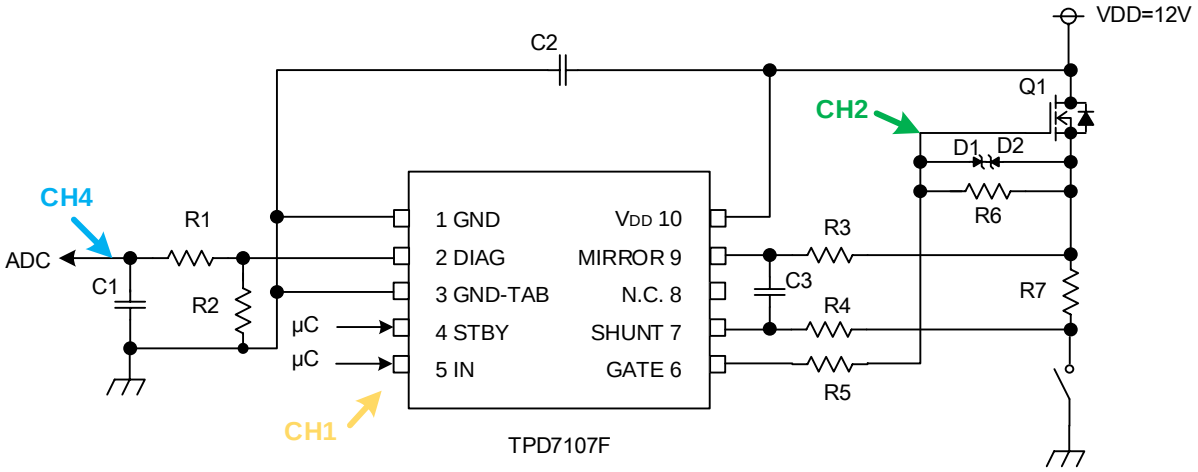


Figure 7.6 Load Disconnection Detection Evaluation Conditions

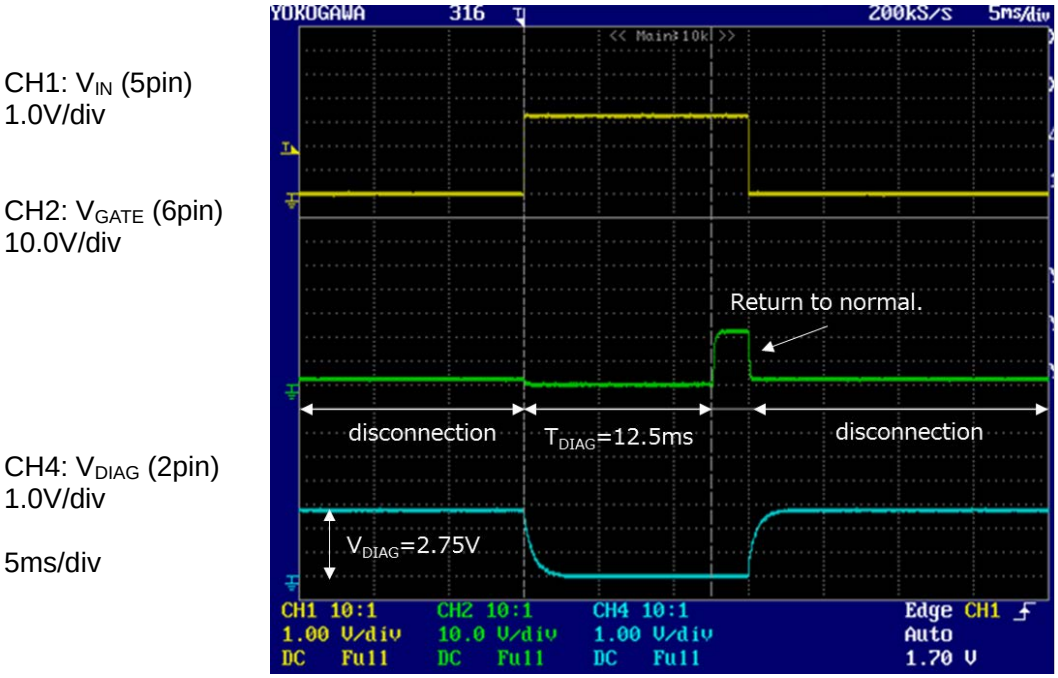


Figure 7.7 Load disconnection detected (V_{DD}=12V, IN=0 to 3.3V, Rload=open)

7.5. V_{DD} short detection

Figure 7.9 shows each output waveform at the time of a short to power fault. In the circuit diagram, the drain and source of Q1 are short-circuited to reproduce the short to power operation and check the diagnostic output at that time. When a load disconnection is detected, a voltage of 2.75V is output, but when the short to power is detected, a 5V is output to enable the microcontroller to recognize the short to power.

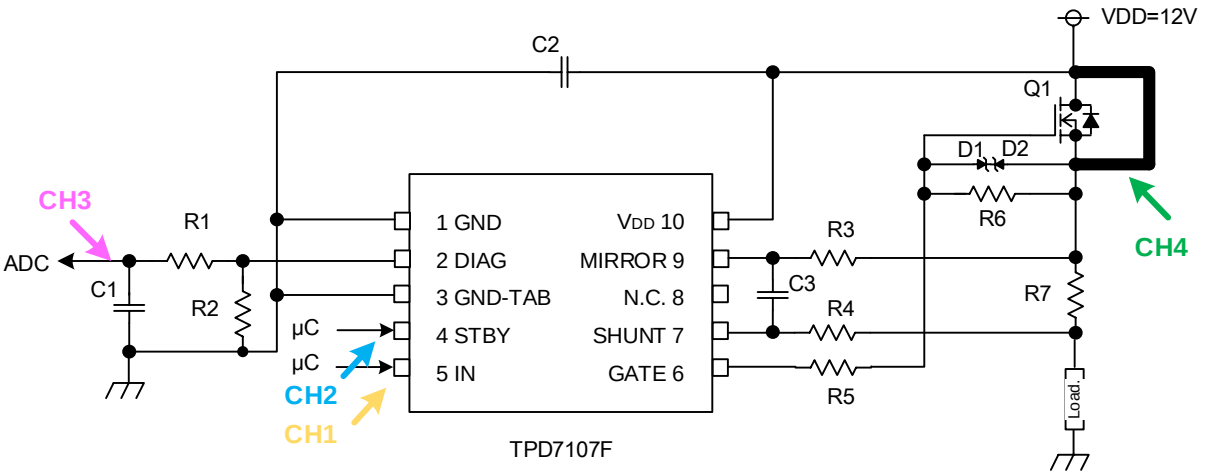


Figure 7.8 Measurement condition of V_{DD} short detection.

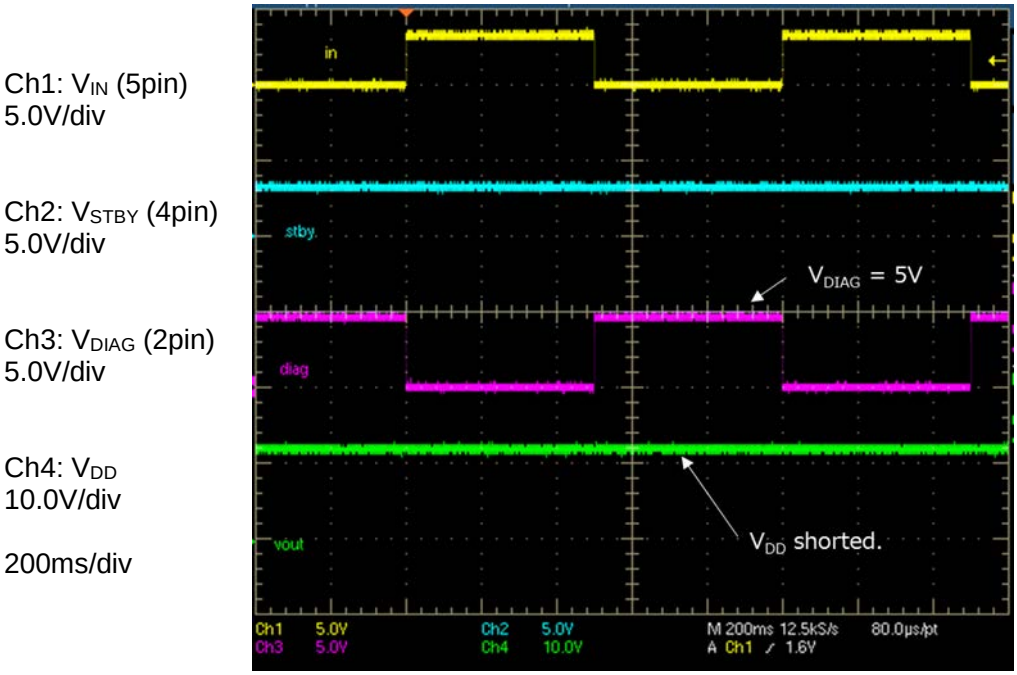


Figure 7.9 V_{DD} short detection(V_{DD}=12V, IN=0 to 3.3V, Q1 drain-source shorted).

7.6. GND disconnection detection

Figure 7.10 shows the measurement circuit. GND disconnection detection is a function that maintains off so that an external MOSFET does not operate when the GND line of this product is disconnected. When the GND on the IC side is opened, the GND terminal (it display on Ch2) of the IC floats and the voltage rises. The V_{GS} of external MOSFET is monitored with the differential probe and turns off (≈0V) at approximately 450μs. Since the V_{GS} has dropped below Vth, the external MOSFET turns off and cuts off the current to the GND.

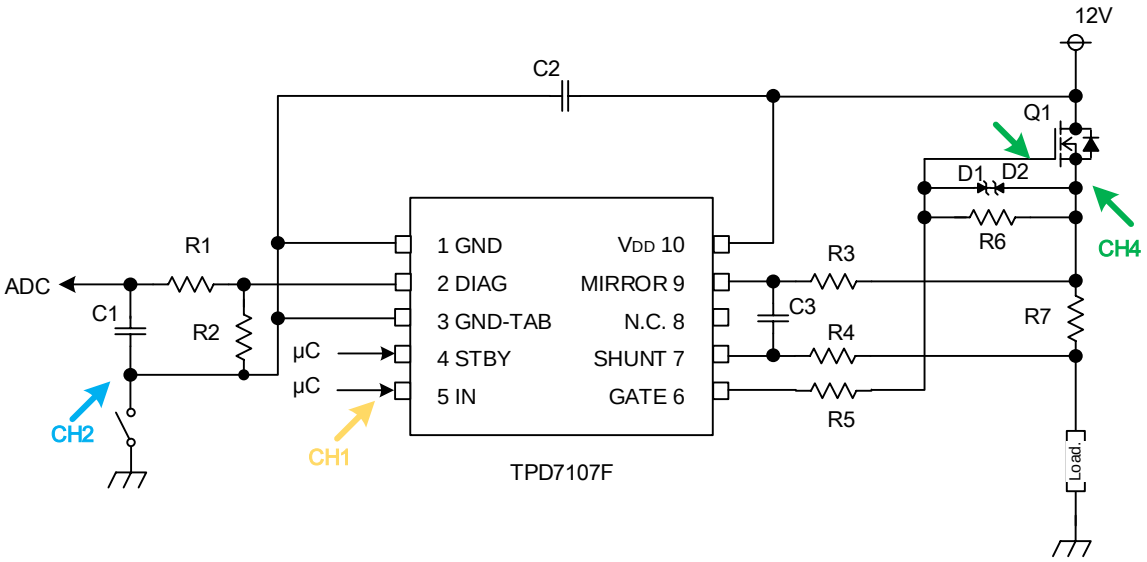


Figure 7.10 GND Disconnection Detection

Ch1: V_{IN} (5pin)
5.0V/div

Ch4: V_{GS}
5.0V/div (diff)

Ch2: GND
5.0V/div

100μs/div

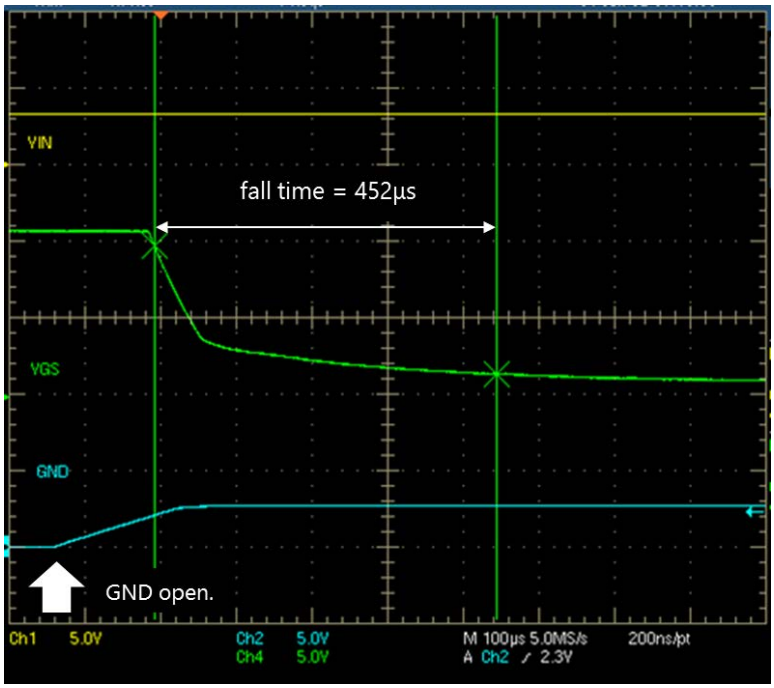


Figure 7.11 GND Disconnection Detected (V_{DD}=12V, IN=3.3V, with GND pin open asynchronously)

7.7. Abnormal external MOSFET drain-source voltage

When a gate bias is applied to an external MOSFET, but an abnormal potential occurs between the drain and source, an H-state is output from the diagnostic output to indicate an error. Figure 7.12 is an evaluation condition that deliberately reproduces the drain-source anomaly. A 220 Ω (R8) is deliberately inserted between the V_{DD} (12V) and the drain of Q1, and a 100 Ω load resistor is connected. This unit monitors the V_{DD}-SHUNT voltages. Figure 7.13 shows the evaluation results. When a pulse is input to the IN terminal and the turn-on operation is performed, a normal bias is applied to the V_{GS}. However, since 220 Ω is connected to the R8, the SHUNT terminal voltage is about 3.9V without an increase. The V_{DD}-SHUNT voltage is about 8.1V, and the IC detects an abnormal drain-source voltage. The detection time is about 13.5ms.

In the case where a drain-to-source voltage error and low-voltage detection (UV5) occur simultaneously, this device determines that a load is short-circuited, performs rapid OFF operation without waiting for the detection time, and outputs the H-state to the diagnostic output DIAG pin.

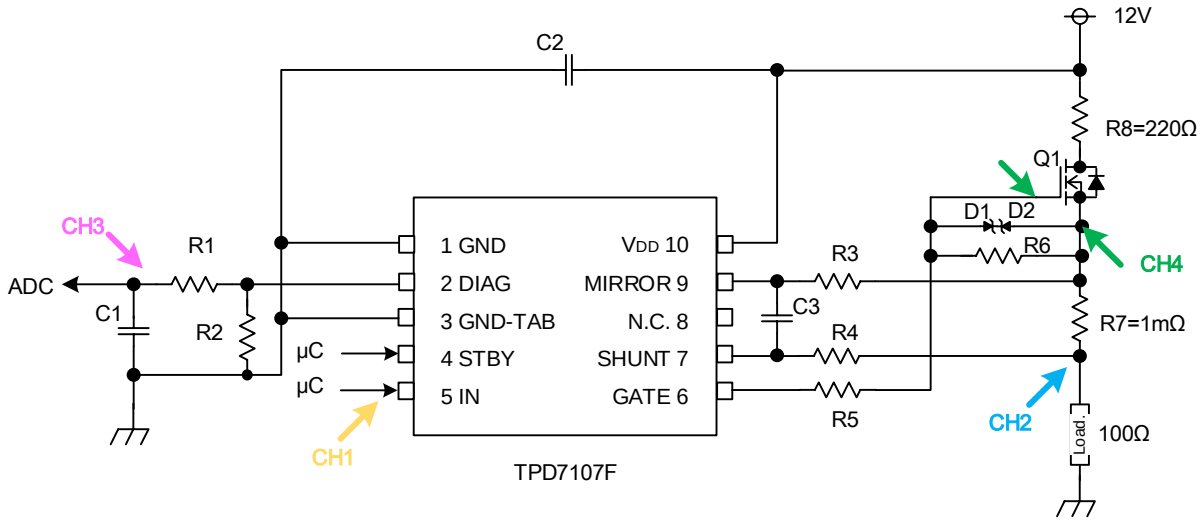


Figure 7.12 FET drain to source voltage abnormality

Ch1: V_{IN} (5pin)
5.0V/div

Ch2: V_{SHUNT} (7pin)
5.0V/div

Ch3: V_{DIAG} (2pin)
5.0V/div

Ch4: V_{GS}
10.0V/div

4.0ms/div

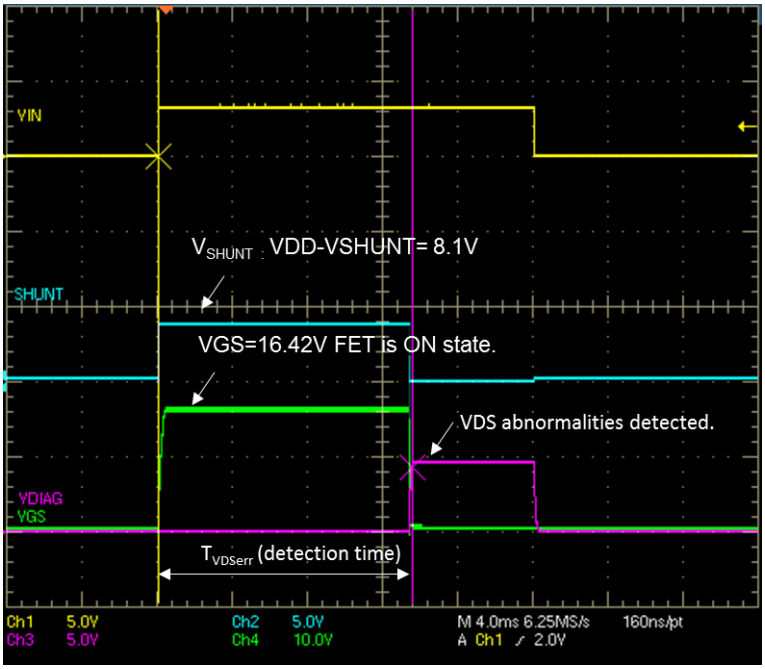


Figure 7.13 FET drain to source voltage abnormality

(V_{DD}=12V, IN=0 to 3.3V, pulse width 20ms, Rload = 100Ω, R8=220Ω)

8. Evaluation board

We prepare evaluation boards that mount MOSFET and other peripheral devices. You can check the function under actual load and the protection diagnosis function.

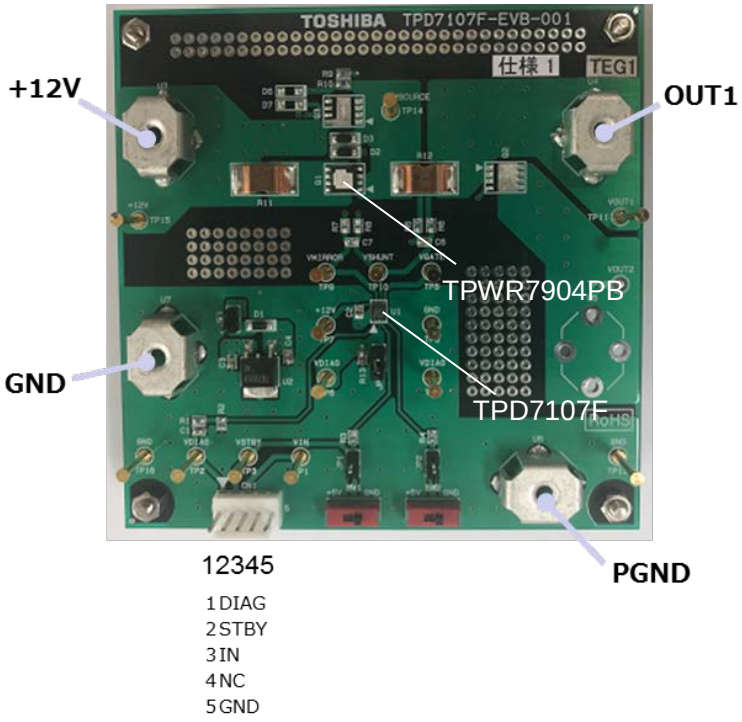
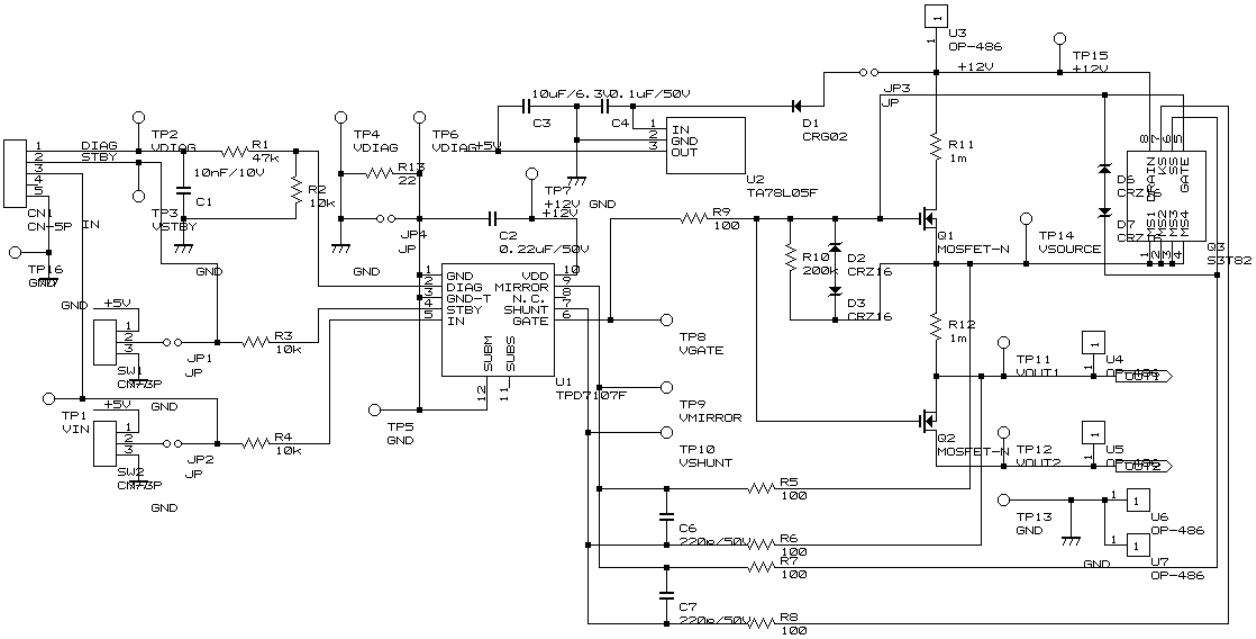


Figure 8.1 Evaluation board (TPD7107F)



Note1: Unimplemented parts: Q2,Q3,U5,TP12,D6,D7,C7,R7,R8

Figure 8.2 Evaluation board schematic.

9. Points to note in the description

1. Block diagram
   Functional blocks, circuits, constants, etc. in the block diagram may be partially omitted or simplified to explain the functions.

2. Equivalent circuit
   The equivalent circuit may be partially omitted or simplified to illustrate the circuit.

10. Points to Remember on Handling of ICs

10.1. Precautions for use

1. The absolute maximum rating is the standard which must exceed no one value of two or more rating even the instant. It cannot exceed to any of two or more rating. When the absolute maximum rating is exceeded, it may become the cause of destruction, damage, and degradation, and it may be injured by the burst and combustion.

2. Since current sensing voltages and more than diagnostic output voltage may be outputted to the DIAG output by the injection of the power supply, interception condition (rising and bringing down), the input condition (MIRROR, SHUNT) to current sense amplifier, etc., please confirm problem existence by the set in the case of use. Also, please give me the measure by the capacitor etc. if needed.

RESTRICTIONS ON PRODUCT USE

Toshiba Corporation and its subsidiaries and affiliates are collectively referred to as “TOSHIBA”.
Hardware, software and systems described in this document are collectively referred to as “Product”.

- TOSHIBA reserves the right to make changes to the information in this document and related Product without notice.
- This document and any information herein may not be reproduced without prior written permission from TOSHIBA. Even with TOSHIBA's written permission, reproduction is permissible only if reproduction is without alteration/omission.
- Though TOSHIBA works continually to improve Product's quality and reliability, Product can malfunction or fail. Customers are responsible for complying with safety standards and for providing adequate designs and safeguards for their hardware, software and systems which minimize risk and avoid situations in which a malfunction or failure of Product could cause loss of human life, bodily injury or damage to property, including data loss or corruption. Before customers use the Product, create designs including the Product, or incorporate the Product into their own applications, customers must also refer to and comply with (a) the latest versions of all relevant TOSHIBA information, including without limitation, this document, the specifications, the data sheets and application notes for Product and the precautions and conditions set forth in the "TOSHIBA Semiconductor Reliability Handbook" and (b) the instructions for the application with which the Product will be used with or for. Customers are solely responsible for all aspects of their own product design or applications, including but not limited to (a) determining the appropriateness of the use of this Product in such design or applications; (b) evaluating and determining the applicability of any information contained in this document, or in charts, diagrams, programs, algorithms, sample application circuits, or any other referenced documents; and (c) validating all operating parameters for such designs and applications. **TOSHIBA ASSUMES NO LIABILITY FOR CUSTOMERS' PRODUCT DESIGN OR APPLICATIONS.**
- **PRODUCT IS NEITHER INTENDED NOR WARRANTED FOR USE IN EQUIPMENTS OR SYSTEMS THAT REQUIRE EXTRAORDINARILY HIGH LEVELS OF QUALITY AND/OR RELIABILITY, AND/OR A MALFUNCTION OR FAILURE OF WHICH MAY CAUSE LOSS OF HUMAN LIFE, BODILY INJURY, SERIOUS PROPERTY DAMAGE AND/OR SERIOUS PUBLIC IMPACT ("UNINTENDED USE").** Except for specific applications as expressly stated in this document, Unintended Use includes, without limitation, equipment used in nuclear facilities, equipment used in the aerospace industry, lifesaving and/or life supporting medical equipment, equipment used for automobiles, trains, ships and other transportation, traffic signaling equipment, equipment used to control combustions or explosions, safety devices, elevators and escalators, and devices related to power plant. **IF YOU USE PRODUCT FOR UNINTENDED USE, TOSHIBA ASSUMES NO LIABILITY FOR PRODUCT.** For details, please contact your TOSHIBA sales representative or contact us via our website.
- Do not disassemble, analyze, reverse-engineer, alter, modify, translate or copy Product, whether in whole or in part.
- Product shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable laws or regulations.
- The information contained herein is presented only as guidance for Product use. No responsibility is assumed by TOSHIBA for any infringement of patents or any other intellectual property rights of third parties that may result from the use of Product. No license to any intellectual property right is granted by this document, whether express or implied, by estoppel or otherwise.
- **ABSENT A WRITTEN SIGNED AGREEMENT, EXCEPT AS PROVIDED IN THE RELEVANT TERMS AND CONDITIONS OF SALE FOR PRODUCT, AND TO THE MAXIMUM EXTENT ALLOWABLE BY LAW, TOSHIBA (1) ASSUMES NO LIABILITY WHATSOEVER, INCLUDING WITHOUT LIMITATION, INDIRECT, CONSEQUENTIAL, SPECIAL, OR INCIDENTAL DAMAGES OR LOSS, INCLUDING WITHOUT LIMITATION, LOSS OF PROFITS, LOSS OF OPPORTUNITIES, BUSINESS INTERRUPTION AND LOSS OF DATA, AND (2) DISCLAIMS ANY AND ALL EXPRESS OR IMPLIED WARRANTIES AND CONDITIONS RELATED TO SALE, USE OF PRODUCT, OR INFORMATION, INCLUDING WARRANTIES OR CONDITIONS OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, ACCURACY OF INFORMATION, OR NONINFRINGEMENT.**
- Do not use or otherwise make available Product or related software or technology for any military purposes, including without limitation, for the design, development, use, stockpiling or manufacturing of nuclear, chemical, or biological weapons or missile technology products (mass destruction weapons). Product and related software and technology may be controlled under the applicable export laws and regulations including, without limitation, the Japanese Foreign Exchange and Foreign Trade Law and the U.S. Export Administration Regulations. Export and re-export of Product or related software or technology are strictly prohibited except in compliance with all applicable export laws and regulations.
- Please contact your TOSHIBA sales representative for details as to environmental matters such as the RoHS compatibility of Product. Please use Product in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. **TOSHIBA ASSUMES NO LIABILITY FOR DAMAGES OR LOSSES OCCURRING AS A RESULT OF NONCOMPLIANCE WITH APPLICABLE LAWS AND REGULATIONS.**