TOSHIBA Photocoupler IRED + Photo IC

TLP351F

Inverter for Air Conditioner IGBT/Power MOS FET Gate Drive Industrial Inverter

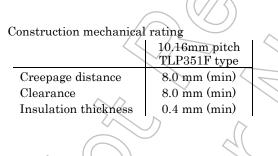
The TOSHIBA TLP351F consists of an infrared light emitting diode and a integrated photodetector.

This unit is 8-lead DIP package.

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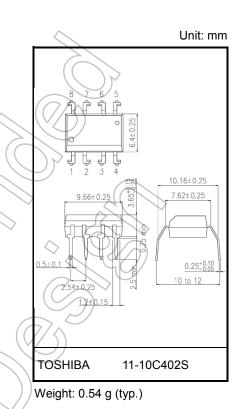
TLP35F1 is suitable for gate driving circuit of IGBT or power MOS FET. Especially TLP351F is capable of "direct" gate drive of lower Power IGBTs.

- Peak output current: ±0.6 A (max)
- Guaranteed performance over temperature: -40 to 100° C
- Supply current: 2 mA (max)
- Power supply voltage: 10 to 30 V
- Threshold input current : $I_F = 5 \text{ mA} (max)$
- Switching time (t_{pLH}/t_{pHL}): 700 ns (max)
- Common mode transient immunity: ±10 kV/µs
- Isolation voltage: 3750 Vrms
- UL-recognized: UL 1577, File No.E67349
- cUL-recognized: CSA Component Acceptance Service No.5A File No.E67349
- VDE-approved: EN 60747-5-5 (Note 1)
 - Note 1: When a VDE approved type is needed, please designate the **Option(D4)**.

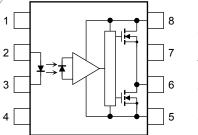


Truth Table

Input	LED	Tr1	Tr2	Output
Н	ON	ON	OFF	Н
L	OFF	OFF	ON	L

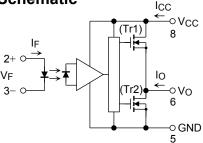


Pin Configuration (top view)



1: N.C. 2: Anode 3: Cathode 4: N.C. 5: GND 6: Vo (output) 7: N.C. 8: Vcc

Schematic



A 0.1 μF bypass capacitor must be connected between pin 8 and 5.

Start of commercial production 2002-05

Absolute Maximum Ratings (Ta = 25°C)

					-
	Characteristics	Symbol	Rating	Unit	
	Forward current	lF	20	mA	
	Forward current derating (Ta ≥ 85°C)	ΔIF/ΔTa	-0.54	mA/°C	
	Peak transient forward current (Note 1)	IFP	1	A	
-ED	Reverse voltage	V _R	5	X	
1	Power Dissipation	PD	40	mW	90
	Power Dissipation Derating (Ta ≥ 85°C)	∆PD /°C	-1.0	mW/°C	\mathcal{D}
	Junction temperature	Тј	125	(°C)	
	"H" peak output current (Note 2)	IOPH	-0.6	A	
	"L" peak output current (Note 2)	IOPL	0.6	A	
or	Output voltage	Vo	35	V	
Detector	Supply voltage	Vcc	35	V	$\langle \langle \rangle$
ŏ	Output Power Dissipation	Po	260	mW	$\leq >$
	Output Power Dissipation Derating (Ta ≥ 85°C)	ΔPo /°C	6.5	mW/°C	
	Junction temperature	j	125	3°	S
Oper	rating frequency (Note 3)	f	25	kHz	\sim
Stora	age temperature range	Tstg	-55 to 125	°c	
Oper	ating temperature range	Topr	-40 to 100	○°C	
Lead	soldering temperature (10 s) (Note 4)	T _{sol}	260	J₀c	
Isola	tion voltage (AC, 60 s, R.H. \leq 60 %) (Note 5)	BVs	3750	Vrms	

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Pulse width $PW \le 1 \mu s$, 300 pps

Note 2: Exponential waveform pulse width PW \leq 10 µs, f \leq 15 kHz

Note 3: Exponential waveform IOPH $\leq -0.4 \text{ A}$ ($\leq 2.0 \text{ }\mu\text{s}$), IOPL $\leq +0.4 \text{ A}$ ($\leq 2.0 \text{ }\mu\text{s}$), Ta = 100 °C

Note 4: It is 2 mm or more from a lead root.

Note 5: Device considered a two terminal device: pins 1, 2, 3 and 4 shorted together, and pins 5, 6, 7 and 8 shorted together.

Recommended Operating Conditions

Characteristics	$\langle \rangle$	Symbol	Min	Тур.	Max	Unit
Input current, ON	(Note 7)	IF (ON)	7.5	_	10	mA
Input voltage, OFF		VF (OFF)	0	_	0.8	V
Supply voltage		Vcc	10	_	30	V
Peak output current		IOPH/IOPL	_	_	±0.2	А
Operating temperature		T _{opr}	-40		100	°C

Note: Recommended operating conditions are given as a design guideline to obtain expected performance of the device. Additionally, each item is an independent guideline respectively. In developing designs using this product, please confirm specified characteristics shown in this document.

Note 7: Input signal rise time (fall time) < 0.5 μ s

Electrical Characteristics (Ta = -40 to 100°C, unless otherwise specified)

Characteristics		Symbol	Test Circuit	Test Condition		Min	Typ.*	Max	Unit
Forward voltage	VF	-	I _F = 5 mA, Ta = 25 °C		_	1.55	1.70	V	
Temperature coefficient of voltage	∆VF/∆Ta	_	IF = 5 mA	\sim	_	-2.0	_	mV/°C	
Input reverse current		IR	_	V _R = 5 V, Ta = 25	°C	X	_	10	μA
Input capacitance		Ст	_	V = 0 V , f = 1 MHz,Ta = 25 °C		(\rightarrow)	45	_	pF
	"H" Level	IOPH1	1	V _{CC} = 15 V	V ₈₋₆ = 4 V		-0.4	-0.2	
Output current	H Level	IOPH2		$I_F = 5 \text{ mA}$	V ₈₋₆ = 10 V	<u></u>	-0.67	-0.4	
(Note 8)	"L" Level	IOPL1	2	V _{CC} = 15 V I _F = 0 mA	V ₆₋₅ = 2 V	0.2	0.35	_	A
		IOPL2			V ₆₋₅ = 10 V	0.4	0.63	_	
Output voltage	"H" Level	Vон	3	V/22 = 10 V/	10 = -100 mA, IF = 5 mA	6.0	8.5	_	v
Output voltage	"L" Level	Vol	4	Vcc = 10 V	IO = 100 mA, VF = 0.8 V	4	0.4	1.0	
Cuerch current	"H" Level	Іссн	5	Vcc = 10 to 30 V	IF = 10 mA 🚫	(\mathbf{Q})	1.4	2.0	
Supply current	"L" Level	ICCL	6	Vo open	IF = 0 mA	174	1.3	2.0	mA
Threshold input current $L \rightarrow H$		IFLH	_	Vcc = 15 V, Vo >	1V (C)		2.5	5	mA
Threshold input voltage $H \rightarrow L$ V _{FHL} — V _{CC} = 15 V, V _O < 1 V		1V	0.8	_	_	V			
Supply voltage	Vcc	-((\sim -	- (775	10	—	30	V	

*: All typical values are at Ta = 25 °C

Note 8: Duration of IO time \leq 50 μ s

Note 9: This product is more sensitive than the conventional product to static electricity (ESD) because of a lowest power consumption design.

General precaution to static electricity (ESD) is necessary for handling this component.

Isolation Characteristics (Ta = 25°C)

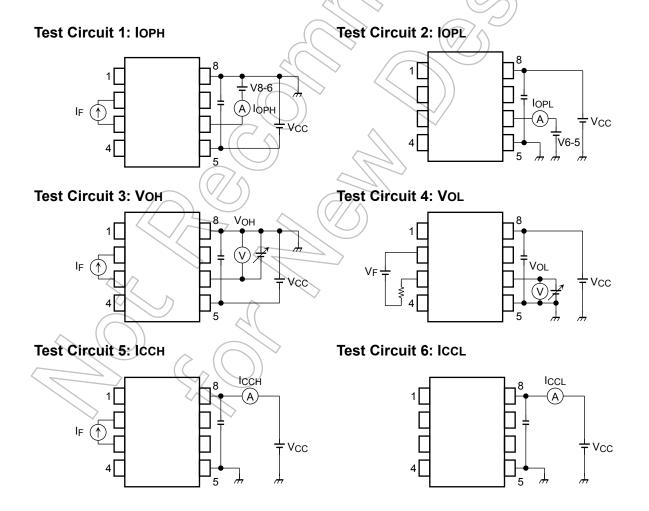
Characteristic	Symbol	Test Conditions		Min	Тур.	Max	Unit
Capacitance input to output	Cs	Vs = 0V, f = 1MHz	(Note5)	-	1.0		pF
Isolation resistance	Rs	Vs = 500 V, R.H. ≤ 60 %	(Note5)	1×10 ¹²	10 ¹⁴		Ω
Isolation voltage	BVs	AC,60 s		3750	_	_	Vrms

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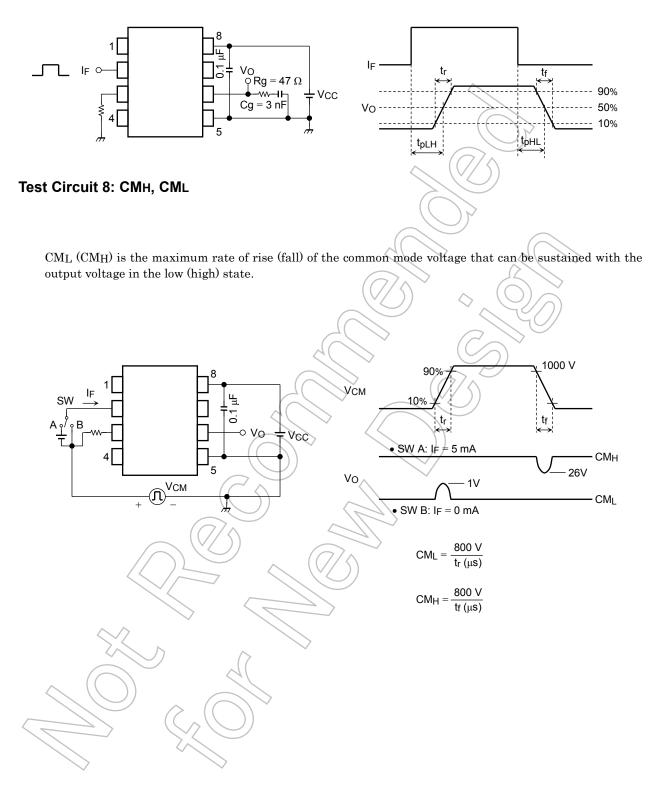
Switching Characteristics (Ta = -40 to 100° C, unless otherwise specified)

Characteristics		Symbol	Test Circuit	Test Co	ndition	Min	Typ.*	Max	Unit	
	$L \rightarrow H$	tpLH			V _{CC} = 30 V	$I_F = 0 \rightarrow 5 \text{ mA}$	100		700	
Propagation delay time	$H \rightarrow L$	tpHL		$R_g = 47 \Omega$ $C_g = 3 nF$	$I_F = 5 \rightarrow 0 mA$	100	-	700	ns	
Propagation delay difference between any two parts or chann		PDD t _{pHL} -t _{pLH}	7	$V_{CC} = 30 \text{ V},$ $R_g = 47 \Omega$ $C_g = 3 \text{ nF}$		-500)	500	ns	
Output rise time (10-90%)	1	tr		V _{CC} = 30 V	$F = 0 \rightarrow 5 \text{ mA}$		50	Ι		
Output fall time (90-10%)		tf		$R_g = 47 \Omega$ $C_g = 3 nF$	$I_F = 5 \rightarrow 0 \text{mA}$	_	50	-	ns	
Common mode transient immunity at high level output		CMH		V _{CM} = 1000 Vp-p	$I_F = 5 \text{ mA}$ VO (min) = 26 V -10000	-10000		\langle		
Common mode transient i at low level output	mmunity	CML	8	Ta = 25 °C V _{CC} = 30 V	IF = 0 mA VO (max) = 1 V	10000		_	V/μs	

*: All typical values are at Ta = 25 $^{\circ}$ C

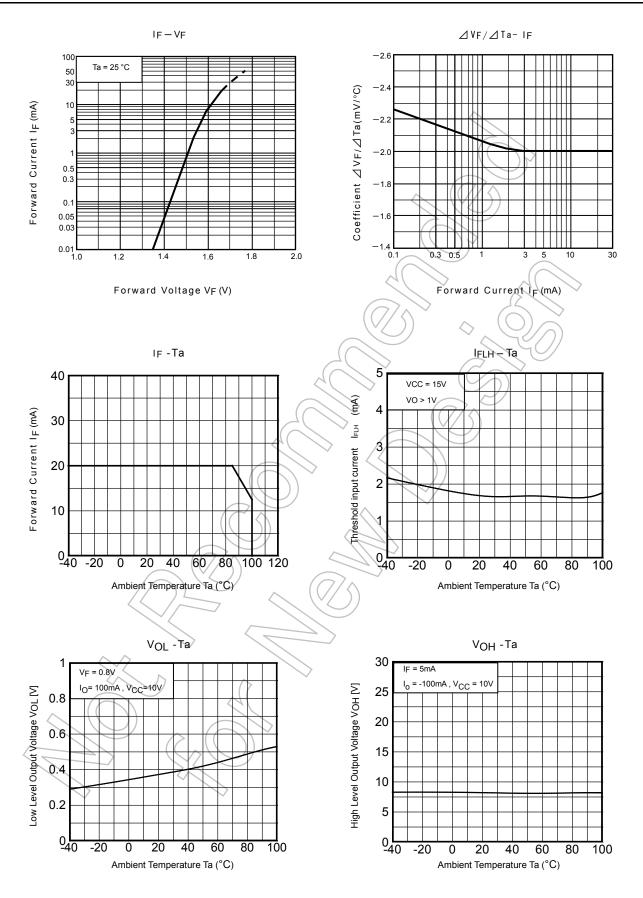


Test Circuit 7: tpLH, tpHL, tr, tf, PDD

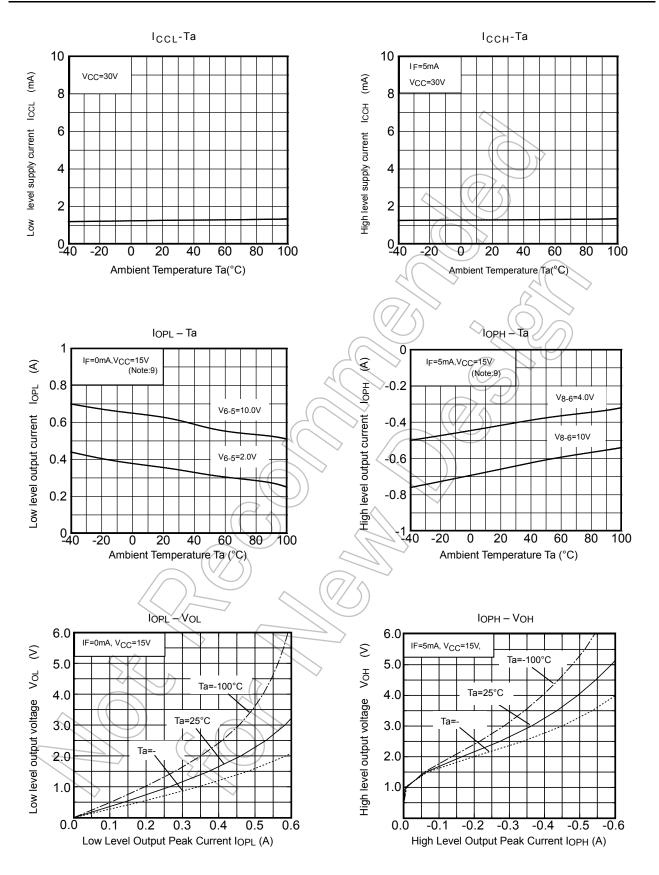


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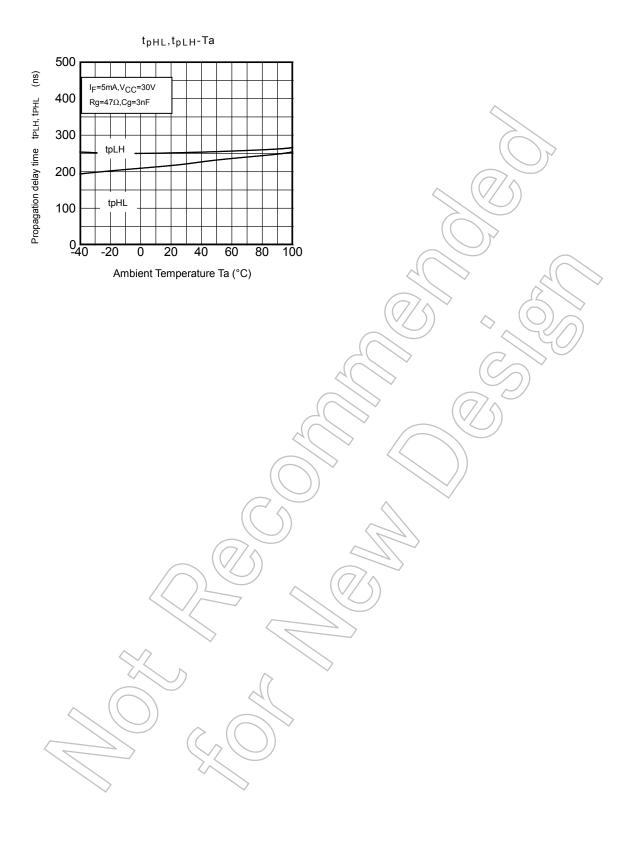
TLP351F



NOTE: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.



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