SiC MOSFET
Absolute Maximum Ratings and Electrical Characteristics

Description

SiC is a compound semiconductor material consisting of silicon (Si) and carbon (C). SiC MOSFET using SiC materials is a new-generation power device that can achieve higher withstand voltage and lower on-resistance than conventional Si MOSFET.

This document focuses on the absolute maximum ratings and electrical characteristics listed in SiC MOFET datasheet.

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1. Absolute Maximum Ratings

1.1. Absolute Maximum Ratings

Absolute maximum ratings are specified for each item that must not be exceeded during operation even instantaneously.

The maximum allowable values of the current that can be applied to SiC MOSFET and the voltage that can be applied are specified as the maximum rated values. Recognizing the maximum rating in designing circuits is very important not only for the effective operation of SiC MOSFET but also for reliable operation that is sufficiently high for the target operating hours.

Characteristics may not be recovered if used beyond the rating. When designing a circuit, pay attention to fluctuations in the supply voltage, variations in the characteristics of electrical components, the stress higher than the maximum ratings at the time of circuit adjustment, changes in ambient temperature, fluctuations in the input signal, etc., and avoid even one of the ratings.

However, even if the product is used under the operating conditions (operating temperature, current, voltage, etc.) within the absolute maximum rating, if the product is used continuously under high loads (high temperature and large current, high voltage application, large temperature change, etc.), the reliability of the product may be significantly reduced. Therefore, in order to ensure reliability, we recommend an appropriate reliability design considering de-rating.

1.2. Parameters Specified as Absolute Maximum Ratings

Items specified vary depending on the product. T_a = 25°C unless otherwise specified.

Item		Symbol	Unit	Description
Drain-Source Voltage		V_{DSS}	V	The maximum voltage allowed between the drain and source with a short circuit between the gate and source.
Gate-Source Voltage		V_{GSS}	V	The maximum voltage allowed between the gate and source with a short circuit between the drain and source.
Drain current	DC	I_D	A	The maximum DC current that can pass through the drain to source.
	Pulse	I_{DP}	A	Maximum allowable peak drain current for pulsed operation.
Power Dissipation (T_c = 25 °C)		P_D	W	The maximum power that can be dissipated by a MOSFET
Avalanche current		I_{AS}	A	The maximum peak non-repetitive current that is permitted under avalanche conditions
Avalanche energy		E_{AS}	mJ	The maximum non-repetitive energy that the MOSFET can dissipate under avalanche breakdown conditions
Channel temperature		T_{ch}	°C	The maximum allowable chip temperature at which a MOSFET operates
Storage temperature range		T_{stg}	°C	The maximum temperature at which a MOSFET may be stored without voltage applying
Isolation voltage		$V_{ISO(RMS)}$	V	The maximum voltage at which a MOSFET can maintain isolation between the designated point on the case and electrode leads
Tightening torque		TOR	N·m	The maximum torque that may be applied in the axial direction when tightening a screw

1.3. Drain-Source Voltage V_{DSS}

The drain-to-source voltage when the gate-to-source is short-circuited. If a voltage exceeding the rating is applied, there is a risk of SiC MOSFET failure due to entering the breakdown mode. Also, do not use the gate open from the source. Since SiC MOSFET has a very high input-impedance, external noises can bias the gate-source and "on" the gate-source, possibly causing degradation or destruction of the device. If it happen, connect a pull-down resistor in parallel between the gate and source.

1.4. Gated-Source Voltage V_{GSS}

The maximum voltage allowed between the gate-to-source with SiC MOSFET drain and source short-circuited. This rating is attributable to the withstand capacity of the gate oxide, but the value is determined in consideration of the practical voltage and reliability.

Generally, V_{GSS} rating of Si MOSFET takes the same value for positive and negative, but for SiC MOSFET, it may differ for positive and negative. When designing, make sure that V_{GSS} is not exceeded maximum rating due to noises, etc.

1.5. Drain Current I_D

Generally, the maximum continuous (DC) current that the power MOSFET can pass in the forward direction is specified as I_D, whereas the pulsed current that the power MOSFET can pass in the forward direction is specified as I_{DP}. Likewise, the DC and pulsed currents in the reverse (diode) direction are specified as I_{DR} and I_{DRP}, respectively (under ideal heat dissipation conditions).

However, the maximum current values in the forward direction are limited by the power loss caused by drain-source on-state resistance, and those in the reverse direction are limited by the power loss due to the forward voltage across the diode. Since current ratings are affected by heat dissipation conditions, maximum allowable current values are specified so that the channel temperature will not exceed the rated $T_{ch\ (max)}$ value.

$$I_D = \sqrt{\frac{T_{ch\ (max)} - T_C}{R_{DS(ON)(max)} \times R_{th(ch-c)}}}$$

$$I_{DP} = \sqrt{\frac{T_{ch\ (max)} - T_C}{R_{DS(ON)(max)} \times r_{th(ch-c)}\ (t)}}$$

$T_{ch\ (max)}$: Channel Temp. max.
T_c: Case temperature (25°C)
$R_{th(ch-c)}$: Steady-state thermal resistance
$r_{th\ (ch-c)}$ (t): Transient thermal resistance
$R_{DS(ON)\ (max)}$: Maximum value of the on-resistance between the drain-source at the maximum channel temperature

The drain current I_D that the MOSFET device can carry is restricted not only by power loss but also by the current-carrying capability of a package, the maximum channel temperature, the safe operating area and other factors.

1.6. Power Dissipation P_D

P_D is the maximum power that the MOSFET can dissipate continuously under the specified thermal conditions.

The allowable power dissipation varies with the conditions under which the MOSFET is used (such as ambient temperature and heat dissipation conditions).

P_D is calculated as the maximum power dissipation for a device with an infinite heat sink at 25 °C ambient.

$$P_D = \frac{T_{ch(max)} - 25\ °C}{R\ th(ch-c)}\ (W)$$

In addition, the power dissipation P_{DP} during the transient period is calculated as follows according to the transient thermal resistance in the individual datasheet.

$$P_{DP} = \frac{T_{ch(max)} - 25\ °C}{r\ th(ch-c)}\ (W)$$

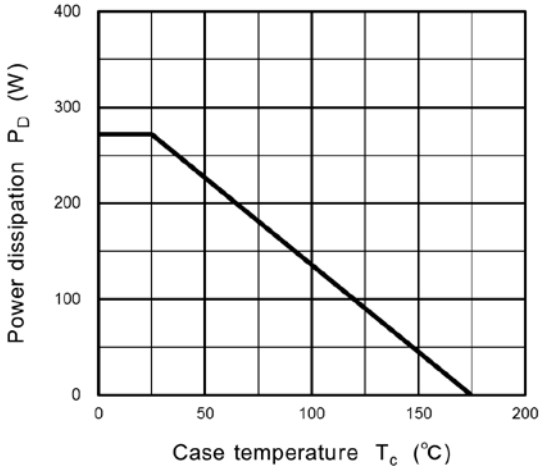


Figure 1.1 Example of P_D - T_c Characteristics

1.7. Avalanche Current I_{AS}, Avalanche Energy E_{AS}

When a SiC MOSFET is used as a high-speed switching device, the self-inductance of the circuit itself and stray inductances cause a high surge voltage to be applied between the drain and source at turn-off, sometimes causing the surge voltage to exceed the rating of the device and enter the breakdown mode. At this time, an avalanche current flows, and if the current or energy exceeds the device limit, destruction will occur. This mode is called avalanche destruction. In addition, the allowable current is called the avalanche current (I_{AS}) and the energy is called the avalanche energy (E_{AS}).

1.8. Channel Temperature T_{ch}, Storage Temperature T_{stg}

The materials that constitute a power MOSFET and their reliability determine the maximum channel temperature $T_{ch\ (max)}$. The maximum channel temperature must be considered not only in terms of the functional operation of the power MOSFET, but also in terms of its reliability such as device degradation and lifetime.

Storage temperature T_{stg} is the temperature range in which a power MOSFET can be stored without voltage applying. The materials that constitute the power MOSFET and their reliability also determine the storage temperature range.

1.9. Isolation Voltage $V_{ISO(RMS)}$

For devices housed in a fully molded package, isolation voltage represents the level of electrical isolation between the designated point on the case and the internal circuit and electrode terminals.

$V_{ISO(RMS)}$ is tested by applying AC voltage to the power MOSFET for a specified period of time. Isolation voltage is specified as the RMS of AC voltage.

1.10. Tightening Torque TOR

When attaching MOSFET devices to a thermal fin, the prescribed tightening torque must be followed.
If the torque is too low, the mounting screws will loosen. If the torque is too high, the device could be damaged.

2. Thermal Resistance

2.1. Thermal Resistance Characteristics

Item	Symbol	Unit	Description
Channel to case thermal resistance	$R_{th(ch-c)}$	°C / W	Thermal resistance with the case temperature kept at an ambient temperature at 25 °C under ideal heat dissipation conditions.
Channel to ambient thermal resistance	$R_{th(ch-a)}$	°C / W	Thermal resistance from channel to ambient temperature at 25 °C.

2.2. What is Thermal Resistance?

Thermal resistance is the ability of a material to resist the flow of thermal energy.

The power consumed by a semiconductor chip is converted into heat, which is transferred to the case (package) and eventually released into ambient air through a thermal fin or other thermally conductive material. An increase in power dissipation (P_D) causes a further increase in the device temperature (ΔT).

ΔT can be calculated as $\Delta T = R_{th} \times P_D$. Here, R_{th} is a constant defining a relationship between ΔT and P_D. This constant is called thermal resistance.

2.3. Thermal Resistance Calculation

The thermal resistance of the product spec mainly include the following.

a) $R_{th(ch-c)}$: Channel to Case Thermal Resistance

This is the thermal resistance when the case temperature is kept at an ambient temperature at 25 °C, which is equivalent to the condition with an infinite hestsink attached.

$$R_{th(ch-c)} = \frac{T_{ch(max)} - 25\ °C}{P_{D(T_C=25°C)}}\ (°C/W)$$

b) $R_{th(ch-a)}$: Channel to ambient Thermal Resistance

Thermal resistance from channels to the ambient air at 25 °C and it is $R_{th(ch-c)}+R_{th(c-a)}$.

Note, however, that thermal resistance varies with board assembly condition and other factors.

$$R_{th(ch-a)} = \frac{T_{ch(max)} - 25\ °C}{P_{D(T_a=25°C)}}\ (°C/W)$$

2.4. Transient Thermal Resistance and Steady-state Thermal Resistance

The transient thermal resistance is the function of time while device is affected by thermal capacitance. Steady-state thermal resistance is a property during the time the device is no longer affected by thermal capacitance. The figure below shows a example of transient thermal resistance curve.

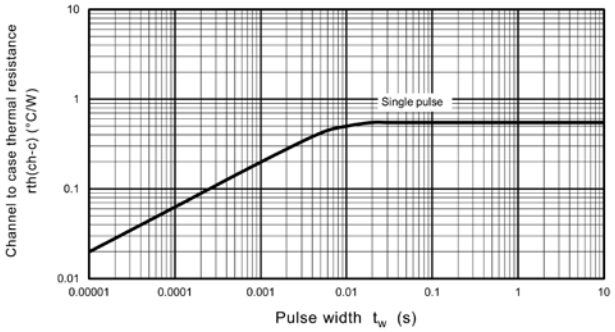


Figure 2.1 Example of $r_{th(ch-c)}$ - t_w Characteristics

3. Safe Operation Area

3.1. What is the Safe Operating Area?

The Safe Operating Area represents the range of current/voltage values that can be applied to the device at a time. There are forward bias and reverse bias safe operating areas.

In designing, the current/voltage applied at the same time is plotted in the safe operating area to find if there are any problems, which is transferred from I_D, V_{DS} waveform during switching operation. If the waveform is not within the safe operating area, it is necessary to take measures including device or circuit change.

3.2. Forward Bias Safe Operating Area

The forward-bias safe operating area shows the area of current and voltage that SiC MOSFET can safely operate except the turn-off period. Channel-temperature increases when SiC MOSFET is operated. If the operating waveform is within the safe operating range, the channel temperature is under the maximum rating. The secondary breakdown limit is the area where the temperature rises rapidly because current does not flow uniformly inside the chip and a portion of the current is concentrated. Except for the turn-off period, the operation waveform of SiC MOSFET must be designed within the forward-bias safe operating area (e.g. review of the heat dissipation design). The forward bias safe operating are is limited from current, on-resistance, Thermal (loss), secondary breakdown and voltage and is specified by:

1. Current limit
   Area limited by drain current rating. Limited by $I_{D(max)}$ for DC (continuous) and $I_{DP(max)}$ for pulse.
2. On-resistance limit
   This area is theoretically limited by the on-resistance $R_{DS(ON)\ (max)}$, and I_D is equal to V_{DS} / $R_{DS(ON)}$.
3. Thermal limit
   The area limited by the power-loss P_D. P_D (allowable losses) = $I_D \times V_{DS}$
4. SB(Secondary Breakdown) limit
   Area equivalent to secondary breakdown due to current concentration.
5. Voltage limit
   This area is limited by the drain source voltage V_{DSS}.

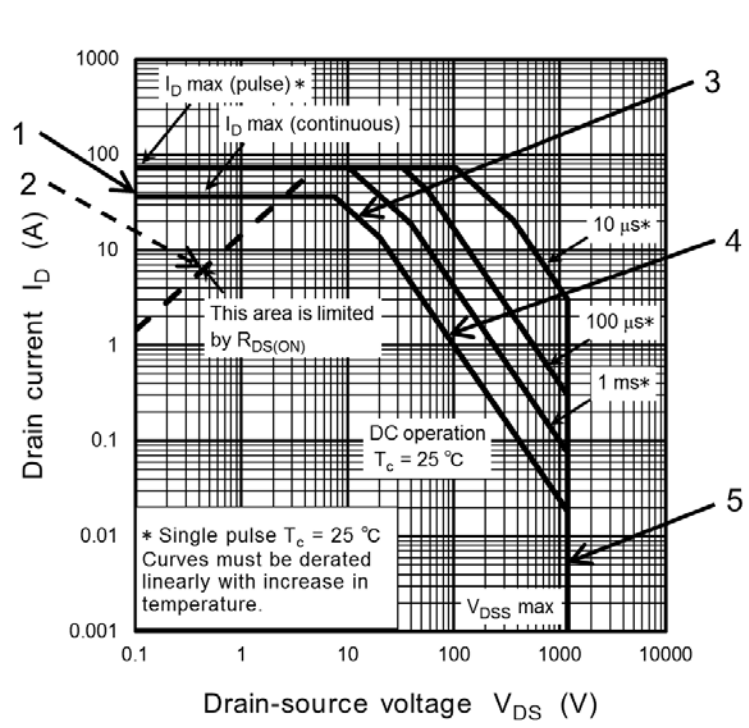


Figure 3.1 Example of forward bias safe operation area

3.3. Reverse Bias Safe Operating Area

The reverse-bias safe operating area shows the current and voltage areas where SiC MOSFET can safely turn off. During the process of turning SiC MOSFET from on-state to off-state, a surge-voltage is generated to SiC MOSFET due to the inductance of the circuit. It is necessary to design the circuit so that the operating locus of the cutoff current and the surge voltage generated of the turn-off at that time to be within the reverse-bias safe operating area (e.g., reduction of circuit inductance, addition of surge absorbing circuit, and relaxation of turn-off speed).

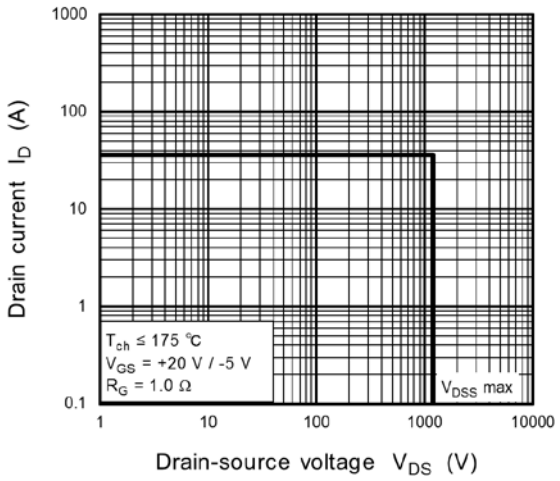


Figure 3.2 Example of reverse bias safe operation area

4. Electrical Characteristics

Electrical characteristics specified in SiC MOSFET datasheet are explained by item. T_a = 25 °C unless otherwise specified.

4.1. Static Characteristics

Item	Symbol	Unit	Description
Gate leakage current	I_{GSS}	μA	The leakage current that occurs when the specified voltage is applied across gate and source with drain and source short-circuited.
Drain cut-off current	I_{DSS}	μA	The leakage current that occurs when a voltage is applied across drain and source with gate and source short-circuited.
Drain-source Breakdown Voltage	$V_{(BR)DSS}$	V	The withstand voltage between the drain and source with the gate and source are short-circuited.
Gate threshold voltage	V_{th}	V	Vth stands for "threshold voltage." Vth is the gate voltage that appears when the specified current flows between drain and source.
Drain-source on-resistance	$R_{DS(ON)}$	Ω	The resistance across drain and source when the MOSFET is in the "on" state.

4.1.1. Gate-Leakage Current I_{GSS}

I_{GSS} is the leakage current when a specified voltage is applied between the gate and source with the drain and source shorted.

Positive or negative may occur depending on the direction of the applied voltage.

4.1.2. Drain Cut-off Current I_{DSS}

I_{DSS} is the leakage current when a specified voltage is applied between the drain and source with the gate and source shorted.

4.1.3. Drain-Source Breakdown Voltage $V_{(BR)DSS}$

$V_{(BR)DSS}$ is specified as voltage with shorted gate and source when a specified drain current I_D is applied.
V_{DSS} of SiC MOSFET has a positive thermal coefficient.In a low-temperature environment, It is less than V_{DSS} specified at 25 ºC.

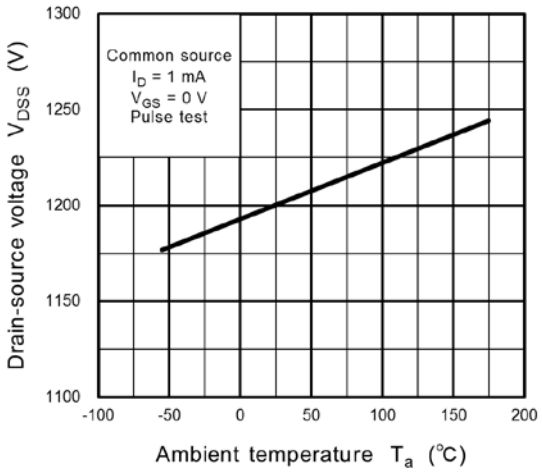


Figure 4.1 Example of V_{DSS} - T_a Characteristics

4.1.4. Gate Threshold Voltage V_{th}

V_{th} is the gate-voltage when a specified current flows between the drain and source. V_{th} has negative temperature coefficient, which make it easier to turn on with lower voltages in high temperature environment. It is necessary to check for malfunction due to noise or mis-firing.

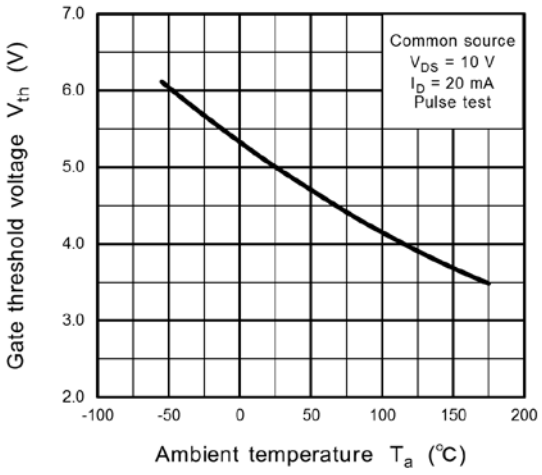


Figure 4-2 Example of V_{th} - T_a Characteristics

4.1.5. Drain-Source On-Resistance $R_{DS(ON)}$

$R_{DS(ON)}$ is the drain-to-source resistance when SiC MOSFET is on. $R_{DS(ON)}$ of SiC MOSFET is temperature-sensitive and must be noted. $R_{DS(ON)}$ in SiC MOSFET mainly consists of a channel resistance component with a negative temperature coefficient and a drift-layer resistance component with a positive temperature coefficient.

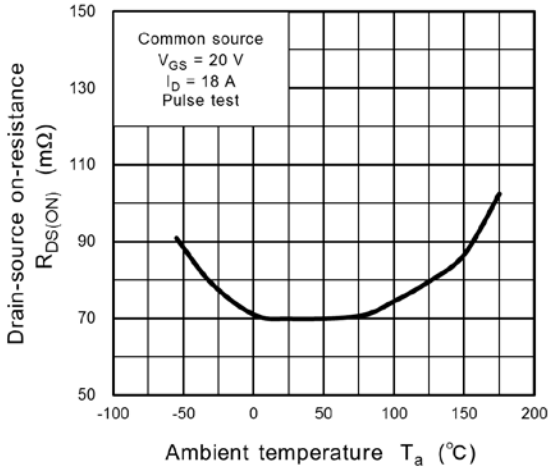


Figure 4.3 Example of $R_{DS(ON)}$ - T_a Characteristics

4.2. Dynamic Characteristics

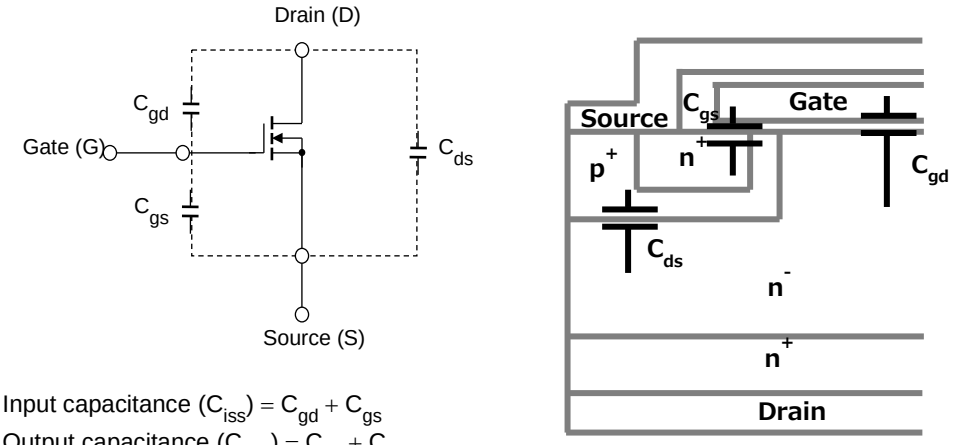
Item	Symbol	Unit	Description
Capacitance	C_{iss} C_{rss} C_{oss}	pF	Ciss is the input capacitance, Crss is the reverse transfer capacitance, and Coss is the output capacitance. Capacitances affect the switching performance of a power MOSFET.
Output Capacitance Charge Energy	E_{oss}	μJ	This is the energy required to charge C_{oss}.
Gate resistance	r_g	Ω	The gate resistance inside SiC MOSFET.
Switching time	$t_{d(on)}$ t_r $t_{d(off)}$ t_f	ns	t_{don} is the turn-on delay time, t_r is the rise time, t_{doff} is the turn-off delay time, and t_f is the fall time.
Switching loss	E_{on} E_{off}	mJ	E_{on} is a turn-on loss and E_{off} is a turn-off loss.

4.2.1. Capacitance Characteristics C_{iss}, C_{rss}, C_{oss}

In a power MOSFET, the gate is insulated by a thin silicon oxide. Therefore, a power MOSFET has capacitances between the gate-drain, gate-source and drain-source terminals as shown in Figure 4.4.
The gate-drain capacitance C_{gd} and the gate-source capacitance C_{gs} are mainly determined by the structure of the gate electrode, while the drain-source capacitance C_{ds} is determined by the capacitance of the vertical p-n junction. For the power MOSFET, the input capacitance ($C_{iss} = C_{gd} + C_{gs}$), the output capacitance ($C_{oss} = C_{ds} + C_{gd}$) and the reverse transfer capacitance ($C_{rss} = C_{gd}$) are important characteristics.

Figure 4.5 shows the dependency of C_{iss}, C_{rss} and C_{oss} on drain-source voltage V_{DS}.
Switching characteristics of a MOSFET manly vary with the input capacitance C_{iss} and the output impedance of the drive circuit.

Gate current flows from gate to source instantaneously to charge the input capacitance. Therefore, the lower the output impedance of the drive circuit, faster the switching speed. Large input capacitance of a MOSFET causes a large power loss at light load. C_{iss}, C_{rss} and C_{oss} hardly vary with temperature.



Input capacitance (C_{iss}) = C_{gd} + C_{gs}
Output capacitance (C_{oss}) = C_{ds} + C_{gd}
Reverse transfer capacitance (C_{rss}) = C_{gd}

Figure 4.4 Capacitance equivalent circuit

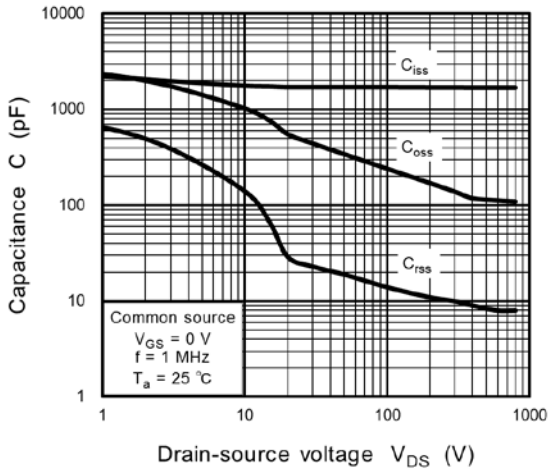


Figure 4.5 Example of C - V_{DS} Characteristics

4.2.2. Output Capacitance Charge Energy E_{oss}

E_{oss} is the energy required to charge C_{oss}. It can be derived from the characteristic between C_{oss} and V_{DS}. C (V) is a function of V_{DS} dependent output capacitance C_{oss}.

$$Q_{oss} = \int_o^{V_{DS}} C(V)\, dv$$

$$E_{oss} = Q_{oss} \times V_{DS}$$

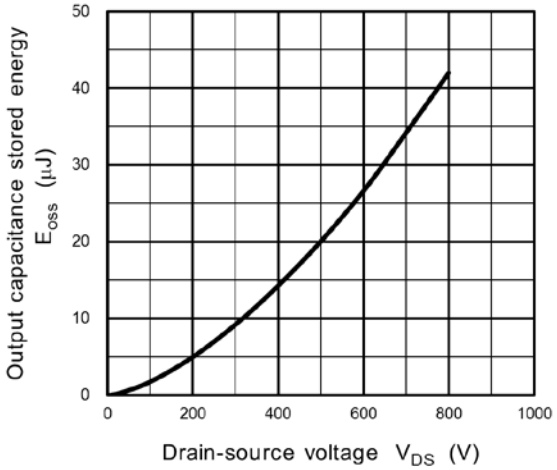


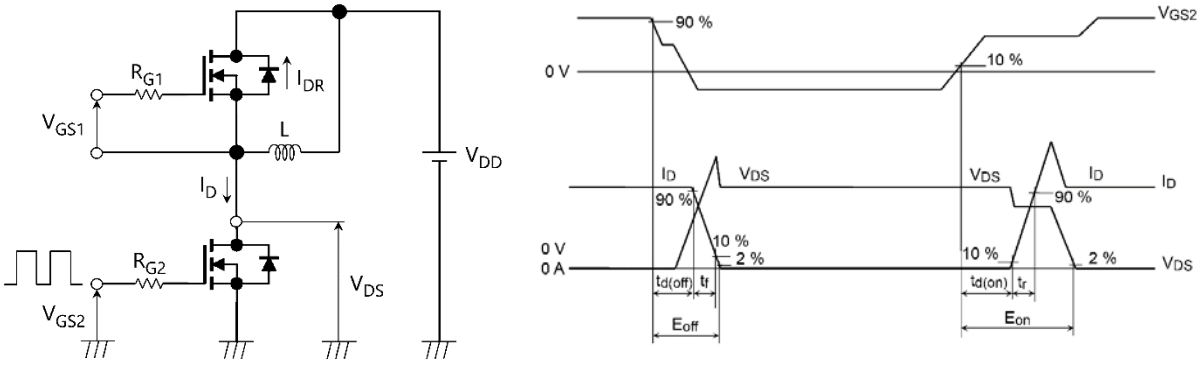
Figure 4.6 Example of E_{oss} - V_{DS} Characteristics

4.2.3. Gate Resistance r_g

Gate resistance inside MOSFET.

4.2.4. Switching-time $t_{d(on)}$, t_r, $t_{d(off)}$, t_{off}

The remarkable property of SiC MOSFET being a majority carrier device is its superiority to bipolar transistors in high-speed operation and high-frequency switching operation. The following figure shows the switching time measurement circuit and the definition of the waveform.



(a) Switching time measurement circuit **b) Waveform definition**

Figure 4.7 Definition of Switching Time Measurement Circuit and Waveform

The symbols used in the above input and output waveforms are briefly explained below:

1) $t_{d(on)}$: turn-on delay time
The time between when the gate source voltage reaches 10% of the set voltage and when the drain current rises to 10% of the set current at turn-on.

2) t_r: Rise time
The time it takes for the drain current to rise from 10% to 90% of the set point at turn-on.

3) t_{on}: turn-on time
Turn-on time is equal to $t_{d(on)} + t_r$.

4) $t_{d(off)}$: turn-off delay time
The time from when the gate-to-source voltage reaches 90% of the set voltage at turn-off until the drain current drops to 90% of the set current.

5) t_f: fall time
The time it takes for the drain current from 90% to drop to 10% of the setpoint at turn-off.

6) t_{off}: turn-off time
Turn off time is equal to $t_{d(off)} + t_f$.

4.2.5. Switching-loss E_{on}, E_{off}

1) E_{on} turn-on switching loss
This is the loss that occurs during the period from 10% of the gate to source voltage until the drain-to-source voltage drops to 2%.

2) E_{off} turn-off switching loss
The loss that occurs during the period from 90% of the gate-to-source voltage until 2% of the drain current.

4.3. Gate Charge Characteristics

Item	Symbol	Unit	Description
Gate input charge	Q_g	nC	The total amount of charge that the gate voltage can reach from zero to the specified voltage.
Gate-Source charge 1	Q_{gs1}	nC	The amount of charge that charges the gate-to-source voltage prior to a drop in the drain-to-source voltage until MOSFET begins to turn on.
Gate-drain charge	Q_{gd}	nC	Q_{gd} is the amount of charge in the mirror period during which the drain-to-source voltage drops and charges the capacitance between the gate and drain.

4.3.1. Gate Charge Q_g, Q_{gs1}, Q_{gd}

The gate which is the input terminal, is isolated. The amount of charge Q seen from the gate terminal is an important parameter. The figure below shows the definition of the gate charge amount.

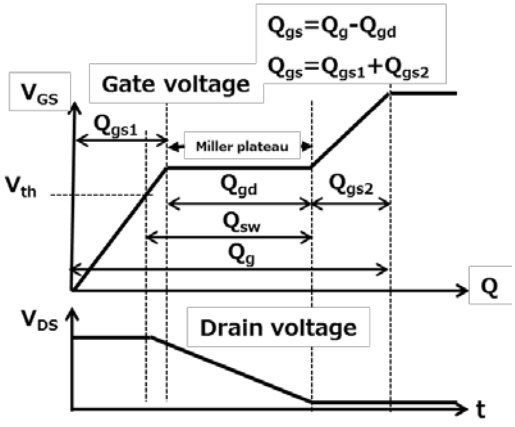
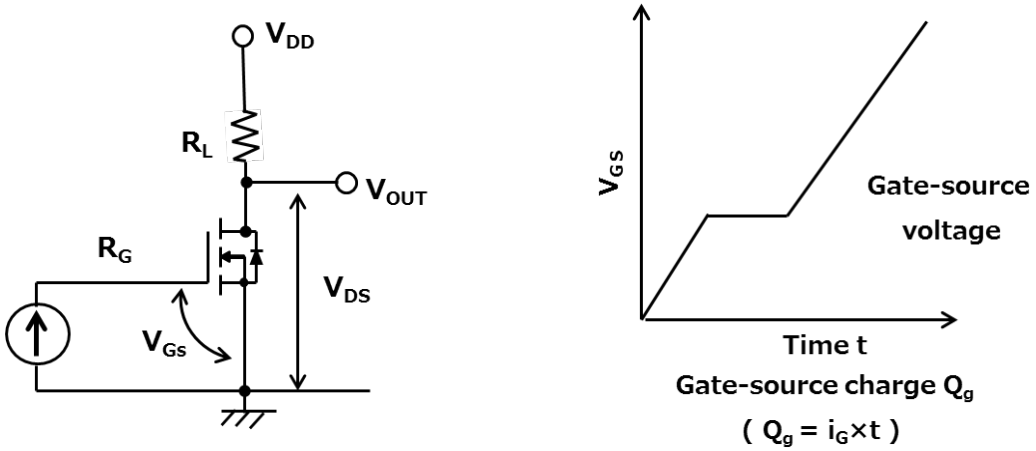


Figure 4.8 Definition of the amount of gate charge

4.3.2. Calculation of Total Gate Charge

During the turn-on of a power MOSFET, a current flows to the gate, charging the gate-source and gate-drain capacitances. The amount of gate charge is measured using a test circuit shown in Figure 4.9 (a). A constant current is applied to the gate to obtain a graph like the one shown in Figure 4.9 (b) showing a change in gate-source voltage V_{GS} over time. The time axis can be expressed in terms of gate capacitance Q_g by multiplying time by constant gate current i_G. Gate charge is calculated as follows:

$$Q_g = \int_0^t i_G(t)dt$$



(a) Gate Charge Measurement Circuit (b) Gate-Source Voltage Waveform

Figure 4.9 Gate Charge Measurement Circuit and Gate-Source Voltage Waveform

4.4. Source-Drain Characteristics

Item	Symbol	Unit	Description
Diode forward current (DC)	I_F	A	The maximum permissible forward current (DC) of the diode.
Diode forward current (pulse)	I_{FP}	A	The maximum permissible forward current (pulse) of the diode.
Forward voltage (diode)	V_{DSF}	V	Drain-to-source voltage when forward current is applied to the diode.
Reverse recovery time	t_{rr}	ns	The time (t_{rr}) and charge (Q_{rr}) until the reverse recovery current disappears in the reverse recovery operation of the body diodes under the specified measuring conditions. The peak current at that time is I_{rr}.
Reverse recovery charge	Q_{rr}	nC	
Peak reverse recovery current	I_{rr}	A	

4.4.1. Diode Characteristics

SiC MOSFET is structurally equipped with a body diode (PN-junction diode) between the source and drain.

In addition, some SiC MOSFET products has a built-in SiC SBD in parallel with a body diode in the same direction as the anode to cathode. The "Internal Circuit Diagram" in the data sheet is the same regardless of the presence or absence of SBD. In particular, PN junction diodes and SBD are not separately described.

The current rating of the diodes is defined separately for SiC MOSFET current rating I_D (continuous), I_{DP}

(pulsed), and separately for the electrical characteristics of the datasheet. For the voltage rating V_{RRM} of the diode, values not listed in the electrical characteristics are the same as the drain-source voltage rating V_{DSS} of SiC MOSFET. The figure below shows a sample I_{DR} - V_{DS} response for a MOSFET with a built-in SiC SBD. The forward current I_F to forward voltage V_F characteristics of SBDs are subject to V_{GS}=0 to - 5V conditions of I_{DR} - V_{DS} characteristics.

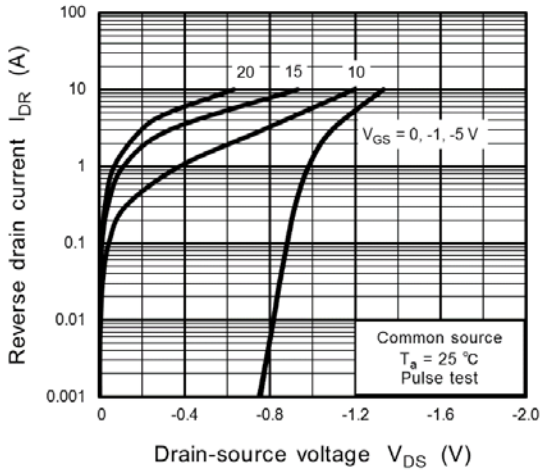


Figure 4.10 I_{DR} - V_{DS} Characteristics (Including I_F - V_F Characteristics of Built-in SBDs)

The figure below shows the measurement circuit of the diode reverse recovery characteristics and the definition of the waveform.

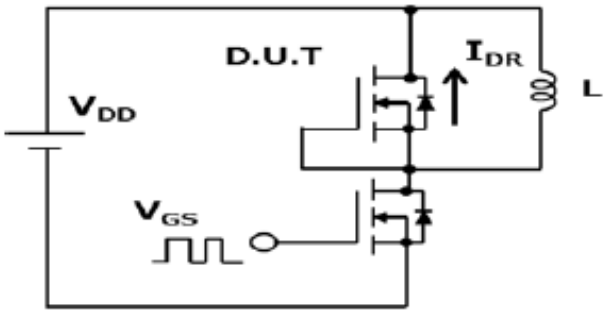


Figure 4.11 Measurement circuit for diode reverse recovery characteristics

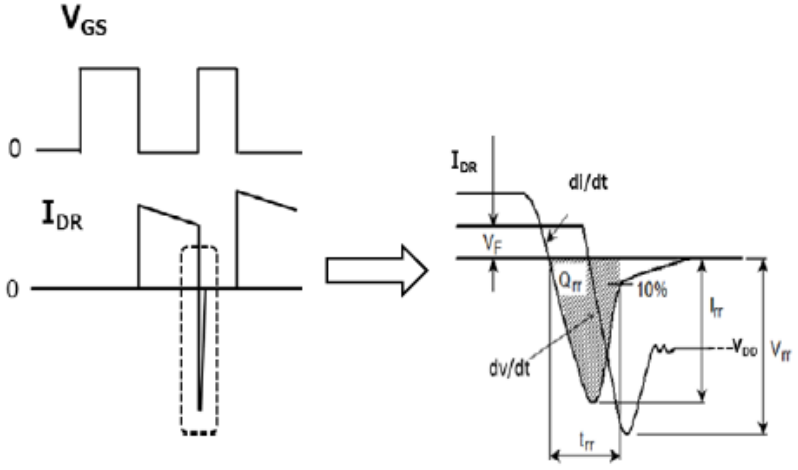


Figure 4.12 Diode Reverse Recovery Characteristic Waveform Definition

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