

CMOS Digital Integrated Circuits Silicon Monolithic

# 74HC4051FT,74HC4052FT

## 1. Functional Description

74HC4051FT: 8-Channel Analog Multiplexer/Demultiplexer

74HC4052FT: Dual 4-Channel Analog Multiplexer/Demultiplexer

## 2. General

The 74HC4051FT/74HC4052FT are high speed CMOS ANALOG MULTIPLEXER/DEMUTIPLEXER fabricated with silicon gate CMOS technology. They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The 74HC4051FT has an 8 channel configuration and the 74HC4052FT has a 4 channel  $\times$  2 configuration.

The digital signal to the control terminal turns "ON" the corresponding switch of each channel a large amplitude signal ( $V_{CC} - V_{EE}$ ) can then be switched by the small logical amplitude ( $V_{CC} - GND$ ) control signal.

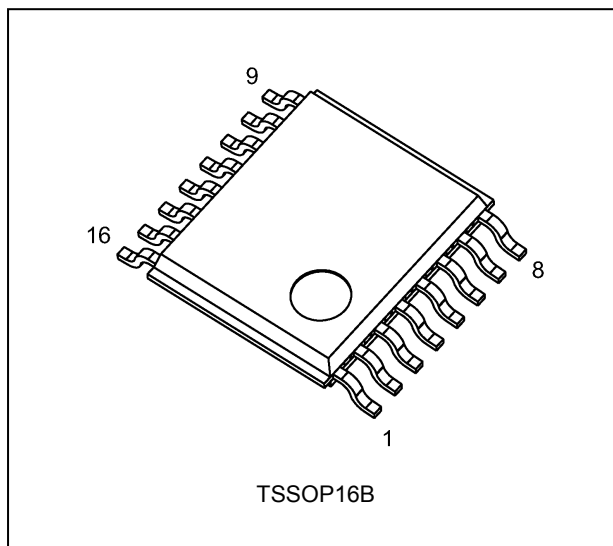
For example, in the case of  $V_{CC} = 5\text{ V}$ ,  $GND = 0\text{ V}$ ,  $V_{EE} = -5\text{ V}$ , signals between  $-5\text{ V}$  and  $+5\text{ V}$  can be switched from the logical circuit with a single power supply of  $5\text{ V}$ . As the ON-resistance of each switch is low, they can be connected to circuits with low input impedance.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

## 3. Features

- (1) Wide operating temperature range:  $T_{opr} = -40$  to  $125\text{ }^{\circ}\text{C}$
- (2) Low power dissipation:  $I_{CC} = 4.0\text{ }\mu\text{A}$  (max) ( $V_{CC} = 6.0\text{ V}$ ,  $V_{EE} = GND$ ,  $T_a = 25\text{ }^{\circ}\text{C}$ )
- (3) Low ON-resistance:  $R_{ON} = 50\text{ }\Omega$  (typ.) at  $V_{CC} - V_{EE} = 9\text{ V}$
- (4) High degree of linearity: THD = 0.020 % (typ.) at  $V_{CC} - V_{EE} = 9\text{ V}$

## 4. Packaging

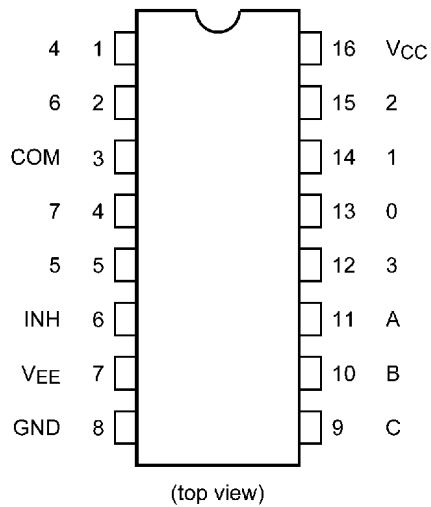


Start of commercial production

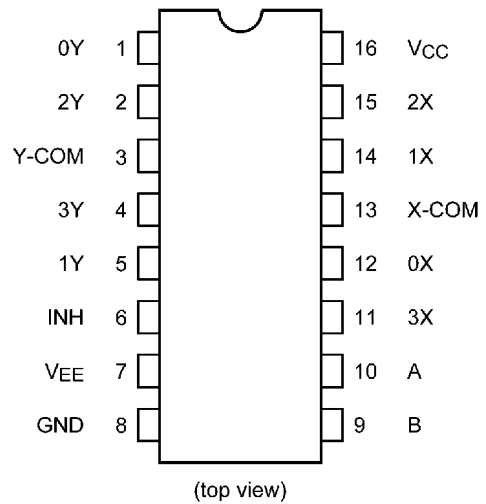
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### 5. Pin Assignment

74HC4051FT

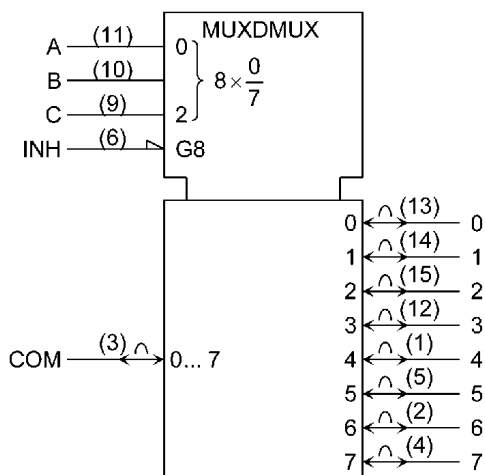


74HC4052FT

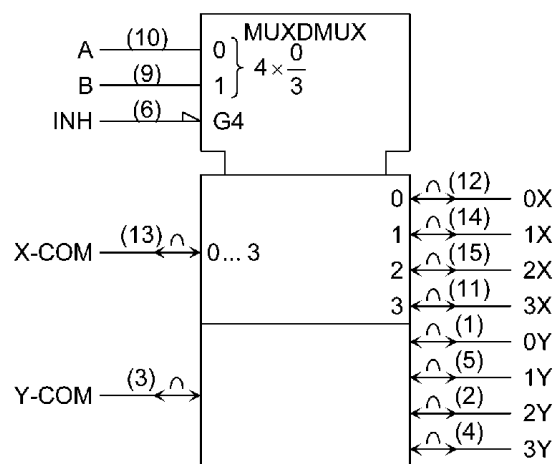


### 6. IEC Logic Symbol

74HC4051FT

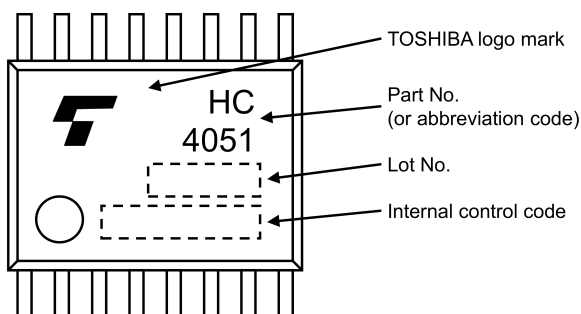


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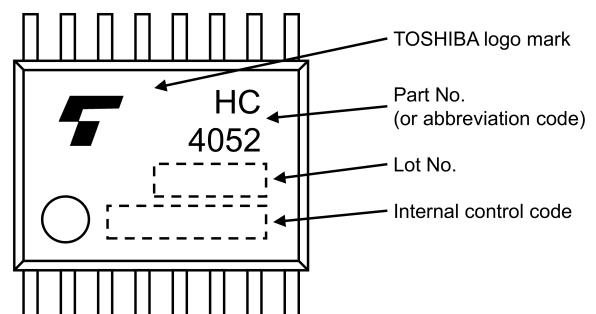


### 7. Marking

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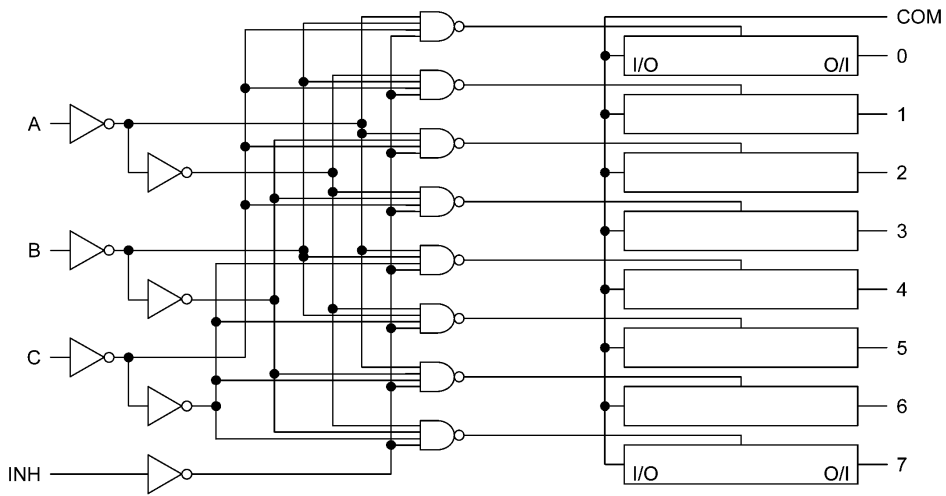


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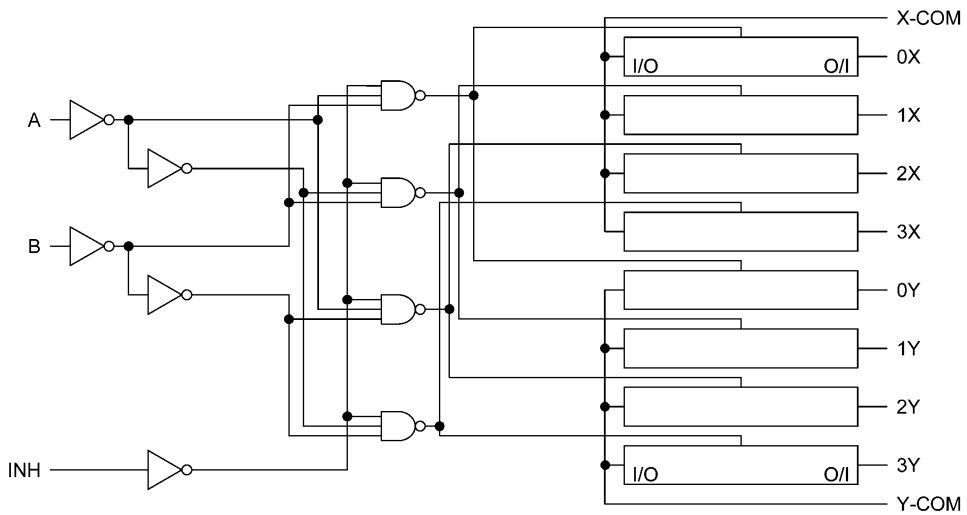


### 8. System Diagram

74HC4051FT



74HC4052FT



### 9. Truth Table

Input Inhibit	Input C*	Input B	Input A	ON Channel 74HC4051FT	ON Channel 74HC4052FT
L	L	L	L	0	0X, 0Y
L	L	L	H	1	1X, 1Y
L	L	H	L	2	2X, 2Y
L	L	H	H	3	3X, 3Y
L	H	L	L	4	—
L	H	L	H	5	—
L	H	H	L	6	—
L	H	H	H	7	—
H	X	X	X	None	None

X: Don't care

\*: Except 74HC4052FT

### 10. Absolute Maximum Ratings (Note)

Characteristics	Symbol	Note	Rating	Unit
Supply voltage	$V_{CC}$		-0.5 to 7.0	V
Supply voltage	$V_{EE}$		-7.0 to 0	V
Supply voltage	$V_{CC}-V_{EE}$		-0.5 to 13.0	V
Input voltage	$V_{IN}$		-0.5 to $V_{CC} + 0.5$	V
Switch I/O voltage	$V_{I/O}$		$V_{EE} - 0.5$ to $V_{CC} + 0.5$	V
Input diode current	$I_{IK}$		$\pm 20$	mA
I/O diode current	$I_{I/OK}$		$\pm 20$	mA
Switch through current	$I_T$		$\pm 25$	mA
$V_{CC}$ /ground current	$I_{CC}$		$\pm 50$	mA
Power dissipation	$P_D$	(Note 1)	180	mW
Storage temperature	$T_{stg}$		-65 to 150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: 180 mW in the range of  $T_a = -40$  to  $85$  °C. From  $T_a = 85$  to  $125$  °C a derating factor of  $-3.25$  mW/°C shall be applied until 50 mW.

### 11. Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	$V_{CC}$	2.0 to 6.0	V
Supply voltage	$V_{EE}$	-6.0 to 0	V
Supply voltage	$V_{CC}-V_{EE}$	2.0 to 12.0	V
Input voltage	$V_{IN}$	0 to $V_{CC}$	V
Switch I/O voltage	$V_{I/O}$	$V_{EE}$ to $V_{CC}$	V
Operating temperature	$T_{opr}$	-40 to 125	°C
Input rise and fall times	$t_r, t_f$	0 to 50	μs

Note: The operating ranges must be maintained to ensure the normal operation of the device. Unused inputs must be tied to either  $V_{CC}$  or GND.

### 12. Electrical Characteristics

#### 12.1. DC Characteristics (Unless otherwise specified, $T_a = 25\text{ }^\circ\text{C}$ )

Characteristics	Symbol	Test Condition	$V_{EE}$ (V)	$V_{CC}$ (V)	Min	Typ.	Max	Unit
High-level input voltage	$V_{IH}$	—		2.0	1.50	—	—	V
				4.5	3.15	—	—	
				6.0	4.20	—	—	
Low-level input voltage	$V_{IL}$	—		2.0	—	—	0.50	V
				4.5	—	—	1.35	
				6.0	—	—	1.80	
ON-resistance	$R_{ON}$	$V_{IN} = V_{IH}$ or $V_{IL}$ $V_{I/O} = V_{CC}$ to $V_{EE}$ $I_{I/O} \leq 2\text{ mA}$	GND	4.5	—	85	180	$\Omega$
			-4.5	4.5	—	55	120	
			-6.0	6.0	—	50	100	
		$V_{IN} = V_{IH}$ or $V_{IL}$ $V_{I/O} = V_{CC}$ or $V_{EE}$ $I_{I/O} \leq 2\text{ mA}$	GND	2.0	—	150	—	
			GND	4.5	—	70	150	
			-4.5	4.5	—	50	100	
Difference of ON-resistance between switches	$\Delta R_{ON}$	$V_{IN} = V_{IH}$ or $V_{IL}$ $V_{I/O} = V_{CC}$ to $V_{EE}$ $I_{I/O} \leq 2\text{ mA}$	GND	4.5	—	10	30	$\Omega$
			-4.5	4.5	—	5	12	
			-6.0	6.0	—	5	10	
Input/Output leakage current (Switch OFF)	$I_{OFF}$	$V_{OS} = V_{CC}$ or GND $V_{IS} = \text{GND}$ or $V_{CC}$ $V_{IN} = V_{IH}$ or $V_{IL}$	GND	6.0	—	—	$\pm 0.06$	$\mu\text{A}$
			-6.0	6.0	—	—	$\pm 0.1$	
Input/Output leakage current (Switch ON)	$I_{I/O}$	$V_{OS} = V_{CC}$ or GND $V_{IN} = V_{IH}$ or $V_{IL}$	GND	6.0	—	—	$\pm 0.06$	$\mu\text{A}$
			-6.0	6.0	—	—	$\pm 0.1$	
Control input leakage current	$I_{IN}$	$V_{IN} = V_{CC}$ or GND	GND	6.0	—	—	$\pm 0.1$	$\mu\text{A}$
Quiescent supply current	$I_{CC}$	$V_{IN} = V_{CC}$ or GND	GND	6.0	—	—	4.0	$\mu\text{A}$
			-6.0	6.0	—	—	8.0	

### 12.2. DC Characteristics (Unless otherwise specified, $T_a = -40$ to $85$ °C)

Characteristics	Symbol	Test Condition	$V_{EE}$ (V)	$V_{CC}$ (V)	Min	Max	Unit
High-level input voltage	$V_{IH}$	—		2.0	1.50	—	V
				4.5	3.15	—	
				6.0	4.20	—	
Low-level input voltage	$V_{IL}$	—		2.0	—	0.50	V
				4.5	—	1.35	
				6.0	—	1.80	
ON-resistance	$R_{ON}$	$V_{IN} = V_{IH}$ or $V_{IL}$ $V_{I/O} = V_{CC}$ to $V_{EE}$ $I_{I/O} \leq 2$ mA	GND	4.5	—	225	$\Omega$
			-4.5	4.5	—	150	
			-6.0	6.0	—	125	
		$V_{IN} = V_{IH}$ or $V_{IL}$ $V_{I/O} = V_{CC}$ or $V_{EE}$ $I_{I/O} \leq 2$ mA	GND	4.5	—	190	
			-4.5	4.5	—	125	
			-6.0	6.0	—	100	
Difference of ON-resistance between switches	$\Delta R_{ON}$	$V_{IN} = V_{IH}$ or $V_{IL}$ $V_{I/O} = V_{CC}$ to $V_{EE}$ $I_{I/O} \leq 2$ mA	GND	4.5	—	35	$\Omega$
			-4.5	4.5	—	15	
			-6.0	6.0	—	12	
Input/Output leakage current (Switch OFF)	$I_{OFF}$	$V_{OS} = V_{CC}$ or GND $V_{IS} =$ GND or $V_{CC}$ $V_{IN} = V_{IH}$ or $V_{IL}$	GND	6.0	—	$\pm 0.6$	$\mu A$
			-6.0	6.0	—	$\pm 1.0$	
Input/Output leakage current (Switch ON)	$I_{I/O}$	$V_{OS} = V_{CC}$ or GND $V_{IN} = V_{IH}$ or $V_{IL}$	GND	6.0	—	$\pm 0.6$	$\mu A$
			-6.0	6.0	—	$\pm 1.0$	$\mu A$
Control input leakage current	$I_{IN}$	$V_{IN} = V_{CC}$ or GND	GND	6.0	—	$\pm 1.0$	$\mu A$
Quiescent supply current	$I_{CC}$	$V_{IN} = V_{CC}$ or GND	GND	6.0	—	40.0	$\mu A$
			-6.0	6.0	—	80.0	

### 12.3. DC Characteristics (Unless otherwise specified, $T_a = -40$ to $125$ °C)

Characteristics	Symbol	Test Condition	$V_{EE}$ (V)	$V_{CC}$ (V)	Min	Max	Unit
High-level input voltage	$V_{IH}$	—		2.0	1.50	—	V
				4.5	3.15	—	
				6.0	4.20	—	
Low-level input voltage	$V_{IL}$	—		2.0	—	0.50	V
				4.5	—	1.35	
				6.0	—	1.80	
ON-resistance	$R_{ON}$	$V_{IN} = V_{IH}$ or $V_{IL}$ $V_{I/O} = V_{CC}$ to $V_{EE}$ $I_{I/O} \leq 2$ mA	GND	4.5	—	255	$\Omega$
			-4.5	4.5	—	170	
			-6.0	6.0	—	145	
		$V_{IN} = V_{IH}$ or $V_{IL}$ $V_{I/O} = V_{CC}$ or $V_{EE}$ $I_{I/O} \leq 2$ mA	GND	4.5	—	220	
			-4.5	4.5	—	145	
			-6.0	6.0	—	115	
Difference of ON-resistance between switches	$\Delta R_{ON}$	$V_{IN} = V_{IH}$ or $V_{IL}$ $V_{I/O} = V_{CC}$ to $V_{EE}$ $I_{I/O} \leq 2$ mA	GND	4.5	—	35	$\Omega$
			-4.5	4.5	—	15	
			-6.0	6.0	—	12	
Input/Output leakage current (Switch OFF)	$I_{OFF}$	$V_{OS} = V_{CC}$ or GND $V_{IS} =$ GND or $V_{CC}$ $V_{IN} = V_{IL}$	GND	6.0	—	$\pm 3.0$	$\mu A$
			-6.0	6.0	—	$\pm 5.0$	
Input/Output leakage current (Switch ON)	$I_{I/O}$	$V_{OS} = V_{CC}$ or GND $V_{IN} = V_{IH}$ or $V_{IL}$	GND	6.0	—	$\pm 3.0$	$\mu A$
			-6.0	6.0	—	$\pm 5.0$	$\mu A$
Control input leakage current	$I_{IN}$	$V_{IN} = V_{CC}$ or GND	GND	6.0	—	$\pm 1.0$	$\mu A$
Quiescent supply current	$I_{CC}$	$V_{IN} = V_{CC}$ or GND	GND	6.0	—	80.0	$\mu A$
			-6.0	6.0	—	160.0	

### 12.4. AC Characteristics

(Unless otherwise specified,  $C_L = 50 \text{ pF}$ ,  $T_a = 25 \text{ }^\circ\text{C}$ , Input:  $t_r = t_f = 6 \text{ ns}$ )

Characteristics	Part Number	Symbol	Test Condition	$V_{EE}$ (V)	$V_{CC}$ (V)	Min	Typ.	Max	Unit	
Phase difference between input to output		$\varphi_{I/O}$	—	GND	2.0	—	18	25	ns	
				GND	4.5	—	7	12		
				GND	6.0	—	6	10		
				-4.5	4.5	—	5	8		
Output enable time	74HC4051FT	$t_{PZL}, t_{PZH}$	$R_L = 1 \text{ k}\Omega$ Figure 1	GND	2.0	—	90	145	ns	
				GND	4.5	—	30	45		
				GND	6.0	—	25	35		
				-4.5	4.5	—	24	34		
	74HC4052FT			GND	2.0	—	90	145		ns
				GND	4.5	—	30	45		
				GND	6.0	—	25	35		
				-4.5	4.5	—	24	34		
Output disable time	74HC4051FT	$t_{PLZ}, t_{PHZ}$	$R_L = 1 \text{ k}\Omega$ Figure 1	GND	2.0	—	56	85	ns	
				GND	4.5	—	26	35		
				GND	6.0	—	25	33		
				-4.5	4.5	—	24	32		
	74HC4052FT			GND	2.0	—	56	85		ns
				GND	4.5	—	26	35		
				GND	6.0	—	25	33		
				-4.5	4.5	—	24	32		
Control input capacitance		$C_{IN}$	—	—	—	5	10	pF		
Common terminal capacitance	74HC4051FT	$C_{IS}$	Figure 2	-5.0	5.0	—	36	70	pF	
	74HC4052FT					—	19	40		
Switch terminal capacitance	74HC4051FT	$C_{OS}$	Figure 2	-5.0	5.0	—	7	15	pF	
	74HC4052FT					—	7	15		
Feedthrough capacitance	74HC4051FT	$C_{IOS}$	Figure 2	-5.0	5.0	—	0.95	2	pF	
	74HC4052FT					—	0.85	2		
Power dissipation capacitance	74HC4051FT	$C_{PD}$	Figure 2 (Note 1)	-5.0	5.0	—	11	—	pF	
	74HC4052FT					—	19	—		

Note 1:  $C_{PD}$  is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation.

$$I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}$$

### 12.5. AC Characteristics

(Unless otherwise specified,  $C_L = 50 \text{ pF}$ ,  $T_a = -40 \text{ to } 85 \text{ }^\circ\text{C}$ , Input:  $t_r = t_f = 6 \text{ ns}$ )

Characteristics	Part Number	Symbol	Test Condition	$V_{EE}$ (V)	$V_{CC}$ (V)	Min	Max	Unit
Phase difference between input to output		$\varphi_{I/O}$	—	GND	2.0	—	30	ns
				GND	4.5	—	15	
				GND	6.0	—	13	
				-4.5	4.5	—	10	
Output enable time	74HC4051FT	$t_{PZL}, t_{PZH}$	$R_L = 1 \text{ k}\Omega$ Figure 1	GND	2.0	—	150	ns
				GND	4.5	—	55	
				GND	6.0	—	42	
				-4.5	4.5	—	41	
	74HC4052FT		$R_L = 1 \text{ k}\Omega$ Figure 1	GND	2.0	—	150	
				GND	4.5	—	55	
				GND	6.0	—	42	
				-4.5	4.5	—	41	
Output disable time	74HC4051FT	$t_{PLZ}, t_{PHZ}$	$R_L = 1 \text{ k}\Omega$ Figure 1	GND	2.0	—	90	ns
				GND	4.5	—	45	
				GND	6.0	—	40	
				-4.5	4.5	—	39	
	74HC4052FT		$R_L = 1 \text{ k}\Omega$ Figure 1	GND	2.0	—	90	
				GND	4.5	—	45	
				GND	6.0	—	40	
				-4.5	4.5	—	39	
Control input capacitance		$C_{IN}$	—	—	—	10	pF	
Common terminal capacitance	74HC4051FT	$C_{IS}$	Figure 2	-5.0	5.0	—	70	pF
	74HC4052FT					—	40	
Switch terminal capacitance	74HC4051FT	$C_{OS}$	Figure 2	-5.0	5.0	—	15	pF
	74HC4052FT					—	15	
Feedthrough capacitance	74HC4051FT	$C_{IOS}$	Figure 2	-5.0	5.0	—	2	pF
	74HC4052FT					—	2	

### 12.6. AC Characteristics

(Unless otherwise specified,  $C_L = 50 \text{ pF}$ ,  $T_a = -40 \text{ to } 125 \text{ }^\circ\text{C}$ , Input:  $t_r = t_f = 6 \text{ ns}$ )

Characteristics	Part Number	Symbol	Test Condition	$V_{EE}$ (V)	$V_{CC}$ (V)	Min	Max	Unit
Phase difference between input to output		$\varphi_{I/O}$	—	GND	2.0	—	35	ns
				GND	4.5	—	17	
				GND	6.0	—	15	
				-4.5	4.5	—	12	
Output enable time	74HC4051FT	$t_{PZL}, t_{PZH}$	$R_L = 1 \text{ k}\Omega$ Figure 1	GND	2.0	—	155	ns
				GND	4.5	—	62	
				GND	6.0	—	47	
				-4.5	4.5	—	46	
	74HC4052FT		$R_L = 1 \text{ k}\Omega$ Figure 1	GND	2.0	—	155	
				GND	4.5	—	62	
				GND	6.0	—	47	
				-4.5	4.5	—	46	
Output disable time	74HC4051FT	$t_{PLZ}, t_{PHZ}$	$R_L = 1 \text{ k}\Omega$ Figure 1	GND	2.0	—	95	ns
				GND	4.5	—	52	
				GND	6.0	—	45	
				-4.5	4.5	—	44	
	74HC4052FT		$R_L = 1 \text{ k}\Omega$ Figure 1	GND	2.0	—	95	
				GND	4.5	—	52	
				GND	6.0	—	45	
				-4.5	4.5	—	44	
Control input capacitance		$C_{IN}$	—	—	—	10	pF	
Common terminal capacitance	74HC4051FT	$C_{IS}$	Figure 2	-5.0	5.0	—	70	pF
	74HC4052FT					—	40	
Switch terminal capacitance	74HC4051FT	$C_{OS}$	Figure 2	-5.0	5.0	—	15	pF
	74HC4052FT					—	15	
Feedthrough capacitance	74HC4051FT	$C_{IOS}$	Figure 2	-5.0	5.0	—	2	pF
	74HC4052FT					—	2	

### 12.7. Analog Switch Characteristics ( $T_a = 25\text{ }^\circ\text{C}$ ) (Note)

Characteristics	Part Number	Symbol	Test Condition	$V_{EE}$ (V)	$V_{CC}$ (V)	Typ.	Unit		
Sine Wave Distortion		THD	$R_L = 10\text{ k}\Omega$ , $C_L = 50\text{ pF}$ $f_{IN} = 1\text{ kHz}$	$V_{IN} = 4.0\text{ V}_{p-p}$	-2.25	2.25	0.025	%	
				$V_{IN} = 8.0\text{ V}_{p-p}$	-4.5	4.5	0.020		
				$V_{IN} = 11.0\text{ V}_{p-p}$	-6.0	6.0	0.018		
Maximum frequency response		$f_{MAX(I/O)}$	Adjust $f_{IN}$ voltage to obtain 0 dBm at $V_{OS}$ Increase $f_{IN}$ frequency until dB meter reads -3 dB $R_L = 50\text{ }\Omega$ , $C_L = 10\text{ pF}$ $f_{IN} = 1\text{ MHz}$ , sine wave Figure 3	(Note 1)	-2.3	2.3	120	MHz	
	(Note 2)			45					
						70			
	74HC4051FT				(Note 1)	-4.5	4.5		190
	74HC4052FT				(Note 2)				70
							110		
	74HC4051FT				(Note 1)	-6.0	6.0		200
	74HC4052FT				(Note 2)				85
				140					
Feed through attenuation (switch OFF)		FTH	$V_{IN}$ is centered at $(V_{CC}/2)$ . Adjust input for 0 dBm. $R_L = 600\text{ }\Omega$ , $C_L = 50\text{ pF}$ , $f_{IN} = 1\text{ MHz}$ , sine wave Figure 4	-2.25	2.25	-50	dB		
				-4.5	4.5	-50			
				-6.0	6.0	-50			
Crosstalk (control input to signal output)		$X_{talk}$	$R_L = 600\text{ }\Omega$ , $C_L = 50\text{ pF}$ , $f_{IN} = 1\text{ MHz}$ , square wave ( $t_r = t_f = 6\text{ ns}$ ) Figure 5	-2.25	2.25	60	mV		
				-4.5	4.5	140			
				-6.0	6.0	200			
Crosstalk (between any switches)		$X_{talk}$	Adjust $V_{IN}$ to obtain 0 dBm at input. $R_L = 600\text{ }\Omega$ , $C_L = 50\text{ pF}$ , $f_{IN} = 1\text{ MHz}$ , sine wave Figure 6	-2.25	2.25	-50	dB		
				-4.5	4.5	-50			
				-6.0	6.0	-50			

Note: These characteristics are determined by design of devices.

Note 1: Input COMMON terminal, and measured at SWITCH terminal.

Note 2: Input SWITCH terminal, and measured at COMMON terminal.

### 13. AC Test Circuit

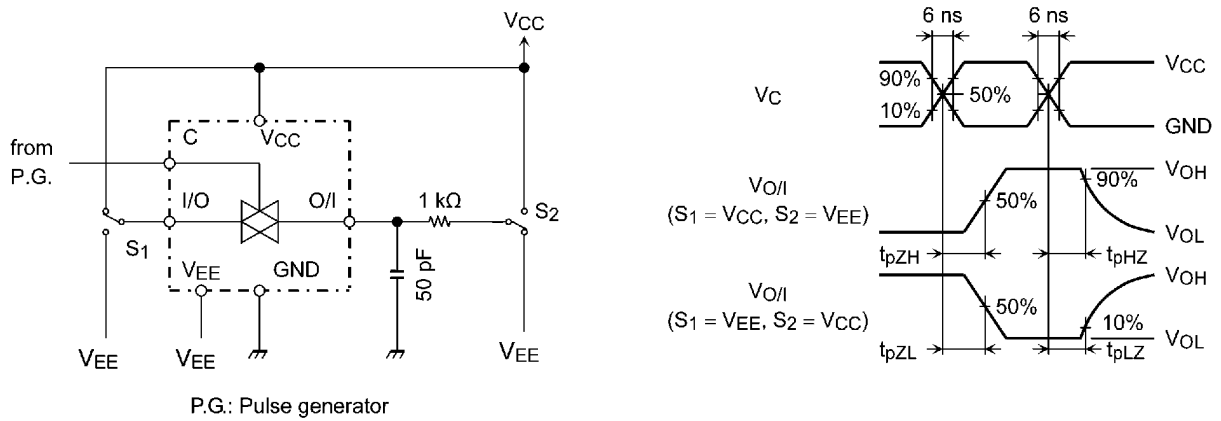


Figure 1  $t_{pLZ}$ ,  $t_{pHZ}$ ,  $t_{pZL}$ ,  $t_{pZH}$

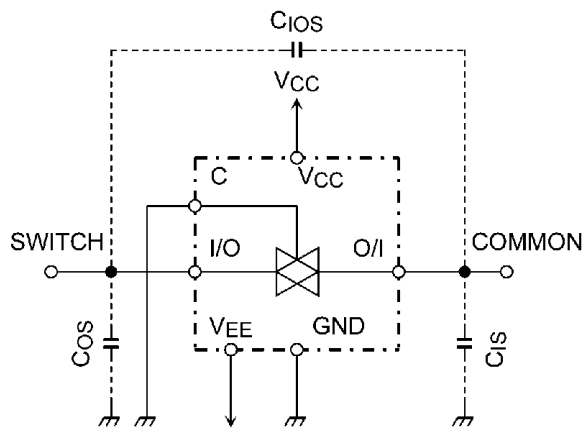


Figure 2  $C_{ios}$ ,  $C_{is}$ ,  $C_{os}$

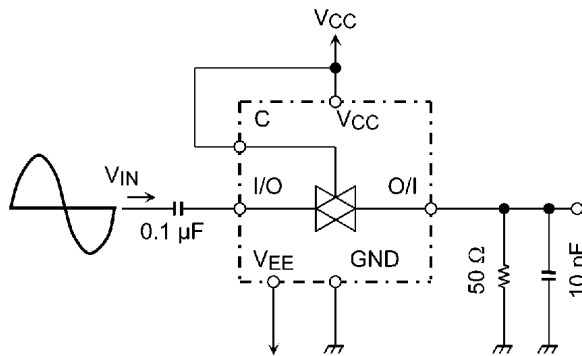


Figure 3 Frequency Response

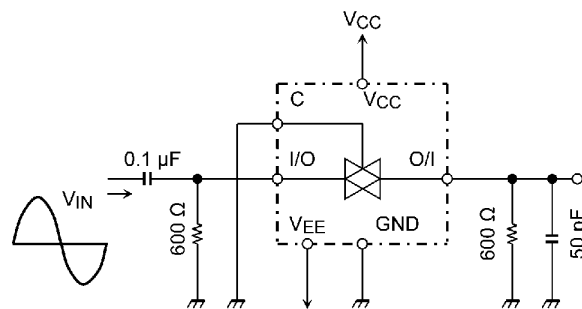
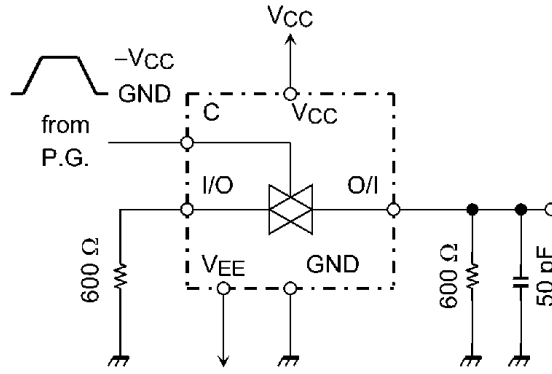
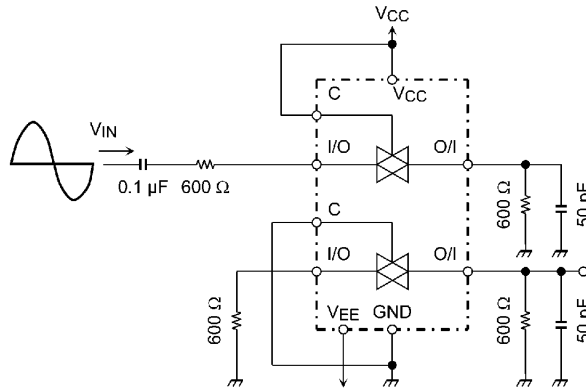


Figure 4 Feedthrough Attenuation



P.G.: Pulse generator

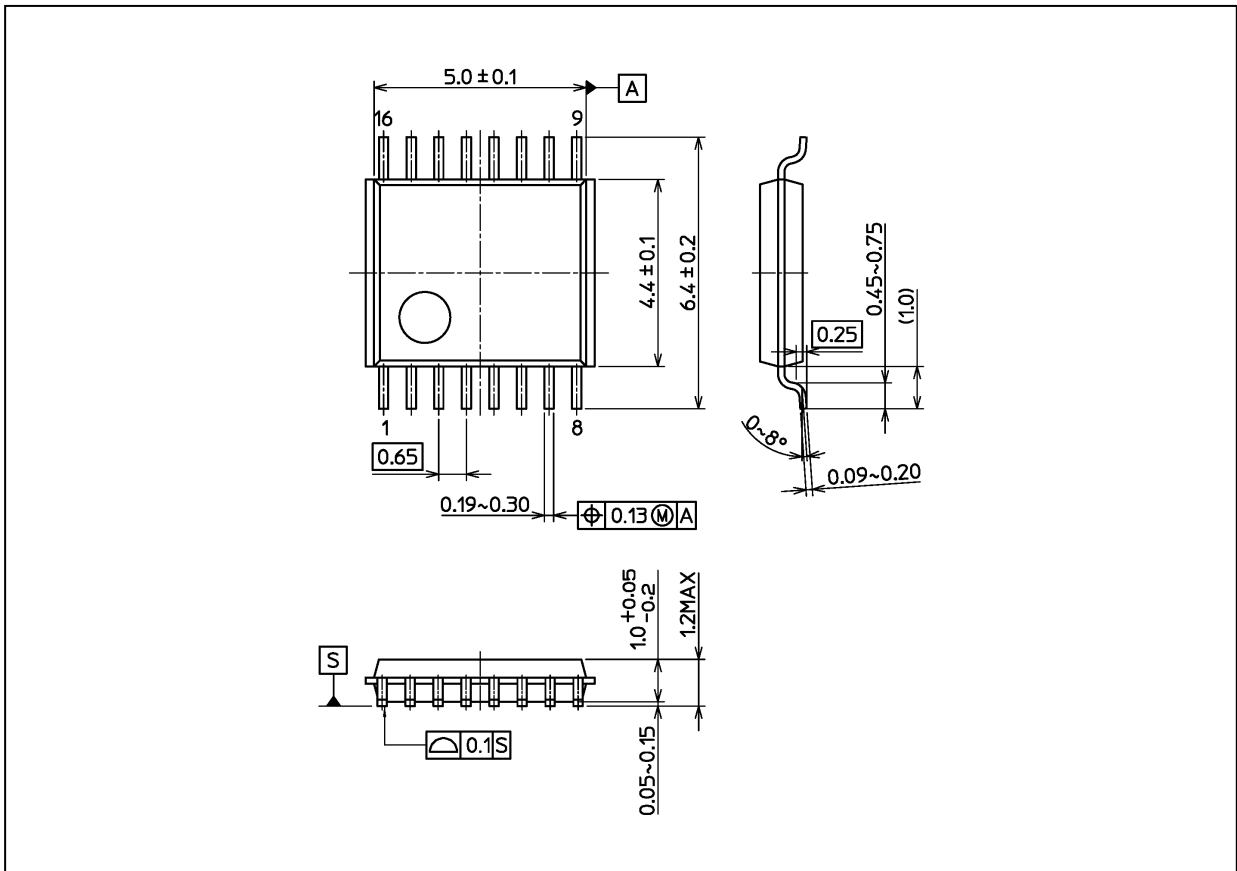
**Figure 5 Cross Talk (control input to output signal)**



**Figure 6 Cross Talk (between any two switches)**

## Package Dimensions

Unit: mm



Weight: 0.055 g (typ.)

Package Name(s)
Nickname: TSSOP16B

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