CMOS Digital Integrated Circuits Silicon Monolithic

TC74LCXR164245

1. Functional Description

- 16-Bit Dual Supply Bus Transceiver with Series Resistor

2. General

The TC74LCXR164245 is a dual supply, advanced high-speed CMOS 16-bit dual supply voltage interface bus transceiver fabricated with silicon gate CMOS technology.

Designed for use as an interface between a 5 V bus and a 3.3 V or 2.5 V bus in mixed 5 V/3.3 V or 2.5 V supply systems, it achieves high-speed operation while maintaining the CMOS low power dissipation.

It is intended for 2 way asynchronous communication between data busses. The direction of data transmission is determined by the level of the DIR input. The enable input ($\overline{OE}$) can be used to disable the device so that the buses are effectively isolated. The B-port interfaces with the 5 V bus, the A-port with the 3.3 V or 2.5 V bus.

The 26 Ω series resistor helps reducing output overshoot and undershoot without external resistor.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

3. Features (Note)

(1) Bidirectional interface between 5 V and 3.3 V or 2.5 V buses

(2) Wide operating temperature range: T_{opr} = -40 to 125 °C (Note 1)

(3) 26 Ω series resistors on outputs

(4) High-speed operation: t_{pd} = 6.8 ns (max) (V_{CCB} = 5.0±0.5 V, V_{CCA} = 3.3±0.3 V, T_a = -40 to 85 °C)

(5) Low power dissipation: I_{CC} = 80 μA (max) at T_a = -40 to 85 °C

(6) Output current: I_{OUTA} = ±12 mA (min)
I_{OUTB} = ±12 mA (min)
(V_{CCA} = 3.0 V / V_{CCB} = 4.5 V)

(7) Power-down protection provided on all inputs and outputs

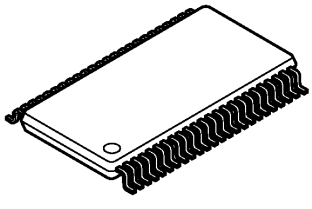
(8) Allows A port and V_{CCA} to float simultaneously in high state at $\overline{OE}$ pin

(9) Package: TSSOP

Note: Do not apply a signal to any bus pins when it is in the output mode. Damage may result.
All floating (high impedance) bus pins must have their input levels fixed by means of pull-up or pull-down resistors.

Note 1: For devices with the ordering part number ending in KF. T_{opr} = -40 °C to 85 °C for the other devices.

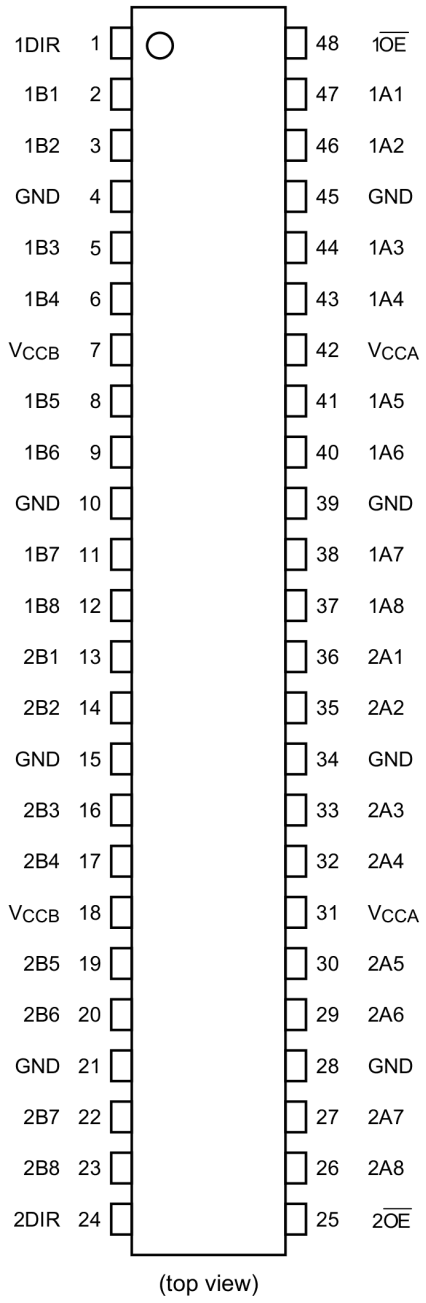
4. Packaging



TSSOP48

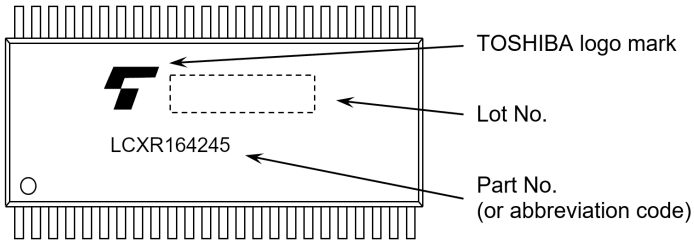
Start of commercial production
2020-01

5. Pin Assignment

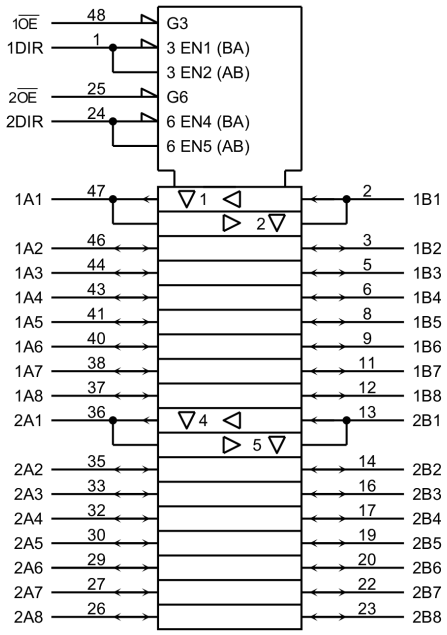


(top view)

6. Marking



7. IEC Logic Symbol

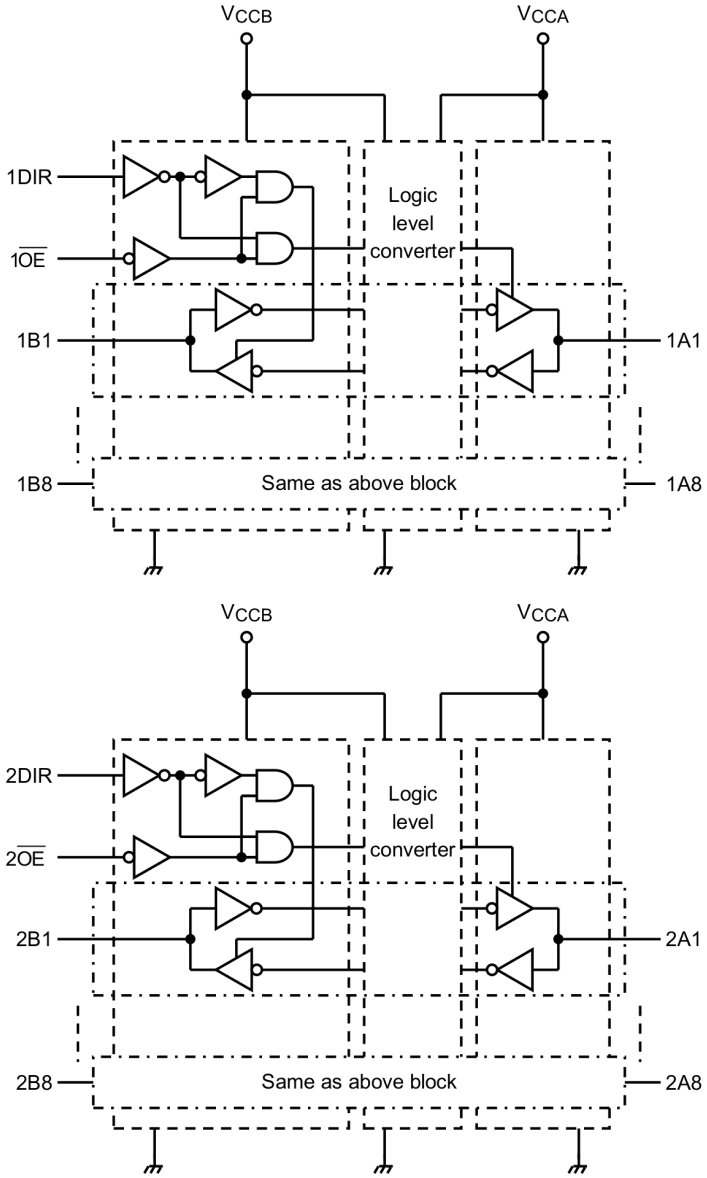


8. Truth Table

Inputs 1$\overline{OE}$ 2$\overline{OE}$	Inputs 1DIR 2DIR	Outputs	Function Bus 1A1-1A8 Bus 2A1-2A8	Function Bus 1B1-1B8 Bus 2B1-2B8
L	L	A = B	Output	Input
L	H	B = A	Input	Output
H	X	Z	Z	Z

X: Don't care
Z: High impedance

9. System Diagram



10. Absolute Maximum Ratings (Note)

Characteristics	Symbol	Note	Rating	Unit
Supply voltage	V_{CCB}	(Note 1)	-0.5 to 7.0	V
	V_{CCA}		-0.5 to V_{CCB} + 0.5	
Input voltage (DIR/$\overline{OE}$)	V_{IN}		-0.5 to 7.0	V
Bus I/O voltage	$V_{I/OB}$	(Note 2)	-0.5 to 7.0	V
		(Note 3)	-0.5 to V_{CCB} + 0.5	
	$V_{I/OA}$	(Note 2)	-0.5 to 7.0	
		(Note 3)	-0.5 to V_{CCA} + 0.5	
Input diode current	I_{IK}		-50	mA
I/O diode current	$I_{I/OK}$	(Note 4)	±50	mA
Output current	I_{OUTB}		±50	mA
	I_{OUTA}		±50	
Power dissipation	P_D	(Note 5)	400	mW
V_{CC}/ground current per supply pin	I_{CCB}		±100	mA
	I_{CCA}		±100	
Storage temperature	T_{stg}		-65 to 150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Don't supply a voltage to V_{CCA} terminal when V_{CCB} is in the off-state.

Note 2: Output in OFF state.

Note 3: High (H) or Low (L) state. I_{OUT} absolute maximum rating must be observed.

Note 4: V_{OUT} < GND, V_{OUT} > V_{CC}

Note 5: 400 mW in the range of Ta = -40 to 85 °C. From Ta = 85 to 125 °C a derating factor of -6.25 mW/°C shall be applied until 150 mW.

11. Operating Ranges (Note)

Characteristics	Symbol	Note	Rating	Unit
Supply voltage	V_{CCB}		4.5 to 5.5	V
	V_{CCA}		2.3 to 3.6	
Input voltage (DIR/$\overline{OE}$)	V_{IN}		0 to 5.5	V
Bus I/O voltage	$V_{I/OB}$	(Note 1)	0 to 5.5	V
		(Note 2)	0 to V_{CCB}	
	$V_{I/OA}$	(Note 1)	0 to 5.5	
		(Note 2)	0 to V_{CCA}	
Output current	I_{OUTB}	(Note 3)	±12	mA
	I_{OUTA}	(Note 4)	±12	
		(Note 5)	±4	
Operating temperature	T_{opr}	(Note 6)	-40 to 125	°C
Input rise and fall times	dt/dv	(Note 7)	0 to 10	ns/V

Note: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs and bus inputs must be tied to either V_{CC} or GND. Please connect both bus inputs and the bus outputs with V_{CC} or GND when the I/O of the bus terminal changes by the function. In this case, please note that the output is not short-circuited.

Note 1: Output in OFF state.

Note 2: High (H) or Low (L) state.

Note 3: V_{CCB} = 4.5 to 5.5 V

Note 4: V_{CCB} = 3.0 to 3.6 V

Note 5: V_{CCA} = 2.3 to 2.7 V

Note 6: For devices with the ordering part number ending in KF. T_{opr} = -40 °C to 85 °C for the other devices.

Note 7: V_{INB} = 0.8 to 2.0 V , V_{CCB} = 5.0 V
V_{INA} = 0.8 to 2.0 V , V_{CCA} = 3.0 V

12. Electrical Characteristics

12.1. DC Characteristics (Unless otherwise specified, T_a = -40 to 85 °C)

Characteristics	Symbol	Test Condition		V_{CCB} (V)	V_{CCA} (V)	Min	Max	Unit
High-level input voltage	V_{IHB}	DIR, $\overline{OE}$, Bn		5.0 ± 0.5	2.3 to 3.6	2.0	—	V
	V_{IHA}	An		5.0 ± 0.5	2.5 ± 0.2	1.7	—	
				5.0 ± 0.5	3.3 ± 0.3	2.0	—	
Low-level input voltage	V_{ILB}	DIR, $\overline{OE}$, Bn		5.0 ± 0.5	2.3 to 3.6	—	0.8	V
	V_{ILA}	An		5.0 ± 0.5	2.5 ± 0.2	—	0.7	
				5.0 ± 0.5	3.3 ± 0.3	—	0.8	
High-level output voltage	V_{OHB}	V_{INA} = V_{IHA} or V_{ILA} V_{INB} = V_{IHB} or V_{ILB}	I_{OHB} = -100 μA	5.0 ± 0.5	2.3 to 3.6	V_{CCB} - 0.2	—	V
			I_{OHB} = -12 mA	4.5	2.3 to 3.6	3.7	—	
	V_{OHA}		I_{OHA} = -100 μA	5.0 ± 0.5	2.3 to 3.6	V_{CCA} - 0.2	—	
			I_{OHA} = -12 mA	5.0 ± 0.5	3.0	2.2	—	
			I_{OHA} = -4 mA	5.0 ± 0.5	2.3	1.8	—	
Low-level output voltage	V_{OLB}	V_{INA} = V_{IHA} or V_{ILA} V_{INB} = V_{IHB} or V_{ILB}	I_{OLB} = 100 μA	5.0 ± 0.5	2.3 to 3.6	—	0.2	V
			I_{OLB} = 12 mA	4.5	2.3 to 3.6	—	0.7	
	V_{OLA}		I_{OLA} = 100 μA	5.0 ± 0.5	2.3 to 3.6	—	0.2	
			I_{OLA} = 12 mA	5.0 ± 0.5	3.0	—	0.8	
			I_{OLA} = 4 mA	5.0 ± 0.5	2.3	—	0.6	
3-state output OFF-state leakage current	I_{OZB}	V_{IN} = V_{IHB} or V_{ILB} $V_{I/OB}$ = 0 to 5.5 V		5.0 ± 0.5	2.3 to 3.6	—	±5.0	μA
	I_{OZA}	V_{IN} = V_{IHB} or V_{ILB} $V_{I/OA}$ = 0 to 5.5 V		5.0 ± 0.5	2.3 to 3.6	—	±5.0	
Input leakage current	I_{IN}	V_{IN} (DIR, $\overline{OE}$) = 0 to 5.5 V		5.5	3.6	—	±5.0	μA
Power-OFF leakage current	I_{OFF}	V_{INA}/V_{INB} = 5.5 V		0	0	—	10	μA
Quiescent supply current	I_{CCB1}	$V_{I/OA}$ = Open, V_{CCA} = Open V_{INB} = V_{CCB} or GND $\overline{OE}$ = V_{CCB}, DIR = GND		5.5	Open	—	80	μA
	I_{CCB2}	V_{INA} = V_{CCA} or GND V_{INB} = V_{CCB} or GND		5.5	3.6	—	80	
	I_{CCA}	V_{INA} = V_{CCA} or GND V_{INB} = V_{CCB} or GND		5.5	3.6	—	50	
	I_{CCTB}	V_{INB} = 3.4 V (per input)		5.5	2.3 to 3.6	—	2.0	mA
	I_{CCTA}	V_{INA} = V_{CCA} - 0.6 V (per input)		5.0 ± 0.5	3.6	—	500	μA

12.2. DC Characteristics (Note) (Unless otherwise specified, T_a = -40 to 125 °C)

Characteristics	Symbol	Test Condition		V_{CCB} (V)	V_{CCA} (V)	Min	Max	Unit
High-level input voltage	V_{IHB}	DIR, $\overline{OE}$, Bn		5.0 ± 0.5	2.3 to 3.6	2.0	—	V
	V_{IHA}	An		5.0 ± 0.5	2.5 ± 0.2	1.7	—	
				5.0 ± 0.5	3.3 ± 0.3	2.0	—	
Low-level input voltage	V_{ILB}	DIR, $\overline{OE}$, Bn		5.0 ± 0.5	2.3 to 3.6	—	0.8	V
	V_{ILA}	An		5.0 ± 0.5	2.5 ± 0.2	—	0.7	
				5.0 ± 0.5	3.3 ± 0.3	—	0.8	
High-level output voltage	V_{OHB}	V_{INA} = V_{IHA} or V_{ILA} V_{INB} = V_{IHB} or V_{ILB}	I_{OHB} = -100 μA	5.0 ± 0.5	2.3 to 3.6	V_{CCB} - 0.2	—	V
			I_{OHB} = -12 mA	4.5	2.3 to 3.6	3.3	—	
	V_{OHA}		I_{OHA} = -100 μA	5.0 ± 0.5	2.3 to 3.6	V_{CCA} - 0.2	—	
			I_{OHA} = -12 mA	5.0 ± 0.5	3.0	1.9	—	
			I_{OHA} = -4 mA	5.0 ± 0.5	2.3	1.55	—	
Low-level output voltage	V_{OLB}	V_{INA} = V_{IHA} or V_{ILA} V_{INB} = V_{IHB} or V_{ILB}	I_{OLB} = 100 μA	5.0 ± 0.5	2.3 to 3.6	—	0.2	V
			I_{OLB} = 12 mA	4.5	2.3 to 3.6	—	0.9	
	V_{OLA}		I_{OLA} = 100 μA	5.0 ± 0.5	2.3 to 3.6	—	0.2	
			I_{OLA} = 12 mA	5.0 ± 0.5	3.0	—	1.1	
			I_{OLA} = 4 mA	5.0 ± 0.5	2.3	—	1.0	
3-state output OFF-state leakage current	I_{OZB}	V_{IN} = V_{IHB} or V_{ILB} $V_{I/OB}$ = 0 to 5.5 V		5.0 ± 0.5	2.3 to 3.6	—	±20.0	μA
	I_{OZA}	V_{IN} = V_{IHB} or V_{ILB} $V_{I/OA}$ = 0 to 5.5 V		5.0 ± 0.5	2.3 to 3.6	—	±20.0	
Input leakage current	I_{IN}	V_{IN} (DIR, $\overline{OE}$) = 0 to 5.5 V		5.5	3.6	—	±20.0	μA
Power-OFF leakage current	I_{OFF}	V_{INA}/V_{INB} = 5.5 V		0	0	—	40	μA
Quiescent supply current	I_{CCB1}	$V_{I/OA}$ = Open, V_{CCA} = Open V_{INB} = V_{CCB} or GND $\overline{OE}$ = V_{CCB}, DIR = GND		5.5	Open	—	320	μA
	I_{CCB2}	V_{INA} = V_{CCA} or GND V_{INB} = V_{CCB} or GND		5.5	3.6	—	320	
	I_{CCA}	V_{INA} = V_{CCA} or GND V_{INB} = V_{CCB} or GND		5.5	3.6	—	200	
	I_{CCTB}	V_{INB} = 3.4 V (per input)		5.5	2.3 to 3.6	—	2.0	mA
	I_{CCTA}	V_{INA} = V_{CCA} - 0.6 V (per input)		5.0 ± 0.5	3.6	—	5.0	mA

Note: For devices with the ordering part number ending in KF. T_{opr} = -40 °C to 85 °C for the other devices.

12.3. AC Characteristics
(Unless otherwise specified, T_a = -40 to 85°C, Input: $t_r = t_f$ = 2.5 ns, R_L = 500 Ω)
V_{CCB} = 3.3 ± 0.3 V

Characteristics	Symbol	Note	Test Condition	C_L (pF)	V_{CCA} (V)	Min	Max	Unit
Propagation delay time (Bn→An)	t_{PLH},t_{PHL}		Input: Bn Output: An (DIR = "L") See 12.8 AC Test Circuit, Table 12.8.1, Fig. 12.9.1, Fig. 12.9.2, Table 12.9.1	50	5.0 ± 0.5	1.0	6.8	ns
3-state output enable time ($\overline{OE}$→An)	t_{PZL},t_{PZH}			50	5.0 ± 0.5	1.0	10.0	
3-state output disable time ($\overline{OE}$→An)	t_{PLZ},t_{PHZ}			50	5.0 ± 0.5	1.0	9.5	
Propagation delay time (An→Bn)	t_{PLH},t_{PHL}		Input: An Output: Bn (DIR = "H") See 12.8 AC Test Circuit, Table 12.8.1, Fig. 12.9.1, Fig. 12.9.2, Table 12.9.1	50	5.0 ± 0.5	1.0	6.8	ns
3-state output enable time ($\overline{OE}$→Bn)	t_{PZL},t_{PZH}			50	5.0 ± 0.5	1.0	10.0	
3-state output disable time ($\overline{OE}$→Bn)	t_{PLZ},t_{PHZ}			50	5.0 ± 0.5	1.0	9.5	
Output skew	t_{osLH},t_{osHL}	(Note 1)	—	50	5.0 ± 0.5	—	1.0	ns

Note 1: Parameter guaranteed by design. (t_{osLH} = $|t_{PLH}m-t_{PLH}n|$, t_{osHL} = $|t_{PHL}m-t_{PHL}n|$)

12.4. AC Characteristics
(Unless otherwise specified, T_a = -40 to 85°C, Input: $t_r = t_f$ = 2.5 ns, R_L = 500 Ω)
V_{CCB} = 2.5 ± 0.2 V

Characteristics	Symbol	Note	Test Condition	C_L (pF)	V_{CC} (V)	Min	Max	Unit
Propagation delay time (Bn→An)	t_{PLH},t_{PHL}		Input: Bn Output: An (DIR = "L") See 12.8 AC Test Circuit, Table 12.8.1, Fig. 12.9.1, Fig. 12.9.2, Table 12.9.1	30	5.5 ± 0.5	1.0	9.0	ns
3-state output enable time ($\overline{OE}$→An)	t_{PZL},t_{PZH}			30	5.5 ± 0.5	1.0	12.5	
3-state output disable time ($\overline{OE}$→An)	t_{PLZ},t_{PHZ}			30	5.5 ± 0.5	1.0	11.5	
Propagation delay time (An→Bn)	t_{PLH},t_{PHL}		Input: An Output: Bn (DIR = "H") See 12.8 AC Test Circuit, Table 12.8.1, Fig. 12.9.1, Fig. 12.9.2, Table 12.9.1	50	5.5 ± 0.5	1.0	10.0	ns
3-state output enable time ($\overline{OE}$→Bn)	t_{PZL},t_{PZH}			50	5.5 ± 0.5	1.0	12.5	
3-state output disable time ($\overline{OE}$→Bn)	t_{PLZ},t_{PHZ}			50	5.5 ± 0.5	1.0	11.5	
Output skew	t_{osLH},t_{osHL}	(Note 1)	—	30 or 50	5.5 ± 0.5	—	1.0	ns

Note 1: Parameter guaranteed by design. (t_{osLH} = $|t_{PLH}m-t_{PLH}n|$, t_{osHL} = $|t_{PHL}m-t_{PHL}n|$)

12.5. AC Characteristics (Note)
(Unless otherwise specified, T_a = -40 to 125 °C, Input: $t_r = t_f$ = 2.5 ns, R_L = 500 Ω)
V_{CCB} = 3.3 ± 0.3 V

Characteristics	Symbol	Note	Test Condition	C_L (pF)	V_{CCA} (V)	Min	Max	Unit
Propagation delay time (Bn→An)	t_{PLH},t_{PHL}		Input: Bn Output: An (DIR = "L") See 12.8 AC Test Circuit, Table 12.8.1, Fig. 12.9.1, Fig. 12.9.2, Table 12.9.1	50	5.5 ± 0.5	1.0	7.3	ns
3-state output enable time ($\overline{OE}$→An)	t_{PZL},t_{PZH}			50	5.5 ± 0.5	1.0	10.7	
3-state output disable time ($\overline{OE}$→An)	t_{PLZ},t_{PHZ}			50	5.5 ± 0.5	1.0	10.2	
Propagation delay time (An→Bn)	t_{PLH},t_{PHL}		Input: An Output: Bn (DIR = "H") See 12.8 AC Test Circuit, Table 12.8.1, Fig. 12.9.1, Fig. 12.9.2, Table 12.9.1	50	5.5 ± 0.5	1.0	7.3	ns
3-state output enable time ($\overline{OE}$→Bn)	t_{PZL},t_{PZH}			50	5.5 ± 0.5	1.0	10.7	
3-state output disable time ($\overline{OE}$→Bn)	t_{PLZ},t_{PHZ}			50	5.5 ± 0.5	1.0	10.2	
Output skew	t_{osLH},t_{osHL}	(Note 1)	—	50	5.5 ± 0.5	—	1.0	ns

Note: For devices with the ordering part number ending in KF. T_{opr} = -40 °C to 85 °C for the other devices.
Note 1: Parameter guaranteed by design. ($t_{osLH} = |t_{PLHm} - t_{PLHn}|$, $t_{osHL} = |t_{PHLm} - t_{PHLn}|$)

12.6. AC Characteristics (Note)
(Unless otherwise specified, T_a = -40 to 125 °C, Input: $t_r = t_f$ = 2.5 ns, R_L = 500 Ω)
V_{CCB} = 2.5 ± 0.2 V

Characteristics	Symbol	Note	Test Condition	C_L (pF)	V_{CCA} (V)	Min	Max	Unit
Propagation delay time (Bn→An)	t_{PLH},t_{PHL}		Input: Bn Output: An (DIR = "L") See 12.8 AC Test Circuit, Table 12.8.1, Fig. 12.9.1, Fig. 12.9.2, Table 12.9.1	30	5.0 ± 0.5	1.0	9.7	ns
3-state output enable time ($\overline{OE}$→An)	t_{PZL},t_{PZH}			30	5.0 ± 0.5	1.0	13.4	
3-state output disable time ($\overline{OE}$→An)	t_{PLZ},t_{PHZ}			30	5.0 ± 0.5	1.0	12.4	
Propagation delay time (An→Bn)	t_{PLH},t_{PHL}		Input: An Output: Bn (DIR = "H") See 12.8 AC Test Circuit, Table 12.8.1, Fig. 12.9.1, Fig. 12.9.2, Table 12.9.1	50	5.0 ± 0.5	1.0	10.7	ns
3-state output enable time ($\overline{OE}$→Bn)	t_{PZL},t_{PZH}			50	5.0 ± 0.5	1.0	13.4	
3-state output disable time ($\overline{OE}$→Bn)	t_{PLZ},t_{PHZ}			50	5.0 ± 0.5	1.0	12.4	
Output skew	t_{osLH},t_{osHL}	(Note 1)	—	30 or 50	5.0 ± 0.5	—	1.0	ns

Note: For devices with the ordering part number ending in KF. T_{opr} = -40 °C to 85 °C for the other devices.
Note 1: Parameter guaranteed by design. ($t_{osLH} = |t_{PLHm} - t_{PLHn}|$, $t_{osHL} = |t_{PHLm} - t_{PHLn}|$)

12.7. Capacitive Characteristics (Unless otherwise specified, T_a = 25°C)
V_{CCB} = 2.5, 3.3 V

Characteristics	Symbol	Note	Test Condition	V_{CCA} (V)	Typ.	Unit
Input capacitance	C_{IN}		DIR, $\overline{OE}$	2.5, 3.3	7	pF
Bus I/O capacitance	$C_{I/O}$		An, Bn	2.5, 3.3	8	pF
Power dissipation capacitance	C_{PDA}	(Note 1)	A→B (DIR = "H")	2.5, 3.3	2	pF
			B→A (DIR = "L")	2.5, 3.3	26	
	C_{PDB}		A→B (DIR = "H")	2.5, 3.3	36	
			B→A (DIR = "L")	2.5, 3.3	4	

Note 1: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation.
$I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/16$ (per bit)

12.8. AC Test Circuit

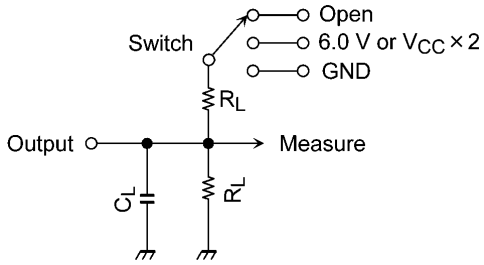


Table 12.8.1 Parameter for AC Test Circuit

Parameter	Switch	Test Condition
t_{PLH}, t_{PHL}	OPEN	—
t_{PLZ}, t_{PZL}	6.0 V	V_{CC} = 3.3 ± 0.3 V
	V_{CC} × 2	V_{CC} = 2.5 ± 0.2 V
t_{PHZ}, t_{PZH}	GND	—

12.9. AC Waveform

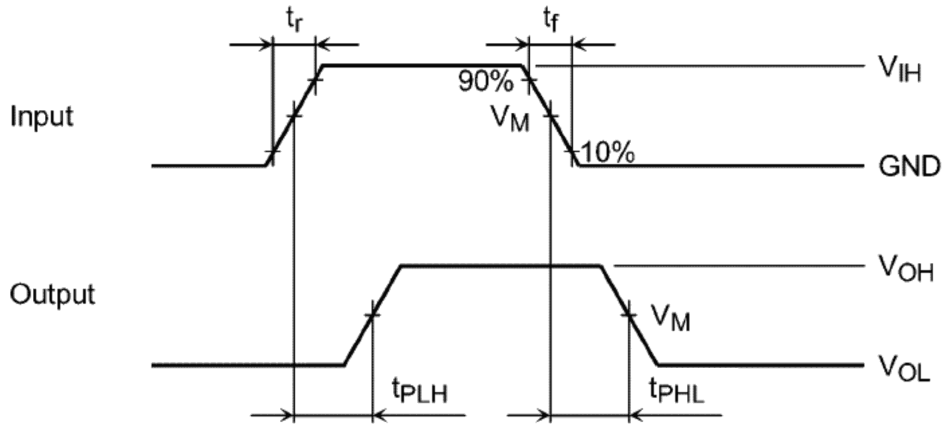


Fig. 12.9.1 t_{PLH}, t_{PHL}

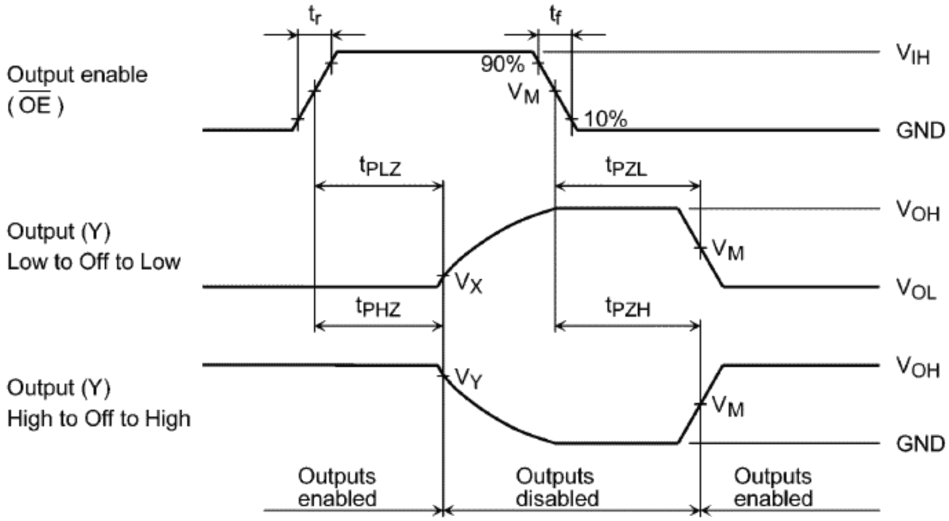


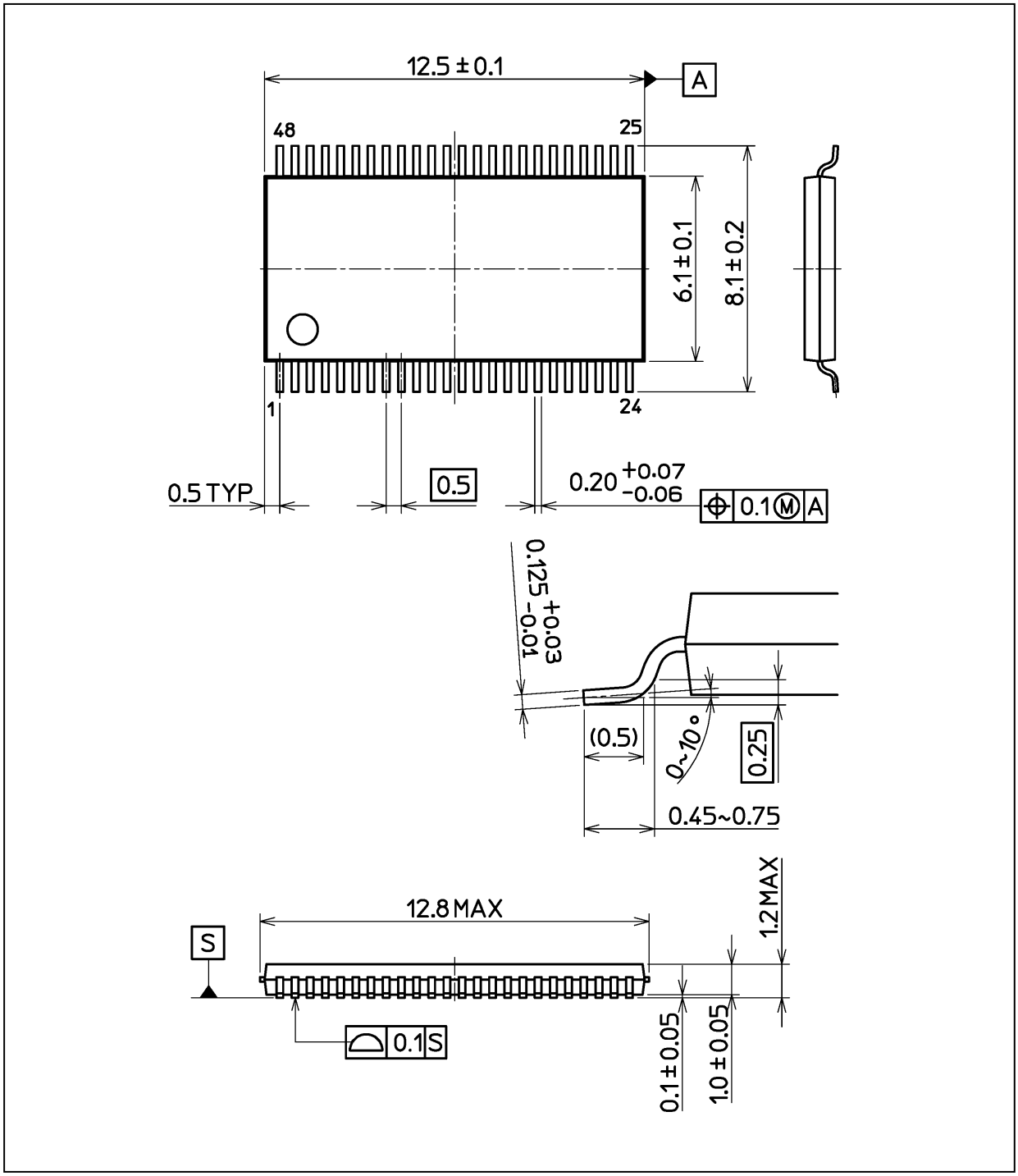
Fig. 12.9.2 t_{PLZ}, t_{PHZ}, t_{PZL}, t_{PZH}

Table 12.9.1 AC Waveform Symbols

Symbol	V_{CC} = 3.3 ± 0.3 V	V_{CC} = 2.7 V	V_{CC} = 2.5 ± 0.2 V
V_{IH}	2.7 V	2.7 V	V_{CC}
V_M	1.5 V	1.5 V	V_{CC}/2
V_X	V_{OL} + 0.3 V	V_{OL} + 0.3 V	V_{OL} + 0.15 V
V_Y	V_{OH} - 0.3 V	V_{OH} - 0.3 V	V_{OH} - 0.15 V
C_L	50 pF	30 pF	30 pF
R_L	500 Ω	500 Ω	500 Ω

Package Dimensions

Unit: mm



Weight: 0.25 g (typ.)

Package Name(s)
Nickname: TSSOP48

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