32-bit RISC Microcontroller

TXZ+ Family
TMPM4K Group(2)

Reference Manual
Clock Control and Operation Mode
(CG-M4K(2)-E)

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Conventions

- Numeric formats follow the rules as shown below:
  Hexadecimal: 0xABC
  Decimal: 123 or 0d123 - Only when it needs to be explicitly shown that they are decimal numbers.
  Binary: 0b111 - It is possible to omit the "0b" when the number of bits can be distinctly understood from a sentence.
- "_N" is added to the end of signal names to indicate low active signals.
- It is called "assert" that a signal moves to its active level, "deassert" to its inactive level.
- When two or more signal names are referred, they are described like as [m:n].
  Example: S[3:0] shows four signal names S3, S2, S1 and S0 together.
- The characters surrounded by ***[ ]*** defines the register.
  Example: ***[ABCD]***
- "N" substitutes suffix number of two or more same kind of registers, fields, and bit names.
  Example: ***[XYZ1]***, ***[XYZ2]***, ***[XYZ3]*** → ***[XYZn]***
- "x" substitutes suffix number or character of units and channels in the register list.
- In case of unit, "x" means A, B, and C, ...
  Example: ***[ADACR0]***, ***[ADBCR0]***, ***[ADCCR0]*** → ***[ADxCR0]***
- In case of channel, "x" means 0, 1, and 2, ...
  Example: ***[T32A0RUNA]***, ***[T32A1RUNA]***, ***[T32A2RUNA]*** → ***[T32AxRUNA]***
- The bit range of a register is written like as [m: n].
  Example: Bit[3: 0] expresses the range of bit 3 to 0.
- The configuration value of a register is expressed by either the hexadecimal number or the binary number.
  Example: ***[ABCD]***<EFG> = 0x01 (hexadecimal), ***[XYZn]***<VW> = 1 (binary)
- Word and byte represent the following bit length.
  Byte: 8 bits
  Half word: 16 bits
  Word: 32 bits
  Double word: 64 bits
- Properties of each bit in a register are expressed as follows:
  R: Read only
  W: Write only
  R/W: Read and write are possible.
- Unless otherwise specified, register access supports only word access.
- The register defined as "Reserved" must not be rewritten. Moreover, do not use the read value.
- The value read from the bit having default value of "-" is unknown.
- When a register containing both of writable bits and read-only bits is written, read-only bits should be written with their default value, In the cases that default is "-", follow the definition of each register.
- Reserved bits of the write-only register should be written with their default value. In the cases that default is "-", follow the definition of each register.
- Do not use read-modified-write processing to the register of a definition which is different by writing and read out.

Terms and Abbreviations

Some of abbreviations used in this document are as follows:

ADC	Analog to Digital Converter
A-ENC32	Advanced Encoder input Circuit (32-bit)
A-PMD	Advanced Programmable Motor Control Circuit
A-VE+	Advanced Vector Engine Plus
CG	Clock Control and Operation Mode
CRC	Cyclic Redundancy Check
D-Bus	DCode memory interface
DMAC	Direct Memory Access Controller
DNF	Digital Noise Filter
EI2C	I^2C Interface Version A
EHOSC	External High-speed Oscillator
fsys	frequency of SYSTEM Clock
IA(INTIF)	Interrupt control register A
IB(INTIF)	Interrupt control register B
I-Bus	ICode memory interface
IHOSC	Internal High-speed Oscillator
IMN	Interrupt Monitor
INT	Interrupt
I2C	Inter-Integrated Circuit
LVD	Voltage Detection Circuit
NBDIF	Non Break Debug Interface
NMI	Non-Maskable Interrupt
OFD	Oscillation Frequency Detector
OPAMP	Operational Amplifier
POR	Power On Reset Circuit
PORF	Power On Reset Circuit for FLASH and debug
RAMP	RAM Parity
RLM	Low speed oscillation / power supply control / reset
S-Bus	System interface
SIWDT	Clock Selective Watchdog Timer
TRGSEL	Trigger Selection Circuit
TRM	Trimming Circuit
TSPI	Serial Peripheral Interface
T32A	32-bit Timer Event Counter
UART	Asynchronous Serial Communication Circuit

1. Clock control and operation mode

1.1. Outlines

The clock/mode control block can select a clock gear and prescaler clock, and set the warming-up of oscillator and so on.

Furthermore, it has Normal mode and a low power consumption mode in order to reduce power consumption using mode transition.

Functions related to a clock are as follows.

- System clock control
- Prescaler clock control

1.2. Clock control

1.2.1. Clock type

This section shows a list of clocks:

EHCLKIN	: The high speed clock input from the external
fosc	: A clock generated in the internal oscillation circuit or input from the X1 and X2 pins after being selected by ***[CGOSCCR]***<OSCSEL>.
f_{PLL}	: A clock multiplied with PLL0
fc	: A clock selected by ***[CGPLL0SEL]***<PLL0SEL> (High speed clock)
fsysh	: A high speed system clock selected by ***[CGSYSCR]***<GEAR[2:0]>
fsysm	: A middle speed system clock selected by ***[CGSYSCR]***<GEAR[2:0]><MCKSEL[1:0]>
ΦT0h	: A high speed clock selected by ***[CGSYSCR]***<PRCK[3:0]> (High speed prescaler clock)
ΦT0m	: A middle speed clock selected by ***[CGSYSCR]***<PRCK[3:0]> <MCKSEL[1:0]> (Middle speed prescaler clock)
f_{IHOSC1}	: A clock generated with the internal high speed oscillator1
f_{IHOSC2}	: A clock generated with the internal high speed oscillator2
ADCLK	: A conversion clock for ADC
TRCLKIN	: A clock for tracing facilities of a debugging circuit (Trace or SWV)

Note: The high speed system clock and the middle speed system clock are collectively called System clock (fsys). And the high speed prescaler clock and the middle speed prescaler clock are collectively called Prescaler clock (ΦT0).

1.2.2. The initial value by a reset action

A clock setup is initialized to the following states by a reset action.

External high speed oscillator	: Stop
Internal high speed oscillator1	: Oscillation
Internal high speed oscillator2	: Stop
PLL (multiplying circuit)	: Stop
Gear clock	: fc (no frequency dividing)

1.2.3. Clock System diagram

The figure below shows a clock system diagram.

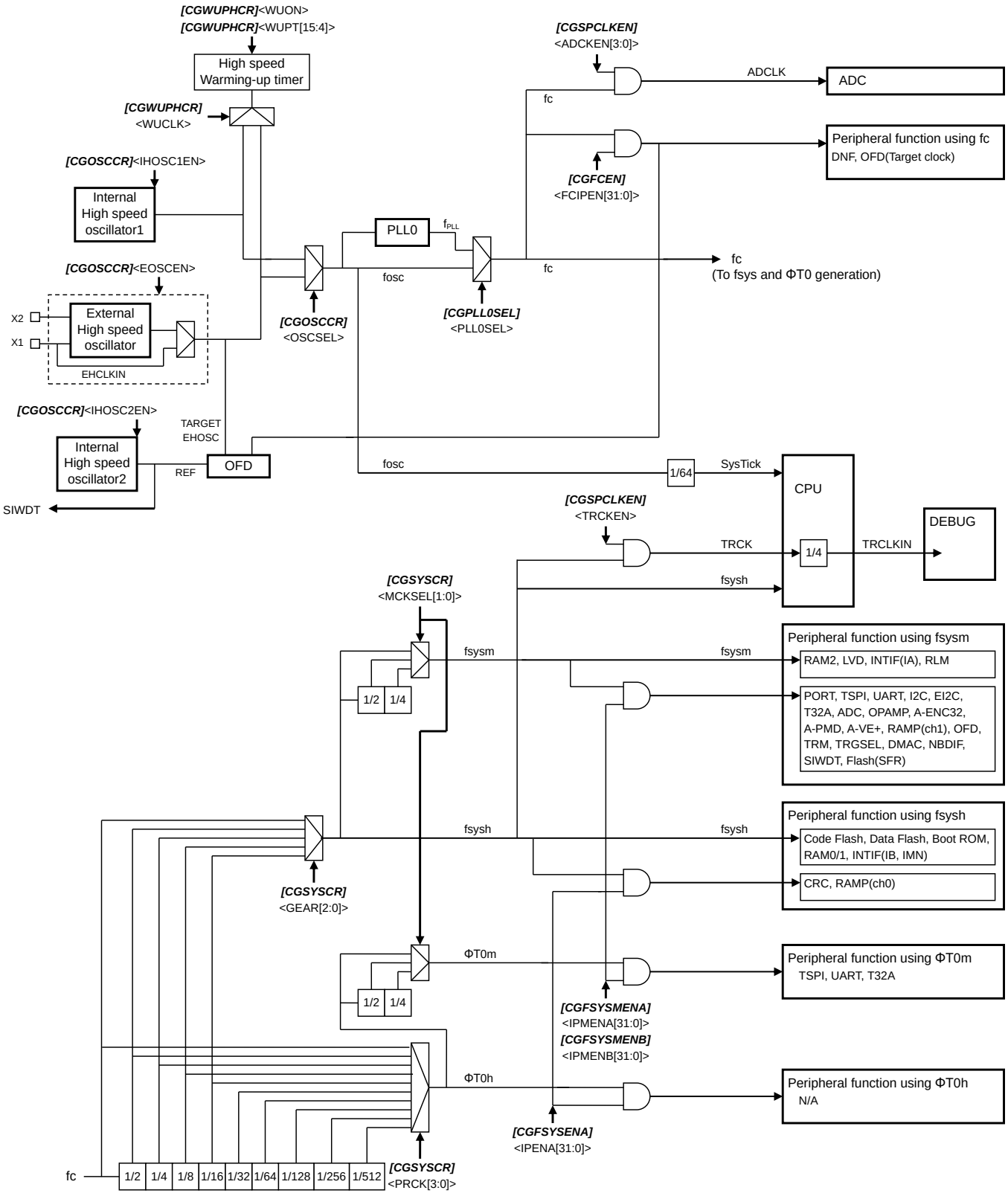

Figure 1.1 Clock system diagram

1.2.4. Warming-up function

A warming-up function starts the warming-up timer for high speed oscillator automatically to secure the oscillation stable time when the STOP1 mode is released.

It is also available as a count-up timer which uses the warming-up timer for high speed oscillator to secure the stability of an external oscillator or an internal oscillator.

This chapter explains the setting method to the register for warming-up timers, and the case where it is used as a count-up timer. The detailed explanation at the time of STOP1 mode release, refer to "1.3.3.2. Warming-up at the release of Low Power Consumption mode".

1.2.4.1. The warming-up timer for a high speed oscillation

A 16-bit up-timer is built in as a warming-up timer only for a high speed oscillation. Also when setting it before changes to the STOP1 mode, calculate with the following formula and set ***[CGWUPHCR]***<WUPT[15:4]> to the upper 12 bits of the result. Lower 4bits are ignored.

<Formula>

(Using external high speed oscillator)

Warming-up timer setting value (16 bits) = (warming-up time (s) / clock period (s)) - 16

(Example) When 5 ms of warming-up time is set up with 10 MHz (100 ns of clock periods) of oscillators

Warming-up timer setting value (16 bits) = (5ms / 100ns) - 16
= 50000 - 16
= 49984
= 0xC340

Since upper 12 bits are used, set the register as follows.

[CGWUPHCR]<WUPT[15:4]> = 0xC34

(Using internal high speed oscillator1)

Warming-up timer setting value (16 bits) = (warming-up time (s) – 63.3(μs)) / clock period (s) - 41

(Example) When 163.4 μs of warming-up time is set up with 10 MHz (100 ns of clock periods) of oscillators

Warming-up timer setting value (16 bits) = ((163.4μs – 63.3μs) / 100ns) - 41
= (100.1μs – 100ns) - 41
= 960
= 0x03C0

Since upper 12 bits are used, set the register as follows.

[CGWUPHCR]<WUPT[15:4]> = 0x03C

The setting range is 0x03C ≤ <WUPT[15:4]> ≤ 0xFFF, warming-up time is set from 163.4 μs to 6.6194 ms.

1.2.4.2. The directions for a warming-up timer

The directions for a warming-up function are explained.

(1) Selection of a clock

In a high speed oscillation, the clock classification (internal oscillation/external oscillation) counted with a warming-up timer is selected by ***[CGWUPHCR]***<WUCLK>.

(2) Calculation of warming-up timer setting value

The warming-up time can set any value to the timer for a high speed oscillation. Please compute and set up from the formula.

(3) The start of warming-up, and a termination Confirmation

When software (command) performs the start of warming-up, starting warming-up count is carried out by setting ***[CGWUPHCR]***<WUON> to "1". Termination is confirmed with ***[CGWUPHCR]***<WUEF> that becomes from "1" to "0". "1" shows that it is warming-up and "0" shows termination. After a counting end, a timer is reset and returns to an initial state.

It is not forced to terminate, although "0" is written to ***[CGWUPHCR]***<WUON> during timer operation. Writing "0" is disregarded.

Note: Since it is operating with the oscillating clock, a warming-up timer includes an error, when Oscillation frequency has fluctuation. Therefore, It serves an approximate time.

1.2.5. Clock multiplying circuit (PLL) for fsys

The clock multiplying circuit outputs the f_{PLL} clock (maximum 160MHz) multiplied by the optimum condition for the frequency (6 MHz to 12 MHz) of the output clock fosc of the high speed oscillator.

So, it is possible to make input frequency to an oscillator low and to make an internal clock high speed by this circuit.

1.2.5.1. A PLL setup after reset release

The PLL is disabled after reset release.

In order to use the PLL, set ***[CGPLL0SEL]***<PLL0SET[23:0]> to a multiplication value while ***[CGPLL0SEL]*** <PLL0ON> is "0". Then wait until approximately 100 µs has elapsed as a PLL initial stabilization time, and set <PLL0ON> to "1" to start PLL operation. After that, to use f_{PLL} clock which is multiplied fosc, wait until approximately 400 µs has elapsed as a lock up time. Then set ***[CGPLL0SEL]***<PLL0SEL> to "1".

Note that a time is required until PLL operation becomes stable using the warming-up function, etc.

1.2.5.2. The formula and the example of a setting of a PLL multiplication value

The details of the items of ***[CGPLL0SEL]***<PLL0SET[23:0]> which set up a PLL multiplication value are shown below.

Table 1.1 Details of *[CGPLL0SEL]*<PLL0SET[23:0]> setup

The items of PLL0SET	Function	
[23:17]	Correction value setup	The quotient of fosc/450000 (integer). For details, refer to Table 1.2.
[16:14]	fosc setup	000: 6 < fosc ≤ 7 (unit: MHz) 001: 7 < fosc ≤ 8 010: 8 < fosc ≤ 10 011: 10 < fosc ≤ 12 100 to 111: Reserved
[13:12]	Dividing setup	00: Reserved 01: Dividing by 2 (×1/2) 10: Dividing by 4 (×1/4) 11: Dividing by 8 (×1/8)
[11:8]	Fraction part Multiplication setup	0000: 0.0000 0001: 0.0625 0010: 0.1250 0011: 0.1875 0100: 0.2500 0101: 0.3125 0110: 0.3750 0111: 0.4375 1000: 0.5000 1001: 0.5625 1010: 0.6250 1011: 0.6875 1100: 0.7500 1101: 0.8125 1110: 0.8750 1111: 0.9375
[7:0]	Integer part Multiplication setup	0x00: 0 0x01: 1 0x02: 2 : 0xFD: 253 0xFE: 254 0xFF: 255

Note: A multiplication value is the total of <PLL0SET[7:0]> (integer part) and <PLL0SET[11:8]> (fraction part).

f_{PLL} is denoted by the following formulas.

f_{PLL} = fosc × (***[CGPLL0SEL]***<PLL0SET[7:0]> + ***[CGPLL0SEL]***<PLL0SET[11:8]>) × (***[CGPLL0SEL]***<PLL0SET[13:12]>)

Note1: The absolute value of frequency accuracy is not guaranteed.

Note2: There is no Linearity in the frequency by the Fraction part Multiplication setup.

Note3: f_{PLL} ≤ (Maximum Operating Frequency)

Table 1.2 PLL correction (example)

fosc (MHz)	<PLL0SET[23:17]> (a decimal, an integral value)
6.00	14
8.00	18
10.00	23
12.00	27

The PLL correction value can be calculated below.

fosc = 10.0 MHz, 10.0/0.45 = 22.22 → 23; A fraction part is rounded up.

The main examples of a setting of ***[CGPLL0SEL]***<PLL0SET[23:0]> are shown below.

It multiplies by PLL, and dividing is carried out and the target Clock frequency (f_{PLL}) is generated for input frequency (fosc).

A dividing value is chosen from 1/2, 1/4, and 1/8.
Moreover, set up the frequency after multiplication in the following ranges.
200 MHz ≤ (fosc × Multiplication value) ≤ 400 MHz

Table 1.3 PLL0SET setting value (example)

fosc (MHz)	Multiplication value	Dividing value	f_{PLL} (MHz)	<PLL0SET[23:0]>
6.00	53.3125	1/2	159.94	0x1C1535
8.00	40.0000	1/2	160	0x245028
10.00	32.0000	1/2	160	0x2E9020
12.00	26.6250	1/2	159.75	0x36DA1A

1.2.5.3. Change of the PLL multiplication value under operation

To change the setting of a PLL multiplication during PLL multiplication clock operation, set ***[CGPLL0SEL]*** <PLL0SEL> to "0" that does not use a PLL multiplication clock. And ***[CGPLL0SEL]***<PLL0ST> =0 is read to confirm that a multiplication clock setting is not used, then, ***[CGPLL0SEL]***<PLL0ON> is set to "0", and PLL is stopped.

Then, the multiplication value of ***[CGPLL0SEL]***<PLL0SET[23:0]> is changed, as reset time of PLL, after about 100 µs has elapsed, ***[CGPLL0SEL]***<PLL0ON> is set to "1", and operation of PLL is started.

Then, ***[CGPLL0SEL]***<PLL0SEL> is set to "1" after lock-up time (about 400µs) has elapsed.

Finally, ***[CGPLL0SEL]***<PLL0ST> is read and it checks having changed.

1.2.5.4. PLL operation start / stop / switching procedure

(1) fc setup (PLL stop >>> PLL start)

As an fc setup, the example of switching procedure from the PLL stop state to the PLL operation state is as follows.

<< The state before switching >>	
[CGPLL0SEL]<PLL0ON> =0	Stops the PLL operation for fsys.
[CGPLL0SEL]<PLL0SEL> =0	Selects the setting of the PLL for fsys to "PLL is unused (fosc)".
[CGPLL0SEL]<PLL0ST> =0	Indicates the status of the PLL for fsys to "PLL is unused (fosc)".
[CGSYSCR]<MCKSEL> =00	Ratios of (High speed system clock vs Middle speed system clock) and (High speed prescaler clock vs Middle speed system clock) are 1:1.

<< The example of switching procedure >>		
1	***[CGSYSCR]***<MCKSEL[1:0]> = 01 or 1*	Ratios of (High speed system clock vs Middle speed system clock) and (High speed prescaler clock vs High speed system clock) are changed.
2	***[CGSYSCR]*** <MCKSELGST> <MCKSELPST> is read	Wait until they become the values set at Step 1.
3	***[CGPLL0SEL]***<PLL0SET[23:0]> =0xX	A PLL multiplication value setup is chosen.
4	Wait 100 µs or more.	Latency time after a multiplication setup
5	***[CGPLL0SEL]***<PLL0ON> =1	PLL operation for fsys is carried out to an oscillation.
6	Wait 400 µs or more.	PLL output clock stable latency time
7	***[CGPLL0SEL]***<PLL0SEL> =1	PLL selection for fsys is carried out to PLL use (f_{PLL}).
8	***[CGPLL0SEL]***<PLL0ST> is read	It waits until the PLL selection status for fsys becomes PLL use (f_{PLL}) (=1).

Note1: 1 and 2 are executed when the ratio of the system clock should be changed.

Note2: 3 to 6 are unnecessary when the state before switching is ***[CGPLL0SEL]***<PLL0ON> = 1.
When changing from the state where the PLL output clock is stable, it can be changed to the PLL operation state by execution of only 7 and 8.

(2) fc setup (conduct PLL >>> PLL stop)

As an fc setup, the example of switching procedure from the PLL operation state to a PLL stop state is as follows.

<< The state before switching >>	
[CGPLL0SEL]<PLL0ON> =1	Sets the PLL for fsys to oscillate.
[CGPLL0SEL]<PLL0SEL> =1	Selects the PLL for fsys to "PLL is used (f_{PLL})".
[CGPLL0SEL]<PLL0ST> =1	Indicates the status of the PLL for fsys to "PLL is used (f_{PLL})".

<< The example of switching sequence >>		
1	***[CGPLL0SEL]***<PLL0SEL> =0	Selects the PLL for fsys to "PLL is unused (fosc)".
2	***[CGPLL0SEL]***<PLL0ST> is read	Waits until the status of the PLL for fsys becomes "PLL is unused (fosc) (=0)".
3	***[CGPLL0SEL]***<PLL0ON> =0	Sets the PLL operation for fsys to stop.

1.2.6. System clock

An internal high speed oscillation clock or external high speed oscillation clock (connected oscillator or clock input) can be used as a source of system clock.

The system clock consists of "High speed system clock (fsysh)(maximum 160MHz)" for high speed operation and "Middle speed system clock (fsysm)(maximum 80MHz)" which is generated by dividing High speed system clock. Middle speed system clock is used by peripheral function to save power dissipation without degrading CPU performance. The clock domains of the peripheral function can be checked in Table 1.4.

High speed system clock can be generated by dividing fc using ***[CGSYSCR]***<GEAR[2:0]> (Clock gear). And Middle speed system clock is generated by dividing the high speed system clock using ***[CGSYSCR]*** <MCKSEL[1:0]>. Although a setting can be changed during operation, after register writing before the clock actually changes, a time interval shown in Table 1.5 is required. The completion of the clock change should be checked by ***[CGSYSCR]***<GEARST[2:0]> <MCKSELGST[1:0]>.

Table 1.4 Clock domains of CPU and peripherals

Clock domain	Block
High speed system clock	CPU, Code Flash, Data Flash, Boot ROM, RAM0/1, CG, INTIF (IB, IMN), CRC, RAMP (ch0)
Middle speed system clock	DMAC, NBDIF, SIWDT, UART, TSPI, I2C, EI2C, T32A, ADC, OPAMP, PORT, A-PMD, A-ENC32, A-VE+, INTIF(IA), DNF, LVD, TRM, Flash (SFR), OFD, RAMP (ch1) , RLM, TRGSEL, RAM2

Table 1.5 Time interval for changing System clock

System clock	High speed (fsysh)	Middle speed (fsysm)
fsys	16 fc cycles at maximum	16 fc cycles at maximum
fsys/2	-	32 fc cycles at maximum
fsys/4	-	64 fc cycles at maximum

Note1: The clock gear and the system clock should not be changed while the peripheral function such as the timer/counter is operating.

Note2: An access between High speed system clock domain and Middle speed system clock domain cannot be done when the system clock is changing.

The table below shows the example of operating frequency by the clock gear ratio (1/1 to 1/16) to the frequency fc set up with oscillation frequency, a PLL multiplication value, etc.

Table 1.6 Example of operating frequency

External Oscillation (MHz)	External Clock input (MHz)	Built-in oscillation IHOSC1 (MHz)	PLL Multiplication value (after dividing)	Maximum Frequency (fc)(MHz)	Operating frequency (MHz) by the clock gear ratio PLL=ON					Operating frequency (MHz) by the clock gear ratio PLL=OFF				
					1/1	1/2	1/4	1/8	1/16	1/1	1/2	1/4	1/8	1/16
6	6	-	26.66	159.94	159.94	79.97	39.99	19.99	10.00	6	3	1.5	-	-
8	8	-	20	160	160	80	40	20	10	8	4	2	1	-
10	10	10	16	160	160	80	40	20	10	10	5	2.5	1.25	-
12	12	-	13	156	156	78	39	19.5	9.75	12	6	3	1.5	-

Table 1.7 Operating frequency examples of High speed and Middle speed system clocks

High speed system clock fsysh (MHz)	Middle speed system clock fsysm (MHz)		
	1/1	1/2	1/4
160	-	80	40
80	80	40	20

Note: The maximum frequency of Middle speed system clock is 80 MHz.

1.2.6.1. The setting method of a system clock

(1) fosc setup (Internal oscillation >>> External oscillation)

As a fosc setup, the example of switching procedure to the external high speed oscillator (EHOSC) from an internal high speed oscillator1 (IHOSC1) is shown below.

<< The state before switching >>	
[CGOSCCR]<IHOSC1EN> =1	An internal high speed oscillator1 oscillates.
[CGOSCCR]<OSCSEL> =0	The high speed oscillation selection for fosc is an internal high speed oscillator1 (IHOSC1).
[CGOSCCR]<OSCF> =0	The high speed oscillation selection status for fosc is an internal high speed oscillator1 (IHOSC1).
An oscillator is connected to X1 / X2 pin.	Do not connect any devices except a resonator.

<< The example of switching procedure >>		
1	***[PHPDN]***<bit[1:0]> =00 ***[PHIE]***<bit[1:0]> =00	Disable the pull-down resistors of X1 and X2 pins. Disable input control of X1 and X2 pins.
2	***[CGOSCCR]***<EOSCEN[1:0]> =01	It is an external high speed oscillator (EHOSC) about selection of an external oscillation of operation.
3	***[CGWUPHCR]***<WUCLK> =1 ***[CGWUPHCR]***<WUPT[15:4]> = arbitrary value	It is the external high speed oscillator (EHOSC) about high speed oscillation warming-up clock selection. A warming-up timer setting value is set to oscillator stable time.
4	***[CGWUPHCR]***<WUON> =1	High speed oscillation warming-up is started.
5	***[CGWUPHCR]***<WUEF> is read.	It waits until it becomes the termination of high speed oscillation warming-up (= 0).
6	***[CGOSCCR]***<OSCSEL> =1	It is high speed oscillation selection for fosc to the external high speed oscillator (EHOSC).
7	***[CGOSCCR]***<OSCF> is read	It waits until the high speed oscillation selection status for fosc becomes external high speed oscillator (=1).
8	***[CGOSCCR]***<IHOSC1EN> =0	An internal high speed oscillator1 is suspended.

(2) fosc setup (Internal oscillation >>> External clock input)

As a fosc setup, the example of switching procedure to the external clock input (EHCLKIN) from an internal oscillator1(IHOSC1) is shown below.

<< The state before switching >>	
[CGOSCCR]<IHOSC1EN> =1	An internal high speed oscillator1 oscillates.
[CGOSCCR]<OSCSEL> =0	The high speed oscillation selection for fosc is an internal high speed oscillator1 (IHOSC1).
[CGOSCCR]<OSCF> =0	The high speed oscillation selection status for fosc is an internal high speed oscillator1 (IHOSC1).
Clock into to EHCLKIN	Input in the proper voltage range.

<< The example of switching procedure >>		
1	***[PHPDN]***<bit[0]> =0 ***[PHIE]***<bit[0]> =1	Disable the pull-down resistor of X1/EHCLKIN pin. Enable the input control of X1/EHCLKIN pin.
2	***[CGOSCCR]***<EOSCEN[1:0]> =10	Selection of an external high speed oscillation of operation is carried out to an external clock input (EHCLKIN).
3	***[CGOSCCR]***<OSCSEL> =1	It is high speed oscillation selection for fosc to an external clock.
4	***[CGOSCCR]***<OSCF> is read	It waits until the high speed oscillation selection status for fosc becomes external high speed oscillator (=1).
5	***[CGOSCCR]***<IHOSC1EN> =0	An internal high speed oscillator1 is suspended.

(3) fosc setup (External oscillation/External clock input >>> Internal oscillation)

As a fosc setup, the example of switching procedure to the internal high speed oscillator1 (IHOSC1) from an external high speed oscillator (EHOSC) Operation State or an external clock input (EHCLKIN) Operation State is shown below.

<< The state before switching >>	
[CGOSCCR]<EOSCEN[1:0]> = 01 or 10	Selection of an external oscillator of operation is an external high speed oscillator (EHOSC) or external clock input.
[CGOSCCR]<OSCSEL> =1	The high speed oscillation selection for fosc is the external high speed oscillator (EHOSC).
[CGOSCCR]<OSCF> =1	The high speed oscillation selection status for fosc is the external high speed oscillator (EHOSC).

<< The example of switching procedure >>		
1	***[CGWUPHCR]***<WUCLK>=0	Set the warming-up clock selection to internal high speed oscillator1 (IHOSC1).
2	***[CGWUPHCR]***<WUPT[15:4]>=0x03C	Set the high speed oscillation warming-up timer setting value of 163.4 μs (=0x03C) or more.
3	***[CGOSCCR]***<IHOSC1EN> = 1	An internal high speed oscillator1 is oscillated.
4	***[CGWUPHCR]***<WUON> = 1	Start the high speed oscillation warming-up timer
5	***[CGWUPHCR]***<WUEF> is read	Wait until an warming-up timer status flag becomes ends(=1).
6	***[CGOSCCR]***<OSCSEL> = 0	Set the high speed oscillation selection for fosc to internal high speed oscillator1 (IHOSC1).
7	***[CGOSCCR]***<OSCF> is read	It waits until the high speed oscillation selection status for fosc becomes an internal high speed oscillator1 (=0).
8	***[CGOSCCR]***<EOSCEN[1:0]> = 00	Set the selection of an external high speed oscillator operation to unused.

1.2.7. Clock supply setting function

This MCU has the clock supply on/off function for the peripheral circuits. To reduce the power consumption, this MCU can stop supplying the clock to the peripheral functions that are not used.

Except some peripheral functions, clocks are not supplied after reset.

In order to supply the clock of the function to be used, set the bit of relevance of ***[CGFSYSENA]***, ***[CGFSYSMENA]***, ***[CGFSYSMENB]***, ***[CGFCEN]*** and ***[CGSPCLKEN]*** to "1".

For details, refer to "1.4 Explanation of Register".

1.2.8. Prescaler clock

Each peripheral function has a prescaler circuit to divide the ΦT0 clock. The ΦT0 clock which is input into the prescaler circuit can be divided by the ***[CGSYSCR]***<PRCK[3:0]> to generate High speed prescaler clock. And Middle speed prescaler clock is generated by dividing High speed prescaler clock using ***[CGSYSCR]*** <MCKSEL[1:0]>. For ΦT0 clock after reset, fc is chosen.

After register writing before a clock actually changes, a time interval shown in Table 1.8 is required.

To confirm the completion of the clock change, check the status of ***[CGSYSCR]***<PRCKST[3:0]> <MCKSELPST[1:0]>.

Table 1.8 Time interval for changing prescaler clocks

Prescaler clock	High speed (ΦT0h)	Middle speed (ΦT0m)
ΦT0	512 fc cycles at maximum	512 fc cycles at maximum
ΦT0/2	-	1024 fc cycles at maximum
ΦT0/4	-	2048 fc cycles at maximum

Note1: Do not change a prescaler clock during operation of peripheral functions, such as a timer counter.

Note2: An access between High speed system clock domain and Middle speed system clock domain cannot be done when the prescaler clock is changing.

1.3. Operation mode

There are NORMAL mode and a Low Power consumption mode (IDLE, STOP1) in this product as an Operation mode, and it can reduce power consumption by performing mode changes according to directions for use.

1.3.1. Details of an Operation mode

1.3.1.1. The feature in each mode

The feature in NORMAL, Low power consumption modes is as follows.

- NORMAL mode

  CPU core and peripheral circuits operate with the high speed oscillation clock. After reset release, the system operates in NORMAL mode.

- Low power consumption mode

  The feature in Low power consumption modes is as follows.

  – IDLE mode

    It is the mode which CPU stops.

    The peripheral function should perform operation/stop by the register of each peripheral function, a clock supply setting function, etc.

    Note: Note that the CPU cannot clear the watchdog timer in IDLE mode.

  – STOP1 mode

    In this mode, all the internal circuits including the internal oscillator stop.

    If STOP1 mode is canceled, the internal high speed oscillator1 (IHOSC1) will start oscillation, and the system will return to NORMAL mode.

    Please disable interrupt which is not used for STOP1 release before shifting to the STOP1 mode.

1.3.1.2. Transition to and Return from Low Power Consumption mode

In order to shift to each Low Power Consumption mode, the IDLE/STOP1 mode is chosen by standby control register ***[CGSTBYCR]***<STBY[1:0]>, and a WFI (Wait For Interrupt) command is executed. When the transition to the low power consumption mode has been done by WFI instruction, the return from the mode can be done by the reset or an interrupt generation. To return by interrupt, it is necessary to set up. Please refer to "Interrupts" chapter of the reference manual "Exception" for details.

Note1: This product does not support a return by events; therefore, do not make a transition to low-power consumption mode triggered by WFE (Wait For Event).

Note2: This product does not support low power consumption mode by SLEEPDEEP of the Cortex-M4 processor with FPU core. Do not use the <SLEEPDEEP> bit of the system control register.

1.3.1.3. Selection of a Low Power Consumption mode

Low Power Consumption mode selection is chosen by setup of ***[CGSTBYCR]***<STBY[1:0]>.
Following table shows the mode chosen from a setup of <STBY[1:0]>.

Table 1.9 Low Power Consumption mode selection

Mode	***[CGSTBYCR]*<STBY[1:0]>**
IDLE	00
STOP1	01

Note: Do not use the settings other than the above.

1.3.1.4. The peripheral function state in a Low Power Consumption mode

The following Table 1.10 shows the Operation State of the peripheral function (block) in each mode.
In addition, after reset release, it will be in the state where a clock is not supplied except for some blocks.
If needed, set up ***[CGFSYSENA]***, ***[CGFSYSMENA]***, ***[CGFSYSMENB]***, ***[CGFCEN]***, ***[CGSPCLKEN]*** and enable clock supply.

Table 1.10 Block operation status in each Low Power Consumption mode

Block		NORMAL	IDLE	STOP1
Processor core (Including Debug)		✓	-	-
DMAC		✓	✓	-
I/O port	Pin status	✓	✓	✓
	Register	✓	✓	-
ADC (with OPAMP)		✓	✓	-
UART		✓	✓	-
I2C		✓	✓	-
EI2C		✓	✓	-
TSPI		✓	✓	-
A-PMD		✓	✓	-
A-ENC32		✓	✓	-
A-VE+		✓	✓	-
T32A		✓	✓	-
TRGSEL		✓	✓	-
CRC		✓	✓	-
SIWDT		✓	✓ (Note1)	-
LVD		✓	✓	✓
OFD		✓	✓	-
TRM		✓	Unavailable	-
CG		✓	✓	✓
PLL		✓	✓	-
RAMP		✓	✓	-
External High speed oscillator (EHOSC)		✓	✓	-
Internal High speed oscillator1 (IHOSC1)		✓	✓	-
Internal High speed oscillator2 (IHOSC2)		✓	✓	-
Code Flash		Access Possible	Access Possible (Note2)	Data hold
Data Flash				
RAM				

✓: Operation is possible.
-: If it shifts to the object mode, the clock to peripheral circuits stop automatically.

Note1: Protect A mode only. In other cases, stop SIWDT before transiting to IDLE mode.
Note2: It becomes a data hold when peripheral functions (DMA etc.) except CPU which carry out data access (R/W) are not connected on the bus matrix.

1.3.2. Mode State Transition

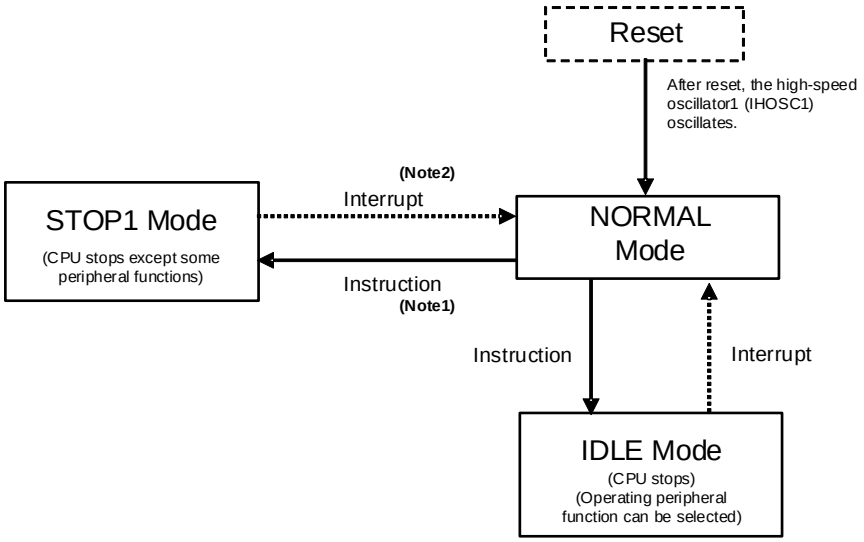

Figure 1.2 Mode State Transition

Note1: Warming-up is required at returning. A warming-up time must be set in the previous mode (NORMAL mode) before entering to STOP1 mode.

Note2: When the MCU returns from STOP1 mode, the MCU branches to the interrupt service routine triggered by interrupt events.

1.3.2.1. IDLE mode transition flow

Set up the following procedure at switching to IDLE mode.

Because IDLE mode is released by an interrupt, set the interrupt before switching to IDLE mode. For the interrupts that can be used to release the IDLE mode, refer to "1.3.3.1. The release source of a Low Power Consumption mode". Disable interrupts not used for release and interrupts that cannot be used.

Transition flow (from Normal mode)		
1	***[SIWDxEN]***<WDTE>=0	Disable SIWDT.
2	***[SIWDxCR]***<WDCR[7:0]>=0xB1	Disable SIWDT.
3	***[FCSR0]***<RDYBSY> is read.	It waits until Flash will be in a Ready state (= 1).
4	***[CGSTBYCR]***<STBY[1:0]>=00	Low Power Consumption mode selection is set to IDLE.
5	***[CGSTBYCR]***<STBY[1:0]> is read.	Check the 4th line register writing (= 00).
6	WFI command execution	Switch to IDLE.

Note: When using the protected A mode of SIWDT, 1 and 2 step are not required.

1.3.2.2. STOP1 mode transition flow

Set up the following procedure at switching to STOP1.

Because STOP1 mode is released by an interrupt, set the interrupt before switching to STOP1 mode. For the interrupts that can be used to release the STOP1 mode, refer to "1.3.3.1. The release source of a Low Power Consumption mode". Disable interrupts not used for release and interrupts that cannot be used.

Transition flow (from Normal mode)		
1	***[SIWDxEN]***<WDTE>=0	Disable SIWDT.
2	***[SIWDxCR]***<WDCR[7:0]>=0xB1	Disable SIWDT.
3	***[FCSR0]***<RDYBSY> is read.	Wait until Flash becomes the Ready state (=1).
4	***[CGWUPHCR]***<WUEF> is read.	Wait until the high speed oscillation warming-up ends (=0).
5	***[CGWUPHCR]***<WUCLK>=0	Set the warming-up clock selection to internal high speed oscillator1 (IHOSC1).
	[CGWUPHCR]<WUPT[15:4]>= 0x03C	Set the high speed oscillation warming-up timer setting value to 163.4 μs(=0x03C) or more.
6	***[CGSTBYCR]***<STBY[1:0]>=01	Low Power Consumption mode selection is set to STOP1.
7	***[CGPLL0SEL]***<PLL0SEL>=0	Set PLL of fsys to fosc (= PLL no USE)
8	***[CGPLL0SEL]***<PLL0ST> is read.	Wait until PLL status of fsys becomes off state (= 0).
9	***[CGPLL0SEL]***<PLL0ON>=0	Stop PLL for fsys
10	***[CGOSCCR]***<IHOSC1EN>=1	Enable the internal high speed oscillator1.
11	***[CGWUPHCR]***<WUON> = 1	Start the high speed oscillation warming-up timer
12	***[CGWUPHCR]***<WUEF> is read	Wait until an warming-up timer status flag becomes ends(=1).
13	***[CGOSCCR]***<OSCSEL>=0	Set the high speed oscillation selection for fosc to internal high speed oscillator1 (IHOSC1).
14	***[CGOSCCR]***<OSCF> is read.	Wait until the high speed oscillation selection status for fosc becomes internal high speed oscillator1 (IHOSC1) (=0).
15	***[CGOSCCR]***<EOSCEN[1:0]>=00	Selection of an external oscillator1 is set to "Unused".
16	***[CGOSCCR]***<IHOSC2EN> =0	The internal high speed oscillator2 (IHOSC2) is stopped.
17	***[CGOSCCR]***<EOSCEN[1:0]> is read.	The register writing of above 15th is checked (=00).
18	***[CGOSCCR]***<IHOSC2F> is read.	Wait until the status of IHOSC2 becomes "0".
19	WFI command execution	Switch to STOP1.

1.3.3. Return from a Low Power Consumption mode

1.3.3.1. The release source of a Low Power Consumption mode

Interrupt, Non-Maskable Interrupt, and reset can perform return from a Low Power Consumption mode. The standby release source which can be used is decided by a Low Power Consumption mode.

It shows the following table about details.

Table 1.11 Release source list

Low Power Consumption mode			IDLE	STOP1
Release Source	Interrupt	INT00 to INT18, INT21 (Note)	✓	✓
		INTVCN0, INTVCT0	✓	-
		INTEMGx, INTOVVx, INTPWMx	✓	-
		INTENCx0, INTENCx1	✓	-
		INTADxPDA, INTADxPDB, INTADxCP0, INTADxCP1, INTADxTRG, INTADxSGL, INTADxCNT	✓	-
		INTSCxRX, INTSCxTX, INTSCxERR	✓	-
		INTI2CxNST, INTI2CxATX, INTI2CxBRX, INTI2CxNA	✓	-
		INTT32AxAC, INTT32AxACCAP0, INTT32AxACCAP1, INTT32AxB, INTT32AxBCAP0, INTT32AxBCAP1	✓	-
		INTPARIx	✓	-
		INTDMAATC,INTDMAAERR	✓	-
		INTFLCRDY	✓	-
		INTFLDRDY	✓	-
	SysTick interrupt		✓	-
	Non-Maskable Interrupt (INTWDT0)		✓	-
	Non-Maskable Interrupt (INTLVD)		✓	✓
	Reset (SIWDT)		✓	-
	Reset (LVD)		✓	✓
	Reset (OFD)		✓	-
	Reset (RESET_N pin)		✓	✓

✓: After release, the interrupt procedure will start.

-: It cannot be used for release.

Note: INT00 to INT18, INT21 (External Interrupt 00 to 18, 21) can select one of falling edge, rising edge and level. For details, please refer to the reference manual "Exception".

- Released by an interrupt request

  When interrupt cancels a Low Power Consumption mode, it is necessary to prepare so that interrupt may be detected by CPU. The interrupt used for release in STOP1 mode needs to set up CPU, and needs to set up detection by INTIF.

- Released by Non-Maskable Interrupt (NMI)

  The WDT interrupt (INTWDT0, Protect A mode only.) or the LVD interrupt (INTLVD) can perform release from the Low Power Consumption modes.

- Released by reset

  The reset can perform release from all the Low Power Consumption modes.

  When released by reset, the registers will be initialized in NORMAL mode after release. For details, refer to "3.2.6.1. The reset factor and the reset range".

- Released by SysTick interrupt

  SysTick interrupt is available only in IDLE mode.

Refer to "Interrupt" chapter of the reference manual "Exception" for details of interrupt.

1.3.3.2. Warming-up at the release of Low Power Consumption mode

Warming-up may be required because of stability of an internal oscillator at the time of mode transition.

When the transition from STOP1 mode to NORMAL mode is done, the internal oscillation is selected automatically and the warming-up timer starts up. The Output of a system clock is started after warming-up time progress.

For this reason, before executing the command which move to the STOP1 mode, set up warming-up time by ***[CGWUPHCR]***<WUPT[15:4]>. For the setting method, refer to "1.2.4.1. The warming-up timer for a high speed oscillation".

The following table shows the necessity of a warming-up setup at the time of each Operation mode transition.

Table 1.12 Warming-up

Operation mode transition	Warming-up setup
NORMAL >>> IDLE	Not required.
NORMAL >>> STOP1	Not required.
IDLE >>> NORMAL	Not required.
STOP1 >>> NORMAL	Required.

1.3.4. Clock operation by mode transition

The clock operation in case of mode transition is shown below.

1.3.4.1. NORMAL >>> IDLE >>> NORMAL Operation mode transition

CPU stops at IDLE mode. The clock supply to a peripheral function holds a setting state. Please perform operation/stop by the register of each peripheral function, a clock supply setting function, etc. if needed. Execution of warming-up operation is not performed at the time of the restart operation in NORMAL mode from IDLE state.

After the command (WFI) execution which switches to IDLE mode, a program counter will show the next point and will be in a CPU idle state. With a release source, it becomes a CPU reboot and, in the case of an enable interrupt state, the shift to next point of the transition command (WFI) will be done, after the interrupt processing by release source.

1.3.4.2. NORMAL >>> STOP1 >>> NORMAL Operation mode transition

When returning to NORMAL mode from the STOP1 mode, warming-up is started automatically.

Please set ***[CGWUPHCR]***<WUPT[15:4]> to warming-up time (163.4 µs or more) before moving to the STOP1 mode.

Note: When the RESET_N pin and LVD reset are the release factors, warming-up time is the same as the operation at the time of warm-reset, and is replaced by "internal processing time" and "CPU operation wait time". For details, refer to "3.2.2.1. Warm reset by RESET_N pin" and "3.2.2.2. Warm reset by LVD".

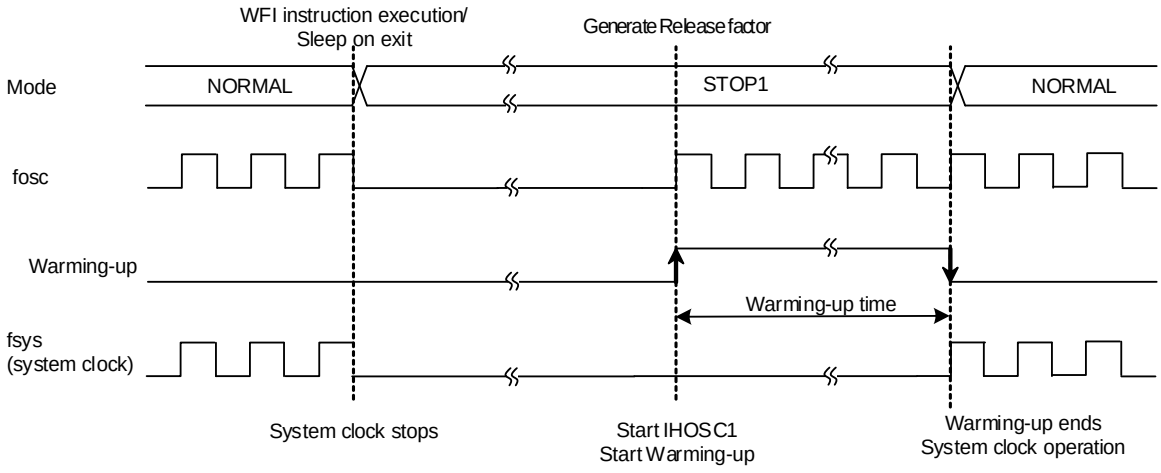

Figure 1.3 NORMAL >>> STOP1 >>> NORMAL Operation mode transition

1.4. Explanation of Register

1.4.1. Register list

The register related to CG and its address information are shown below.

Peripheral function		Channel/Unit	Base address
Clock Control and Operation Mode	CG	-	0x40083000

Register name		Address (Base+)
CG write protection register	***[CGPROTECT]***	0x0000
Oscillation control register	***[CGOSCCR]***	0x0004
System clock control register	***[CGSYSCR]***	0x0008
Standby control register	***[CGSTBYCR]***	0x000C
PLL selection register for fsys	***[CGPLL0SEL]***	0x0020
High speed oscillation warming-up register	***[CGWUPHCR]***	0x0030
Supply and stop register A for fsysm	***[CGFSYSMENA]***	0x0048
Supply and stop register B for fsysm	***[CGFSYSMENB]***	0x004C
Supply and stop register A for fsysh	***[CGFSYSENA]***	0x0050
Clock supply and stop register for fc	***[CGFCEN]***	0x0058
Clock supply and stop register for ADC and Debug circuit	***[CGSPCLKEN]***	0x005C

1.4.2. Detail of Register

1.4.2.1. *[CGPROTECT]* (CG write protection register)

Bit	Bit Symbol	After reset	Type	Function
31:8	-	0	R	Read as "0"
7:0	PROTECT[7:0]	0xC1	R/W	Control write-protection for the CG register (all registers included except this register) 0xC1: CG Registers are write-enabled. Other than 0xC1: Sets write protection (Protect enable)

1.4.2.2. *[CGOSCCR]* (Oscillation control register)

Bit	Bit Symbol	After reset	Type	Function
31:20	-	0	R	Read as "0"
19	IHOSC2F	0	R	Indicates the stability flag of internal oscillation for IHOSC2 0: Stopping or being in warming-up 1: Stable oscillation
18:17	-	0	R	Read as "0"
16	IHOSC1F	1	R	Indicates the stability flag of internal oscillation for IHOSC1 (Note4) 0: Stopping or being in warming-up 1: Stable oscillation
15:13	-	0	R	Read as "0"
12	-	0	R/W	Write as "0"
11:10	-	0	R	Read as "0"
9	OSCF	0	R	Indicates high speed oscillator for fosc selection status. 0: Internal high speed oscillator1 (IHOSC1) 1: External high speed oscillator (EHOSC)
8	OSCSEL	0	R/W	Selects a high speed oscillation for fosc. (Note1) 0: Internal high speed oscillator1 (IHOSC1) 1: External high speed oscillator (EHOSC)
7:4	-	0	R	Read as "0"
3	IHOSC2EN	0	R/W	Enables the internal high speed oscillator2 (IHOSC2) (Note 2) 0: Stop 1: Oscillation
2:1	EOSCEN[1:0]	00	R/W	Selects the operation of the external high speed oscillator. (EHOSC) (Note3) 00: External high speed oscillator is not used 01: Uses the external high speed oscillator (EHOSC) 10: Uses the external clock (EHCLKIN) 11: Reserved
0	IHOSC1EN	1	R/W	Internal high speed oscillator1 (IHOSC1) 0: Stop 1: Oscillation

Note1: When the setting is modified, confirm whether the written value has been reflected to the ***[CGOSCCR]*** <OSCF> bit before executing the next operation.

Note2: Setting cannot be changed, when it is ***[SIWDxOSCCR]***<OSCPRO> =1 (Write protection of SIWDT is effective)

Note3: When using the oscillator connection, set this bit to "01" (external high speed oscillator).

Note4: To wait stabilizing oscillation of an internal high speed oscillator1 (IHOSC1), use a warming-up timer and confirm ***[CGWUPHCR]***<WUEF> instead of <IHOSC1F>.

1.4.2.3. *[CGSYSCR]* (System clock control register)

Bit	Bit Symbol	After reset	Type	Function
31:30	MCKSELPST[1:0]	00	R	Middle speed prescaler clock (ΦT0m) selection status 00: <PRCK[3:0]> setting value (no division) 01: <PRCK[3:0]> setting value is divided by 2 10,11: <PRCK[3:0]> setting value is divided by 4
29:28	-	0	R	Read as "0"
27:24	PRCKST[3:0]	0000	R	High speed prescaler clock (ΦT0h) selection status 0000: fc 0100: fc/16 1000: fc/256 0001: fc/2 0101: fc/32 1001: fc/512 0010: fc/4 0110: fc/64 1010 to 1111: Reserved 0011: fc/8 0111: fc/128
23:22	MCKSELGST[1:0]	00	R	Middle speed system clock (fsysm) selection status 00: <GEAR[2:0]> setting value (no division) 01: <GEAR[2:0]> setting value is divided by 2 10,11: <GEAR[2:0]> setting value is divided by 4
21:19	-	0	R	Read as "0"
18:16	GEARST[2:0]	000	R	High speed system clock (fsysh) gear selection status 000: fc 100: fc/16 001: fc/2 101 to 111: Reserved 010: fc/4 011: fc/8
15:12	-	0	R	Read as "0"
11:8	PRCK[3:0]	0000	R/W	High speed prescaler clock (ΦT0h) selection 0000: fc 0100: fc/16 1000: fc/256 0001: fc/2 0101: fc/32 1001: fc/512 0010: fc/4 0110: fc/64 1010 to 1111: Reserved 0011: fc/8 0111: fc/128 Selects a prescaler clock for the peripheral functions.
7:6	MCKSEL[1:0]	00	R/W	Middle speed system clock (fsysm) and Middle speed prescaler clock (ΦT0m) selection 00: <GEAR[2:0]>, <PRCK[3:0]> setting values (no division) 01: <GEAR[2:0]>, <PRCK[3:0]> setting values are divided by 2. 10,11: <GEAR[2:0]>,<PRCK[3:0]> setting values are divided by 4. Maximum operating frequency of middle speed system clock is 80MHz.
5:3	-	0	R	Read as "0"
2:0	GEAR[2:0]	000	R/W	High speed system clock (fsysh) gear selection 000: fc 100: fc/16 001: fc/2 101 to 111: Reserved 010: fc/4 011: fc/8

1.4.2.4. *[CGSTBYCR]* (Standby control register)

Bit	Bit Symbol	After reset	Type	Function
31:2	-	0	R	Read as "0"
1:0	STBY[1:0]	00	R/W	Selects a low power consumption mode. 00: IDLE 01: STOP1 10: Reserved 11: Reserved

1.4.2.5. *[CGPLL0SEL]* (PLL selection register for fsys)

Bit	Bit Symbol	After reset	Type	Function
31:8	PLL0SET[23:0]	0x000000	R/W	PLL0 multiplication setup About a multiplication setup, refer to "1.2.5.2. The formula and the example of a setting of a PLL multiplication value".
7:3	-	0	R	Read as "0"
2	PLL0ST	0	R	Indicates PLL for fsys selection status. 0: fosc 1: f_{PLL}
1	PLL0SEL	0	R/W	Selects Clock selection for fsys 0: fosc 1: f_{PLL}
0	PLL0ON	0	R/W	Selects PLL operation for fsys 0: Stop 1: Oscillation

1.4.2.6. *[CGWUPHCR]* (High speed oscillation warming-up register)

Bit	Bit Symbol	After reset	Type	Function
31:20	WUPT[15:4]	0x800	R/W	Sets the upper 12 bits of the 16 bits of calculation values of the warming-up timer. About a setup of a warming-up timer, refer to "1.2.4.1. The warming-up timer for a high speed oscillation".
19:16	WUPT[3:0]	0000	R	Sets the lower 4 bits of the 16 bits of calculation values of the warming-up timer. It is fixed to "0000".
15:9	-	0	R	Read as "0"
8	WUCLK	0	R/W	Warming-up clock selection (Note1) 0: Internal high speed oscillator1 (IHOSC1) 1: External high speed oscillator (EHOSC)
7:2	-	0	R	Read as "0"
1	WUEF	0	R	Indicates status of the warming-up timer. (Note2) 0: The end of warming-up 1: In warming-up operation
0	WUON	0	W	Control the warming-up timer. 0: Don't care 1: Warming-up operation start.

Note1: Use the internal oscillator for warming-up when the MCU returns from STOP1 mode. Do not use an external oscillator when the MCU returns from STOP1 mode.

Note2: Do not modify the registers during the warming-up (<WUEF>=1). Set the registers when <WUEF>=0.

1.4.2.7. *[CGFSYSMENA]* (Supply and stop register A for fsysm)

Bit	Bit Symbol	After reset	Type	Function
31	IPMENA31	0	R/W	Clock enable of T32A ch03 (TSEL34,35,36) 0: Clock stop 1: Clock supply
30	IPMENA30	0	R/W	Clock enable of T32A ch02 (TSEL31,32,33) 0: Clock stop 1: Clock supply
29	IPMENA29	0	R/W	Clock enable of T32A ch01 (TSEL28,29,30) 0: Clock stop 1: Clock supply
28	IPMENA28	1	R/W	Clock enable of T32A ch00 (TSEL25,26,27) 0: Clock stop 1: Clock supply
27	IPMENA27	0	R/W	Write as "0"
26	IPMENA26	0	R/W	Clock enable of I2C ch1 0: Clock stop 1: Clock supply
25	IPMENA25	0	R/W	Clock enable of I2C ch0 0: Clock stop 1: Clock supply

Bit	Bit Symbol	After reset	Type	Function
24	IPMENA24	0	R/W	Clock enable of UART ch3 (TSEL24) 0: Clock stop 1: Clock supply
23	IPMENA23	0	R/W	Clock enable of UART ch2 (TSEL23) 0: Clock stop 1: Clock supply
22	IPMENA22	0	R/W	Clock enable of UART ch1 (TSEL22) 0: Clock stop 1: Clock supply
21	IPMENA21	1	R/W	Clock enable of UART ch0 (TSEL21) 0: Clock stop 1: Clock supply
20	IPMENA20	0	R/W	Clock enable of TSPI ch1 (TSEL20) 0: Clock stop 1: Clock supply
19	IPMENA19	0	R/W	Clock enable of TSPI ch0 (TSEL19) 0: Clock stop 1: Clock supply
18	-	0	R	Read as "0"
17	IPMENA17	0	R/W	Clock enable of PORT V 0: Clock stop 1: Clock supply
16	IPMENA16	0	R/W	Clock enable of PORT U 0: Clock stop 1: Clock supply
15	-	0	R	Read as "0"
14	-	0	R	Read as "0"
13	-	0	R	Read as "0"
12	IPMENA12	0	R/W	Clock enable of PORT N 0: Clock stop 1: Clock supply
11	IPMENA11	0	R/W	Clock enable of PORT M 0: Clock stop 1: Clock supply
10	IPMENA10	0	R/W	Clock enable of PORT L 0: Clock stop 1: Clock supply
9	IPMENA09	0	R/W	Clock enable of PORT K 0: Clock stop 1: Clock supply
8	IPMENA08	0	R/W	Clock enable of PORT J 0: Clock stop 1: Clock supply
7	IPMENA07	0	R/W	Clock enable of PORT H 0: Clock stop 1: Clock supply
6	IPMENA06	0	R/W	Clock enable of PORT G 0: Clock stop 1: Clock supply

Bit	Bit Symbol	After reset	Type	Function
5	IPMENA05	0	R/W	Clock enable of PORT F 0: Clock stop 1: Clock supply
4	IPMENA04	0	R/W	Clock enable of PORT E 0: Clock stop 1: Clock supply
3	IPMENA03	0	R/W	Clock enable of PORT D 0: Clock stop 1: Clock supply
2	IPMENA02	1	R/W	Clock enable of PORT C 0: Clock stop 1: Clock supply
1	IPMENA01	0	R/W	Clock enable of PORT B 0: Clock stop 1: Clock supply
0	IPMENA00	0	R/W	Clock enable of PORT A 0: Clock stop 1: Clock supply

Note1: Even if the initial value of the register is set to stop of the clock, the clock is supplied during the reset.

Note2: Write "0" for bit of function that does not exist in TMPM4KM and TMPM4KL. For details, refer to "1.5. Information according to product".

1.4.2.8. *[CGFSYSMENB]* (Supply and stop register B for fsysm)

Bit	Bit Symbol	After reset	Type	Function
31	IPMENB31	1	R/W	Clock enable of SIWDT ch0 0: Clock stop 1: Clock supply
30	IPMENB30	1	R/W	Clock enable of NBDIF 0: Clock stop 1: Clock supply
29	IPMENB29	1	R/W	Write as "1"
28:27	-	0	R	Read as "0"
26	IPMENB26	0	R/W	Clock enable of EI2C ch1 0: Clock stop 1: Clock supply
25	IPMENB25	0	R/W	Clock enable of EI2C ch0 0: Clock stop 1: Clock supply
24:18	-	0	R	Read as "0"
17	IPMENB17	0	R/W	Clock enable of DMAC Unit A (TSEL00 to 15) 0: Clock stop 1: Clock supply
16	IPMENB16	0	R/W	Clock enable of TRGSEL 0: Clock stop 1: Clock supply
15	IPMENB15	0	R/W	Clock enable of TRM 0: Clock stop 1: Clock supply
14	IPMENB14	0	R/W	Clock enable of OFD 0: Clock stop 1: Clock supply
13	IPMENB13	0	R/W	Clock enable of RAMP ch1 0: Clock stop 1: Clock supply
12	IPMENB12	0	R/W	Clock enable of A-VE+ ch0 0: Clock stop 1: Clock supply
11	IPMENB11	0	R/W	Clock enable of A-PMD ch2 0: Clock stop 1: Clock supply
10	IPMENB10	0	R/W	Clock enable of A-PMD ch1 0: Clock stop 1: Clock supply
9	IPMENB09	0	R/W	Clock enable of A-PMD ch0 0: Clock stop 1: Clock supply
8	IPMENB08	0	R/W	Clock enable of A-ENC32 ch2 0: Clock stop 1: Clock supply

Bit	Bit Symbol	After reset	Type	Function
7	IPMENB07	0	R/W	Clock enable of A-ENC32 ch1 0: Clock stop 1: Clock supply
6	IPMENB06	0	R/W	Clock enable of A-ENC32 ch0 0: Clock stop 1: Clock supply
5	IPMENB05	0	R/W	Clock enable of OPAMP Unit A/B/C 0: Clock stop 1: Clock supply
4	IPMENB04	0	R/W	Clock enable of ADC Unit C (TSEL18) 0: Clock stop 1: Clock supply
3	IPMENB03	0	R/W	Clock enable of ADC Unit B (TSEL17) 0: Clock stop 1: Clock supply
2	IPMENB02	0	R/W	Clock enable of ADC Unit A (TSEL16) 0: Clock stop 1: Clock supply
1	IPMENB01	0	R/W	Clock enable of T32A ch05 (TSEL40,41,42) 0: Clock stop 1: Clock supply
0	IPMENB00	0	R/W	Clock enable of T32A ch04 (TSEL37,38,39) 0: Clock stop 1: Clock supply

Note1: Even if the initial value of the register is set to stop of the clock, the clock is supplied during the reset.

Note2: Write "0" for bit of function that does not exist in TMPM4KM and TMPM4KL. For details, refer to "1.5. Information according to product".

1.4.2.9. *[CGFSYSENA]* (Supply and stop register A for fsysh)

Bit	Bit Symbol	After reset	Type	Function
31:2	-	0	R	Read as "0"
1	IPENA01	0	R/W	Clock enable of RAMP ch0 0: Clock stop 1: Clock supply
0	IPENA00	0	R/W	Clock enable of CRC 0: Clock stop 1: Clock supply

Note: Even if the initial value of the register is set to stop of the clock, the clock is supplied during the reset.

1.4.2.10. *[CGFCEN]* (Clock supply and stop register for fc)

Bit	Bit Symbol	After reset	Type	Function
31:29	-	0	R	Read as "0"
28	FCIPEN28	0	R/W	Clock enable of DNF Unit C (INT21) 0: Clock stop 1: Clock supply
27	FCIPEN27	0	R/W	Clock enable of DNF Unit B (INT08b to 18) 0: Clock stop 1: Clock supply
26	FCIPEN26	0	R/W	Clock enable of DNF Unit A (INT00 to 08a,11b) 0: Clock stop 1: Clock supply
25:24	-	0	R	Read as "0"
23	FCIPEN23	0	R/W	Clock enable of OFD detection target clock 1 (fc) 0: Clock stop 1: Clock supply
22:0	-	0	R	Read as "0"

Note1: Even if the initial value of the register is set to stop of the clock, the clock is supplied during the reset.

Note2: Write "0" for bit of function that does not exist in TMPM4KM and TMPM4KL. For details, refer to "1.5. Information according to product".

1.4.2.11. *[CGSPCLKEN]* (Clock supply and stop register for ADC and Debug circuit)

Bit	Bit Symbol	After reset	Type	Function
31:20	-	0	R	Read as "0"
19	-	0	R/W	Write as "0"
18	ADCKEN2	0	R/W	Enable the clock for ADC Unit C (Note2) 0: Clock stop 1: Clock supply
17	ADCKEN1	0	R/W	Enable the clock for ADC Unit B (Note2) 0: Clock stop 1: Clock supply
16	ADCKEN0	0	R/W	Enable the clock for ADC Unit A (Note2) 0: Clock stop 1: Clock supply
15:1	-	0	R	Read as "0"
0	TRCKEN	0	R/W	Enable the Clock for the Trace function of Debug circuit (Trace or SWV). 0: Clock stop 1: Clock supply

Note1: Even if the initial value of the register is set to stop of the clock, the clock is supplied during the reset.

Note2: When setting this bit to "0" (clock stop), please make sure that AD conversion is stopped.

1.5. Information according to product

The information about ***[CGFSYSMENA]***, ***[CGFSYSMENB]***, ***[CGFSYSENA]*** and ***[CGFCEN]*** which are different according to each product is shown below.

1.5.1. *[CGFSYSMENA]*

Table 1.13 *[CGFSYSMENA]* register corresponding to each product

Bit	Bit Symbol	Internal connection peripheral circuit	Channel No./ Unit name / Port name	M4KN	M4KM	M4KL
31	IPMENA31	T32A	3	✓	✓	✓
30	IPMENA30		2	✓	✓	✓
29	IPMENA29		1	✓	✓	✓
28	IPMENA28		0	✓	✓	✓
26	IPMENA26	I2C	1	✓	✓	✓
25	IPMENA25		0	✓	✓	✓
24	IPMENA24	UART	3	✓	✓	-
23	IPMENA23		2	✓	✓	✓
22	IPMENA22		1	✓	✓	✓
21	IPMENA21		0	✓	✓	✓
20	IPMENA20	TSPI	1	✓	✓	✓
19	IPMENA19		0	✓	✓	✓
17	IPMENA17	PORT	V	✓	-	-
16	IPMENA16		U	✓	✓	✓
12	IPMENA12		N	✓	✓	-
11	IPMENA11		M	✓	-	-
10	IPMENA10		L	✓	✓	✓
9	IPMENA09		K	✓	✓	✓
8	IPMENA08		J	✓	✓	✓
7	IPMENA07		H	✓	✓	✓
6	IPMENA06		G	✓	✓	✓
5	IPMENA05		F	✓	✓	✓
4	IPMENA04		E	✓	✓	✓
3	IPMENA03		D	✓	-	-
2	IPMENA02		C	✓	✓	✓
1	IPMENA01		B	✓	✓	✓
0	IPMENA00		A	✓	✓	✓

Note: ✓: Available, -: N/A

1.5.2. *[CGFSYSMENB]*

Table 1.14 *[CGFSYSMENB]* register corresponding to each product

Bit	Bit Symbol	Internal connection peripheral circuit	Channel No./ Unit name / Port name	M4KN	M4KM	M4KL
31	IPMENB31	SIWDT	0	✓	✓	✓
30	IPMENB30	NBDIF	-	✓	-	-
26	IPMENA26	EI2C	1	✓	✓	✓
25	IPMENA25		0	✓	✓	✓
17	IPMENB17	DMAC	A	✓	✓	✓
16	IPMENB16	TRGSEL	-	✓	✓	✓
15	IPMENB15	TRM	-	✓	✓	✓
14	IPMENB14	OFD	-	✓	✓	✓
13	IPMENB13	RAMP	1	✓	✓	✓
12	IPMENB12	A-VE+	0	✓	✓	✓
11	IPMENB11	A-PMD	2	✓	✓	✓
10	IPMENB10		1	✓	✓	✓
9	IPMENB09		0	✓	✓	✓
8	IPMENB08	A-ENC32	2	✓	✓	✓
7	IPMENB07		1	✓	✓ (Note2)	-
6	IPMENB06		0	✓	✓	-
5	IPMENB05	OPAMP	A,B,C	✓	✓	✓
4	IPMENB04	ADC	C	✓	✓	✓
3	IPMENB03		B	✓	✓	✓
2	IPMENB02		A	✓	✓	✓
1	IPMENB01	T32A	5	✓	✓	✓
0	IPMENB00		4	✓	✓	✓

Note1: ✓: Available, -: N/A

Note2: There is no ENCxZ pin in M4KM.

1.5.3. *[CGFSYSENA]*

Table 1.15 *[CGFSYSENA]* register corresponding to each product

Bit	Bit Symbol	Internal connection peripheral circuit	Channel No./ Unit name / Port name	M4KN	M4KM	M4KL
1	IPENA01	RAMP	0	✓	✓	✓
0	IPENA00	CRC	-	✓	✓	✓

Note: ✓: Available, -: N/A

1.5.4. *[CGFCEN]*

Table 1.16 *[CGFCEN]* register corresponding to each product

Bit	Bit Symbol	Internal connection peripheral circuit	Channel No./ Unit name / Port name	M4KN	M4KM	M4KL
28	FCIPEN28	DNF	C	✓	✓	✓
27	FCIPEN27		B	✓	✓	✓
26	FCIPEN26		A	✓	✓	✓
23	FCIPEN23	OFD	-	✓	✓	✓

Note: ✓: Available, -: N/A

2. Memory map

2.1. Outlines

The memory maps for TMPM4K Group(2) are based on the Arm Cortex-M4(with FPU) processor core memory map.

The internal ROM, internal RAM and special function registers (SFR) of TMPM4K Group(2) are mapped to the Code, SRAM and peripheral regions of the Cortex-M4(with FPU) respectively. The special function register (SFR) means the control registers of all input/output ports and peripheral functions.

The CPU register region is the processor core's internal register region.

For more information on each region, see the "Arm documentation set for the Arm Cortex-M4".

Note that access to regions indicated as "Fault" causes a bus fault if bus faults are enabled, or causes a hard fault if bus faults are disabled. Also, do not access the vendor-specific region.

2.1.1. TMPM4KxF10A

- Code Flash : 1MB
- RAM : 64KB
- Data Flash : 32KB
- Products : TMPM4KNF10ADFG, TMPM4KNF10AFG, TMPM4KLF10AUG, TMPM4KLF10AFG

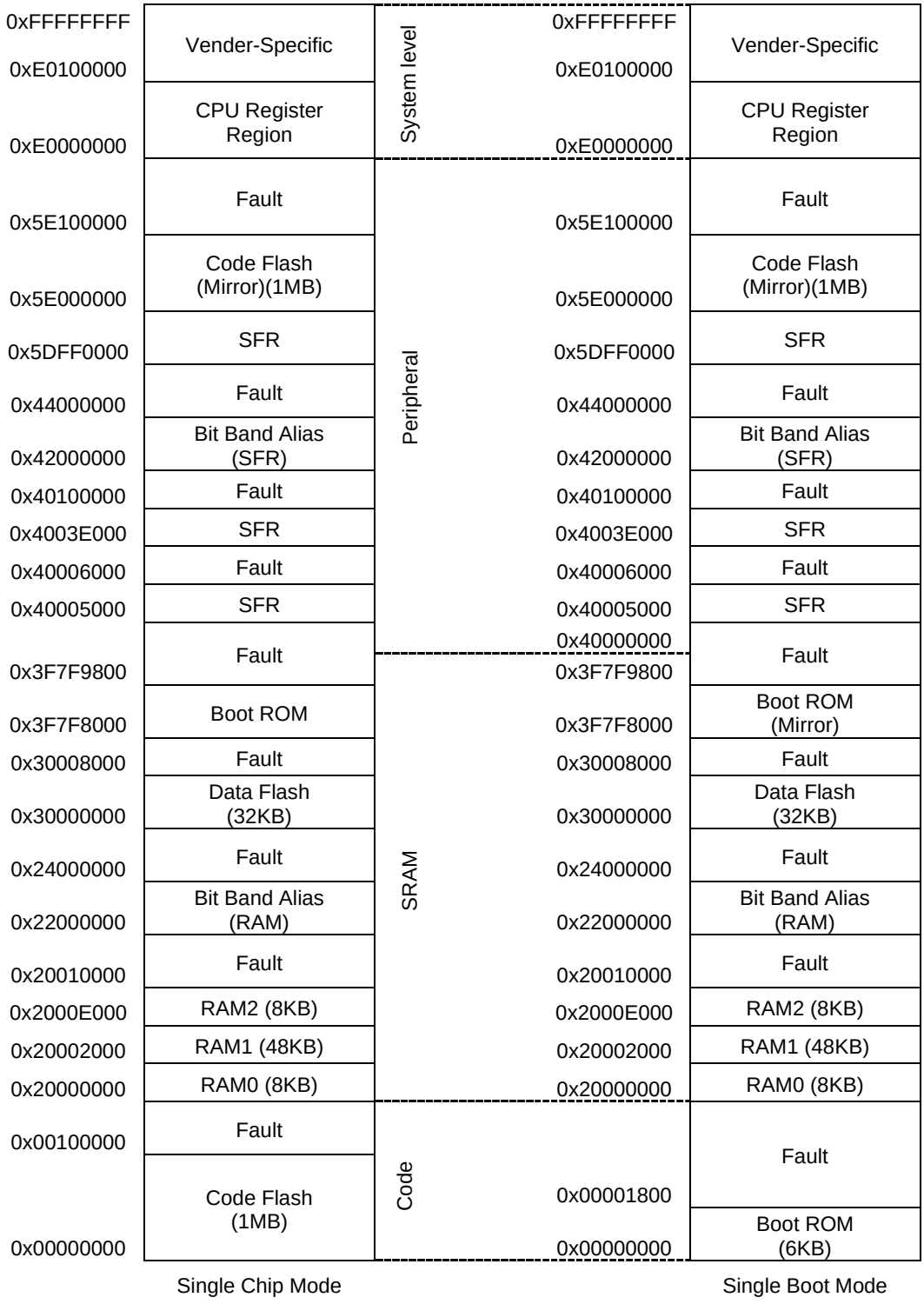

Figure 2.1 TMPM4KxF10A

2.1.2. TMPM4KxFDA

- Code Flash : 512KB
- RAM : 64KB
- Data Flash : 32KB
- Products : TMPM4KNFDADFG, TMPM4KNFDAFG, TMPM4KLFDAUG, TMPM4KLFDAFG

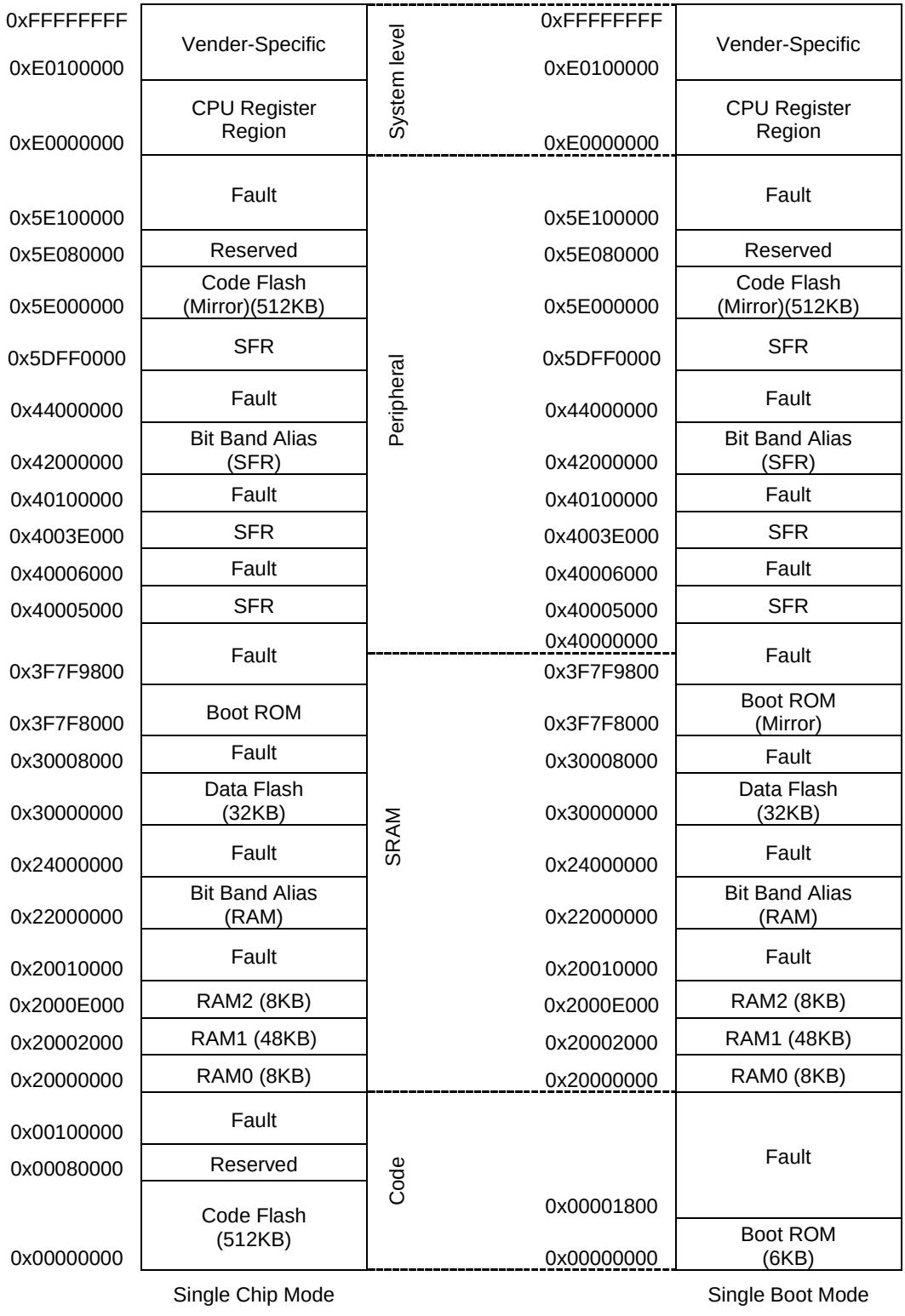

Figure 2.2 TMPM4KxFDA

2.1.3. TMPM4KxFYA

- Code Flash : 256KB
- RAM : 24KB
- Data Flash : 32KB
- Products : TMPM4KLFYAFG, TMPM4KLFYAUG, TMPM4KMFYAFG, TMPM4KNFYAFG, TMPM4KNFYADFG

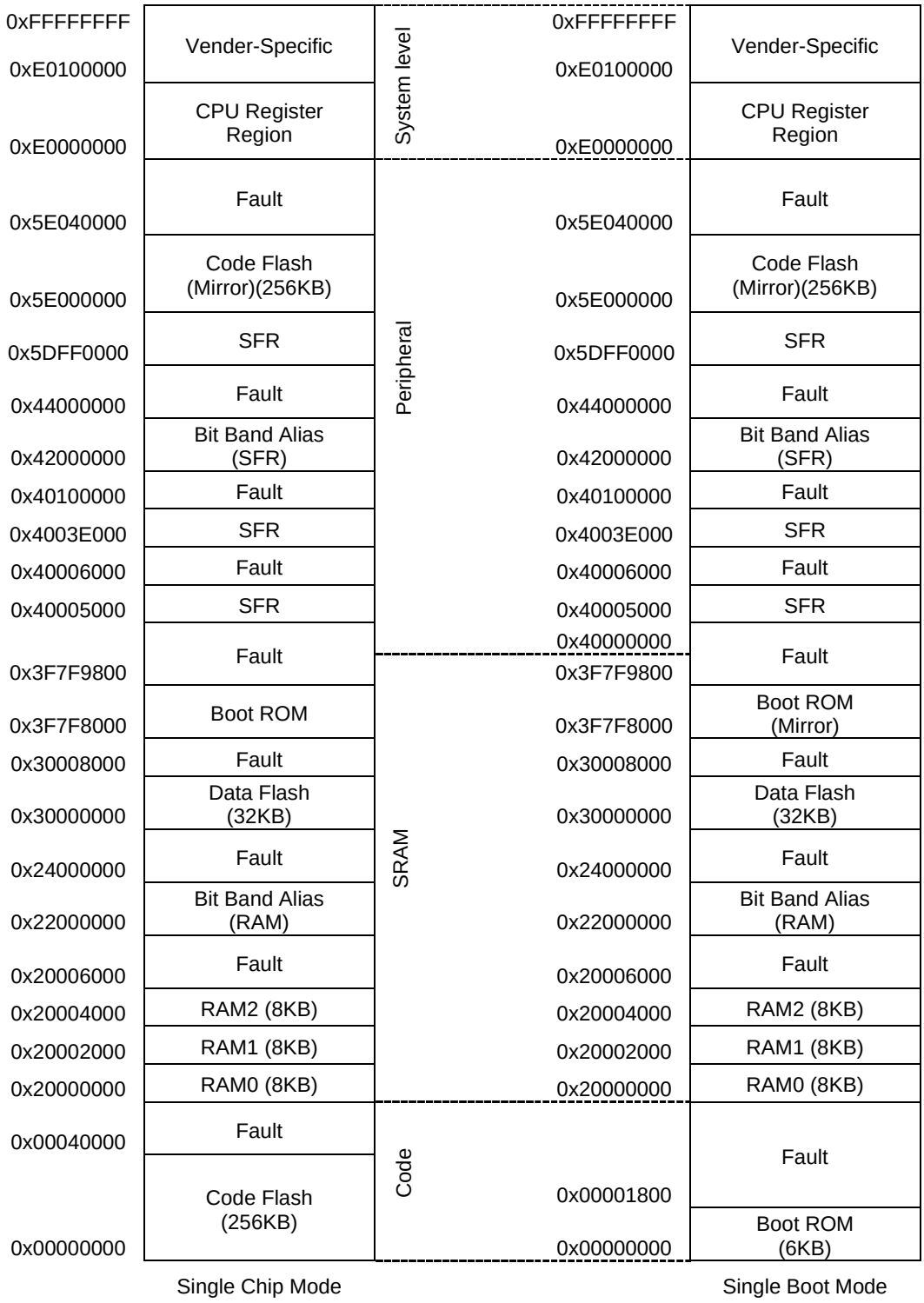

Figure 2.3 TMPM4KxFYA

2.1.4. TMPM4KxFWA

- Code Flash : 128KB
- RAM : 24KB
- Data Flash : 32KB
- Products : TMPM4KLFWAFG, TMPM4KLFWAUG, TMPM4KMFWAFG, TMPM4KNFWAFG, TMPM4KNFWADFG

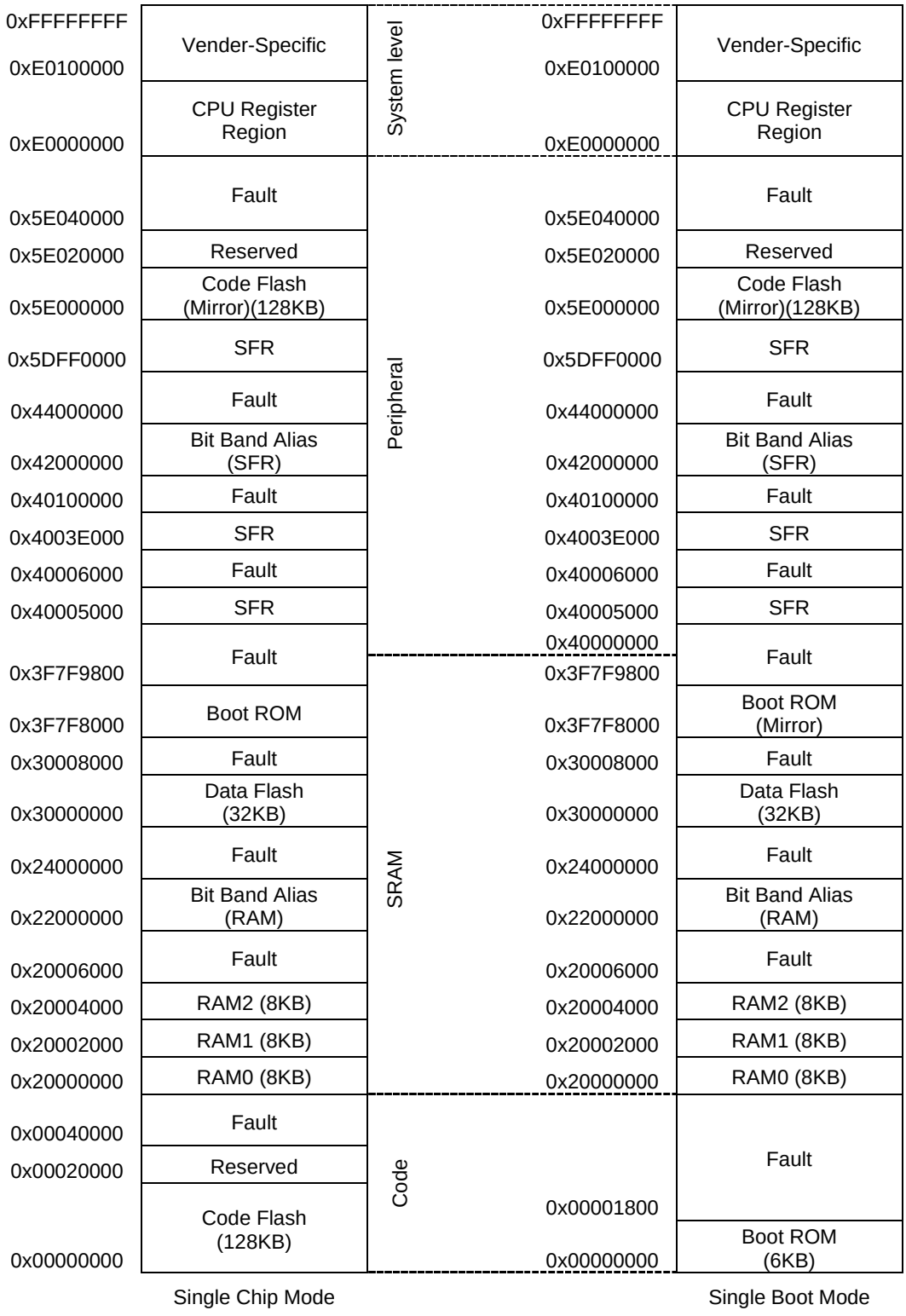

Figure 2.4 TMPM4KxFWA

2.2. Bus Matrix

TMPM4K Group(2) contains the CPU Core of the main master and sub masters. The sub masters include DMA controller (DMAC) and NBDIF.

Main masters connect to slave ports (S0 to S3) of Bus Matrix. In the bus matrix, master ports (M0 to M9) connect to peripheral functions via connections described as (○) or (●) in the following figure. (●) shows a connection to a mirror area.

Sub-masters connect to slave ports (SS0 to SS2) of Bus Matrix. In the bus matrix, sub ports (SM0 to M8) connect to peripheral functions via connections described as (○) or (●) in the following figure.

While multiple slaves are connected to the same bus master line in the Bus Matrix, if multiple slave accesses are generated at the same time, a priority is given to access from a master with the smallest slave number.

2.2.1. Structure

2.2.1.1. Single Chip Mode

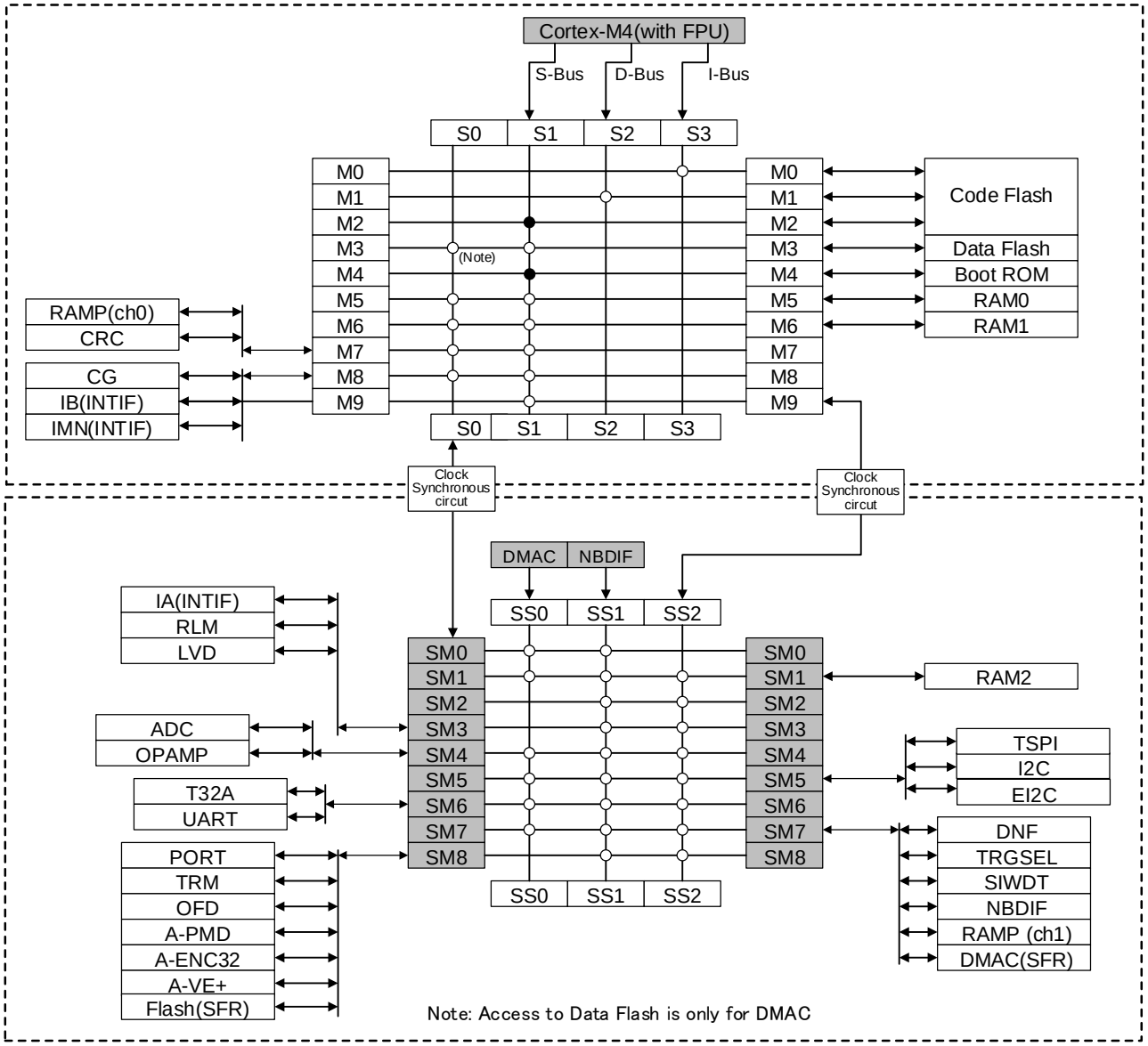

Figure 2.5 Single Chip Mode

2.2.1.2. Single Boot Mode

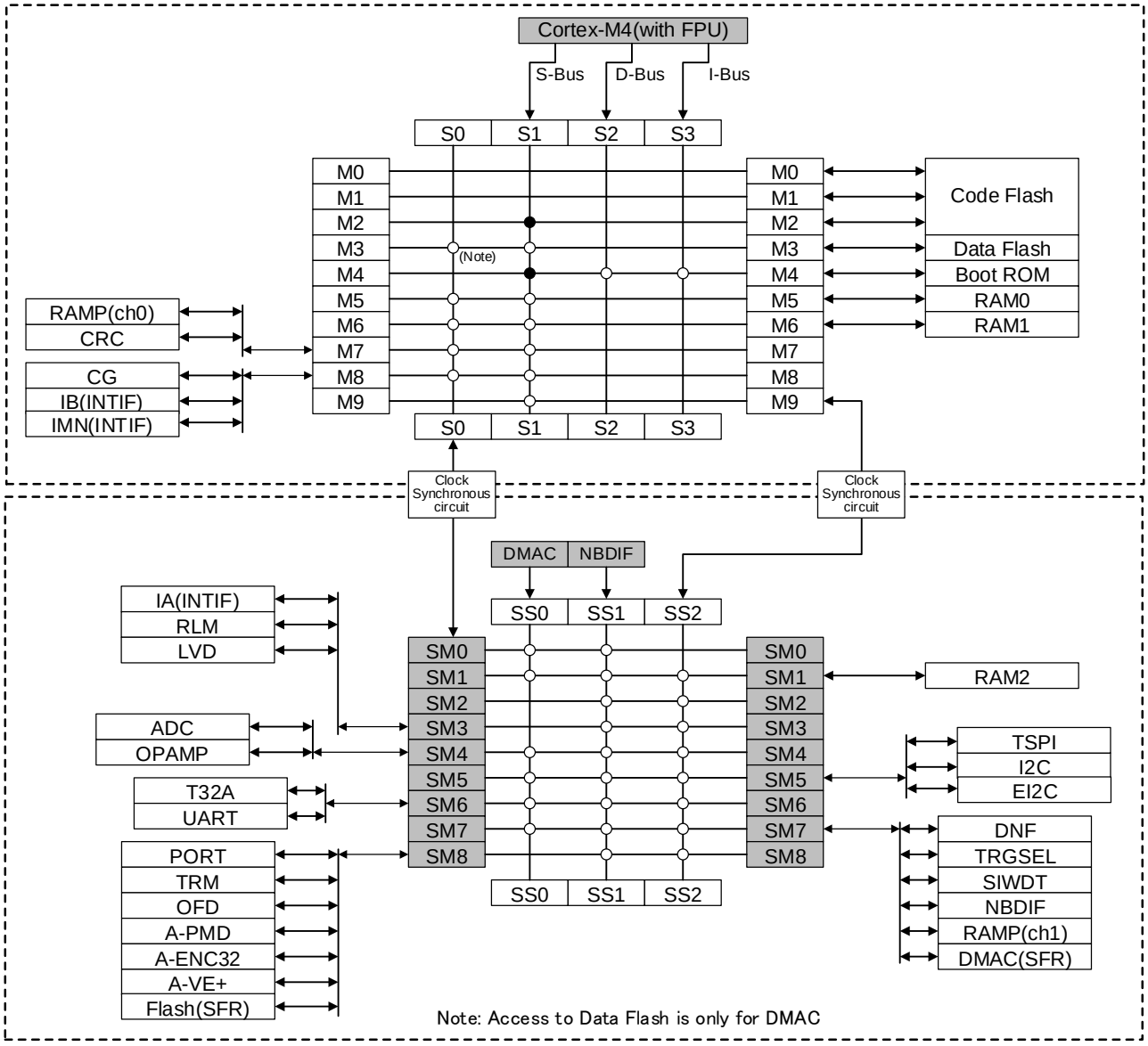

Figure 2.6 Single Boot Mode

2.2.2. Connection table

2.2.2.1. Connection of Memory related

(1) TMPM4KxF10A

- Single Chip Mode

Table 2.1 Single Chip Mode

Start Address	Slave		Sub master		Main master		
			DMAC	NBDIF	Core S-Bus	Core D-Bus	Core I-Bus
			SS0	SS1	S1	S2	S3
0x00000000	Code Flash	M0	Fault	Fault	-	Fault	✓
		M1	Fault	Fault	-	✓	Fault
0x00100000	Fault	-	Fault	Fault	-	Fault	Fault
0x20000000	RAM0	M5	✓	✓	✓	-	-
0x20002000	RAM1	M6	✓	✓	✓	-	-
0x2000E000	RAM2	SM1	✓	✓	✓	-	-
0x20010000	Fault	-	Fault	Fault	Fault	-	-
0x22000000	Bit Band Alias	-	✓	✓	✓	-	-
0x24000000	Fault	-	Fault	Fault	Fault	-	-
0x30000000	Data Flash	M3	✓	Fault	✓	-	-
0x30008000	Fault	-	Fault	Fault	Fault	-	-
0x3F7F8000	Boot ROM	M4	Fault	Fault	✓	-	-
0x3F7F9800	Fault	-	Fault	Fault	Fault	-	-
Refer to "Table 2.9 Connection of peripheral function" for address table during this period.							
0x5E000000	Code Flash (Mirror)	M2	Fault	Fault	✓	-	-

✓: Accessible, -: not accessible, Fault: Fault is caused

- Single Boot Mode

Table 2.2 Single Boot Mode

Start Address	Slave		Sub master		Main master		
			DMAC	NBDIF	Core S-Bus	Core D-Bus	Core I-Bus
			SS0	SS1	S1	S2	S3
0x00000000	Boot ROM	M4	Fault	Fault	-	✓	✓
0x00001800	Fault	-	Fault	Fault	-	-	-
0x20000000	RAM0	M5	✓	✓	✓	-	-
0x20002000	RAM1	M6	✓	✓	✓	-	-
0x2000E000	RAM2	SM1	✓	✓	✓	-	-
0x20010000	Fault	-	Fault	Fault	Fault	-	-
0x22000000	Bit Band Alias	-	Fault	Fault	Fault	-	-
0x24000000	Fault	-	Fault	Fault	Fault	-	-
0x30000000	Data Flash	M3	✓	Fault	✓	-	-
0x30008000	Fault	-	Fault	Fault	Fault	-	-
0x3F7F8000	Boot ROM (Mirror)	M4	Fault	Fault	✓	-	-
0x3F7F9800	Fault	-	Fault	Fault	Fault	-	-
Refer to "Table 2.9 Connection of peripheral function" for address table during this period.							
0x5E000000	Code Flash (Mirror)	M2	Fault	Fault	✓	-	-

✓: Accessible, -: not accessible, Fault: Fault is caused

(2) TMPM4KxFDA

- Single Chip Mode

Table 2.3 Single Chip Mode

Start Address	Slave		Sub master		Main master		
			DMAC	NBDIF	Core S-Bus	Core D-Bus	Core I-Bus
			SS0	SS1	S1	S2	S3
0x00000000	Code Flash	M0	Fault	Fault	-	Fault	✓
		M1	Fault	Fault	-	✓	Fault
0x00080000	Reserved	-	-	-	-	-	-
0x00100000	Fault	-	Fault	Fault	-	Fault	Fault
0x20000000	RAM0	M5	✓	✓	✓	-	-
0x20002000	RAM1	M6	✓	✓	✓	-	-
0x2000E000	RAM2	SM1	✓	✓	✓	-	-
0x20010000	Fault	-	Fault	Fault	Fault	-	-
0x22000000	Bit Band Alias	-	✓	✓	✓	-	-
0x24000000	Fault	-	Fault	Fault	Fault	-	-
0x30000000	Data Flash	M3	✓	Fault	✓	-	-
0x30008000	Fault	-	Fault	Fault	Fault	-	-
0x3F7F8000	Boot ROM	M4	Fault	Fault	✓	-	-
0x3F7F9800	Fault	-	Fault	Fault	Fault	-	-
Refer to "Table 2.9 Connection of peripheral function" for address table during this period.							
0x5E000000	Code Flash (Mirror)	M2	Fault	Fault	✓	-	-

✓: Accessible, -: not accessible, Fault: Fault is caused

- Single Boot Mode

Table 2.4 Single Boot Mode

Start Address	Slave		Sub master		Main master		
			DMAC	NBDIF	Core S-Bus	Core D-Bus	Core I-Bus
			SS0	SS1	S1	S2	S3
0x00000000	Boot ROM	M4	Fault	Fault	-	✓	✓
0x00001800	Fault	-	Fault	Fault	-	-	-
0x20000000	RAM0	M5	✓	✓	✓	-	-
0x20002000	RAM1	M6	✓	✓	✓	-	-
0x2000E000	RAM2	SM1	✓	✓	✓	-	-
0x20010000	Fault	-	Fault	Fault	Fault	-	-
0x22000000	Bit Band Alias	-	Fault	Fault	Fault	-	-
0x24000000	Fault	-	Fault	Fault	Fault	-	-
0x30000000	Data Flash	M3	✓	Fault	✓	-	-
0x30008000	Fault	-	Fault	Fault	Fault	-	-
0x3F7F8000	Boot ROM (Mirror)	M4	Fault	Fault	✓	-	-
0x3F7F9800	Fault	-	Fault	Fault	Fault	-	-
Refer to "Table 2.9 Connection of peripheral function" for address table during this period.							
0x5E000000	Code Flash (Mirror)	M2	Fault	Fault	✓	-	-

✓: Accessible, -: not accessible, Fault: Fault is caused

(3) TMPM4KxFYA

- Single Chip Mode

Table 2.5 Single Chip Mode

Start Address	Slave		Sub master		Main master		
			DMAC	NBDIF	Core S-Bus	Core D-Bus	Core I-Bus
			SS0	SS1	S1	S2	S3
0x00000000	Code Flash	M0	Fault	Fault	-	Fault	✓
		M1	Fault	Fault	-	✓	Fault
0x00040000	Fault	-	Fault	Fault	-	Fault	Fault
0x20000000	RAM0	M5	✓	✓	✓	-	-
0x20002000	RAM1	M6	✓	✓	✓	-	-
0x20004000	RAM2	SM1	✓	✓	✓	-	-
0x20006000	Fault	-	Fault	Fault	Fault	-	-
0x22000000	Bit Band Alias	-	✓	✓	✓	-	-
0x24000000	Fault	-	Fault	Fault	Fault	-	-
0x30000000	Data Flash	M3	✓	Fault	✓	-	-
0x30008000	Fault	-	Fault	Fault	Fault	-	-
0x3F7F8000	Boot ROM	M4	Fault	Fault	✓	-	-
0x3F7F9800	Fault	-	Fault	Fault	Fault	-	-
Refer to "Table 2.9 Connection of peripheral function" for address table during this period.							
0x5E000000	Code Flash (Mirror)	M2	Fault	Fault	✓	-	-

✓: Accessible, -: not accessible, Fault: Fault is caused

- Single Boot Mode

Table 2.6 Single Boot Mode

Start Address	Slave		Sub master		Main master		
			DMAC	NBDIF	Core S-Bus	Core D-Bus	Core I-Bus
			SS0	SS1	S1	S2	S3
0x00000000	Boot ROM	M4	Fault	Fault	-	✓	✓
0x00001800	Fault	-	Fault	Fault	-	-	-
0x20000000	RAM0	M5	✓	✓	✓	-	-
0x20002000	RAM1	M6	✓	✓	✓	-	-
0x20004000	RAM2	SM1	✓	✓	✓	-	-
0x20006000	Fault	-	Fault	Fault	Fault	-	-
0x22000000	Bit Band Alias	-	Fault	Fault	Fault	-	-
0x24000000	Fault	-	Fault	Fault	Fault	-	-
0x30000000	Data Flash	M3	✓	Fault	✓	-	-
0x30008000	Fault	-	Fault	Fault	Fault	-	-
0x3F7F8000	Boot ROM (Mirror)	M4	Fault	Fault	✓	-	-
0x3F7F9800	Fault	-	Fault	Fault	Fault	-	-
Refer to "Table 2.9 Connection of peripheral function" for address table during this period.							
0x5E000000	Code Flash (Mirror)	M2	Fault	Fault	✓	-	-

✓: Accessible, -: not accessible, Fault: Fault is caused

(4) TMPM4KxFWA

- Single Chip Mode

Table 2.7 Single Chip Mode

Start Address	Slave		Sub master		Main master		
			DMAC	NBDIF	Core S-Bus	Core D-Bus	Core I-Bus
			SS0	SS1	S1	S2	S3
0x00000000	Code Flash	M0	Fault	Fault	-	Fault	✓
		M1	Fault	Fault	-	✓	Fault
0x00020000	Reserved	-	-	-	-	-	-
0x00040000	Fault	-	Fault	Fault	-	Fault	Fault
0x20000000	RAM0	M5	✓	✓	✓	-	-
0x20002000	RAM1	M6	✓	✓	✓	-	-
0x20004000	RAM2	SM1	✓	✓	✓	-	-
0x20006000	Fault	-	Fault	Fault	Fault	-	-
0x22000000	Bit Band Alias	-	✓	✓	✓	-	-
0x24000000	Fault	-	Fault	Fault	Fault	-	-
0x30000000	Data Flash	M3	✓	Fault	✓	-	-
0x30008000	Fault	-	Fault	Fault	Fault	-	-
0x3F7F8000	Boot ROM	M4	Fault	Fault	✓	-	-
0x3F7F9800	Fault	-	Fault	Fault	Fault	-	-
Refer to "Table 2.9 Connection of peripheral function" for address table during this period.							
0x5E000000	Code Flash (Mirror)	M2	Fault	Fault	✓	-	-

✓: Accessible, -: not accessible, Fault: Fault is caused

- Single Boot Mode

Table 2.8 Single Boot Mode

Start Address	Slave		Sub master		Main master		
			DMAC	NBDIF	Core S-Bus	Core D-Bus	Core I-Bus
			SS0	SS1	S1	S2	S3
0x00000000	Boot ROM	M4	Fault	Fault	-	✓	✓
0x00001800	Fault	-	Fault	Fault	-	-	-
0x20000000	RAM0	M5	✓	✓	✓	-	-
0x20002000	RAM1	M6	✓	✓	✓	-	-
0x20004000	RAM2	SM1	✓	✓	✓	-	-
0x20006000	Fault	-	Fault	Fault	Fault	-	-
0x22000000	Bit Band Alias	-	Fault	Fault	Fault	-	-
0x24000000	Fault	-	Fault	Fault	Fault	-	-
0x30000000	Data Flash	M3	✓	Fault	✓	-	-
0x30008000	Fault	-	Fault	Fault	Fault	-	-
0x3F7F8000	Boot ROM (Mirror)	M4	Fault	Fault	✓	-	-
0x3F7F9800	Fault	-	Fault	Fault	Fault	-	-
Refer to "Table 2.9 Connection of peripheral function" for address table during this period.							
0x5E000000	Code Flash (Mirror)	M2	Fault	Fault	✓	-	-

✓: Accessible, -: not accessible, Fault: Fault is caused

2.2.2.2. Connection of peripheral function

Table 2.9 Connection of peripheral function

Start Address	Slave		Sub master		Main master		
			DMAC	NBDIF	Core S-Bus	Core D-Bus	Core I-Bus
			SS0	SS1	S1	S2	S3
0x40000000	Fault	-	Fault	Fault	Fault	-	-
0x40005000	Reserved	-	-	-	-	-	-
0x40006000	Fault	-	Fault	Fault	Fault	-	-
0x4003E000	IA (INTIF)	SM3	Fault	✓	✓	-	-
0x4003E400	RLM		Fault	✓	✓	-	-
0x4003EC00	LVD		Fault	✓	✓	-	-
0x40043000	RAMP (ch 0)	M7	✓	✓	✓	-	-
0x40043100	CRC		✓	✓	✓	-	-
0x40043200	Reserved	-	-	-	-	-	-
0x40083000	CG	M8	✓	✓	✓	-	-
0x40083200	IB (INTIF)		✓	✓	✓	-	-
0x40083300	IMN (INTIF)	M8	✓	✓	✓	-	-
0x40083400	Reserved	-	-	-	-	-	-
0x400A0200	DNF	SM7	✓	✓	✓	-	-
0x400A0400	TRGSEL		✓	✓	✓	-	-
0x400A0600	SIWDT		✓	✓	✓	-	-
0x400A0800	DNF		✓	✓	✓	-	-
0x400A2000	NBDIF		✓	✓	✓	-	-
0x400A3000	RAMP (ch 1)		✓	✓	✓	-	-
0x400A4000	DMAC (SFR)		✓	✓	✓	-	-
0x400BA000	ADC	SM4	✓	✓	✓	-	-
0x400BD000	OPAMP		✓	✓	✓	-	-
0x400BD100	Reserved	-	-	-	-	-	-
0x400C1000	T32A	SM6	✓	✓	✓	-	-
0x400CA000	TSPI	SM5	✓	✓	✓	-	-
0x400CE000	UART	SM6	✓	✓	✓	-	-
0x400D1000	I2C	SM5	✓	✓	✓	-	-
0x400D3000	Reserved	-	-	-	-	-	-
0x400D8000	EI2C	SM5	✓	✓	✓	-	-
0x400DA000	Reserved	-	-	-	-	-	-
0x400E0000	PORT	SM8	Fault	✓	✓	-	-
0x400E3100	TRM		Fault	✓	✓	-	-
0x400E4000	OFD		Fault	✓	✓	-	-
0x400E9000	A-PMD		Fault	✓	✓	-	-
0x400EA000	A-ENC32		Fault	✓	✓	-	-
0x400EB000	A-VE+		Fault	✓	✓	-	-
0x40100000	Fault	-	Fault	Fault	Fault	-	-
0x42000000	Bit Band Alias	-	Fault	Fault	✓	-	-
0x44000000	Fault	-	Fault	Fault	Fault	-	-
0x5DFF0000	Flash (SFR)	SM8	Fault	✓	✓	-	-

✓: Accessible, -: not accessible, Fault: Fault is caused

3. Reset and power supply control

3.1. Outlines

Function classification	Factor	Functional Description
Cold reset (Reset by turning on a power supply)	Power On Reset	Reset which occurs at the time of a power supply turning on or turning off.
	LVD reset	Reset which occurs below the set-up voltage
	Reset pin	Reset by a RESET_N pin
	PORF reset	Reset that occurs when power is turned on or off and flash memory and debug circuits are reset with priority.
Warm reset (Reset without turning on a power supply)	Internal reset	Reset by SIWDT, OFD, LVD, LOCKUP, and <SYSRESETREQ>
	Reset pin	Reset by a RESET_N pin
Single Boot starting	Reset pin	After reset is released, it starts from the internal boot ROM.

3.2. Description of function and operation

This chapter describes the power-on, power-off, and reset related items.

Note: Refer to "Electrical Characteristics" of a datasheet for the time and voltage of description of the symbol in a figure.

3.2.1. Cold reset

When turn on a power supply, the stabilization time for the built-in regulator, the built-in flash memory, and the built-in high speed oscillator is necessary. The TXZ+ family automatically inserts a wait time for the stabilization of these circuits.

When turning on the power, make sure that the slope of the power supply voltage rises to the right. If the power supply voltage drops and rises near POR and PORF detection voltage, it may not operate normally even if the power supply voltage rises to the guaranteed operating range thereafter.

3.2.1.1. Reset by a Power On Reset Circuit (without using a RESET_N pin)

After a supply voltage exceeds the release voltage of a Power On Reset (POR), internal reset is deasserted after "Internal initialization time" is elapsed. Please increase a supply voltage goes up into an operating voltage range before "Internal initialization time" is elapsed. The CPU operates after internal reset is released.

After a supply voltage exceeds the release voltage of a Power On Reset (POR), LVD continues to output reset signal until supply voltage exceeds the LVD release voltage.
And internal reset has priority during the time of "Internal initialization time". When rising time of a supply voltage beyond "Internal initialization time", please refer to "3.2.1.3. Continuation of reset by LVD".

For example, if the operating voltage of a circuit board is more than 2.7V, after Power On Reset released, increase a supply voltage to 2.7V before "Internal initialization time" is elapsed. And if the operating voltage of a circuit board is more than 4.5V, after Power On Reset released, increase a supply voltage to 4.5V before "Internal initialization time" is elapsed.

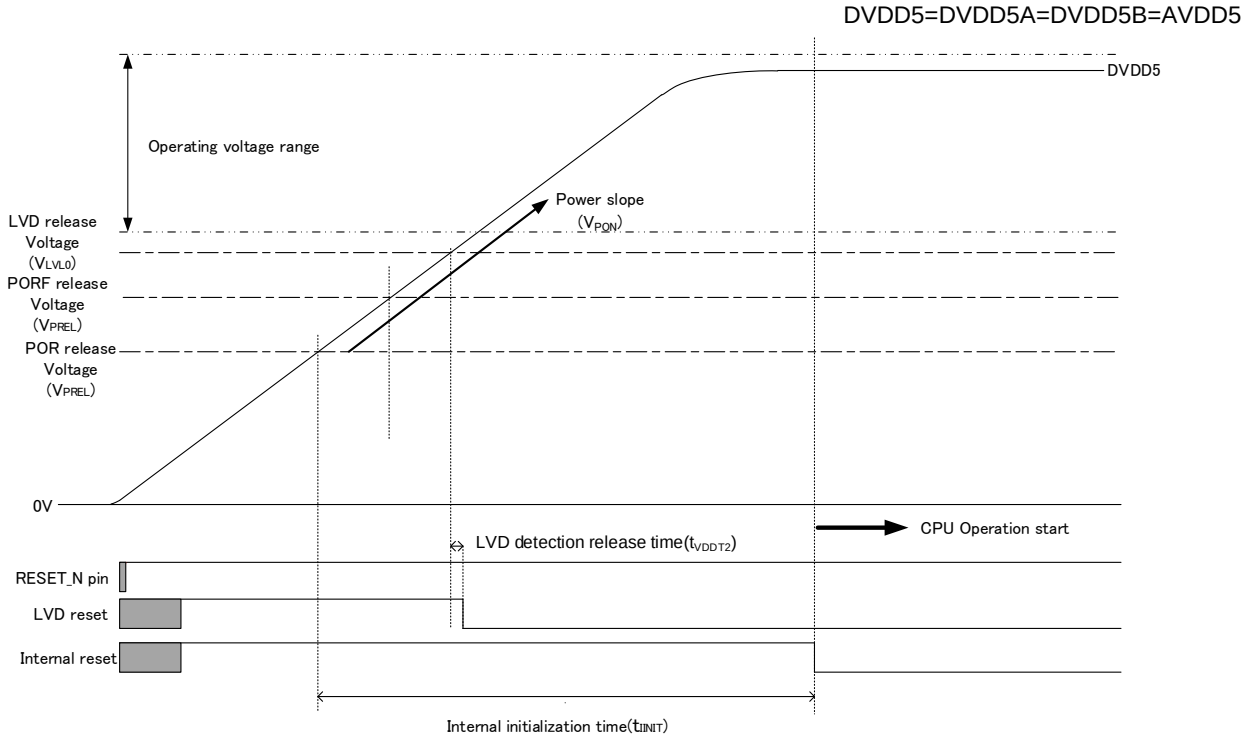

Figure 3.1 The reset operation by a Power On Reset Circuit

Note: When you use only a Power On Reset Circuit without RESET_N pin, the RESET_N pin should input "High" level or opened.

3.2.1.2. Reset by a RESET_N pin

When turn on a power supply, it can control the timing of reset release by using RESET_N pin.

After a supply voltage exceeds the release voltage of a Power On Reset and even after "Internal initialization time" elapsed, if the RESET_N pin is "Low", internal reset continues.
After a supply voltage goes up into an operating voltage range, if a RESET_N pin becomes "High", Internal reset is deasserted after "CPU operation wait time" elapses.

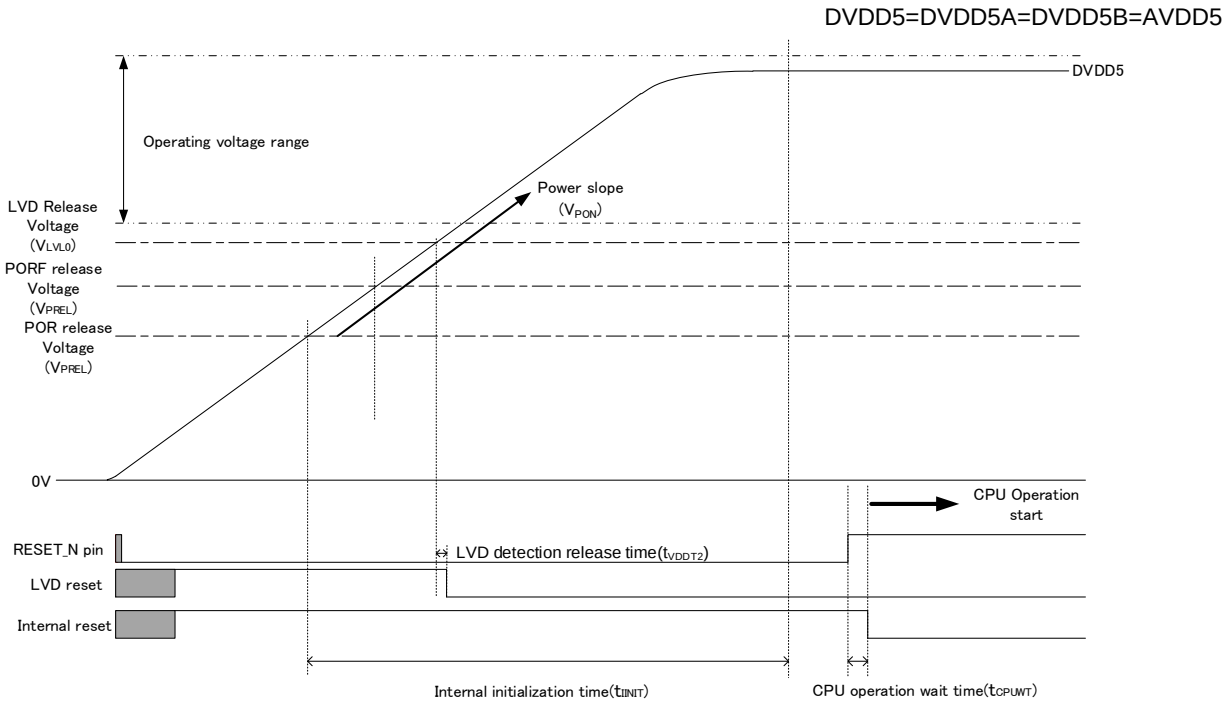

Figure 3.2 Reset operation by a RESET_N pin (1)

In case of RESET_N pin input change from "Low" to "High" before "Internal initialization time" elapses, internal reset signal is released after "Internal initialization time" elapses.

Please goes up a supply voltage into an operating voltage range before "Internal initialization time" elapses. The CPU operates after internal reset release.

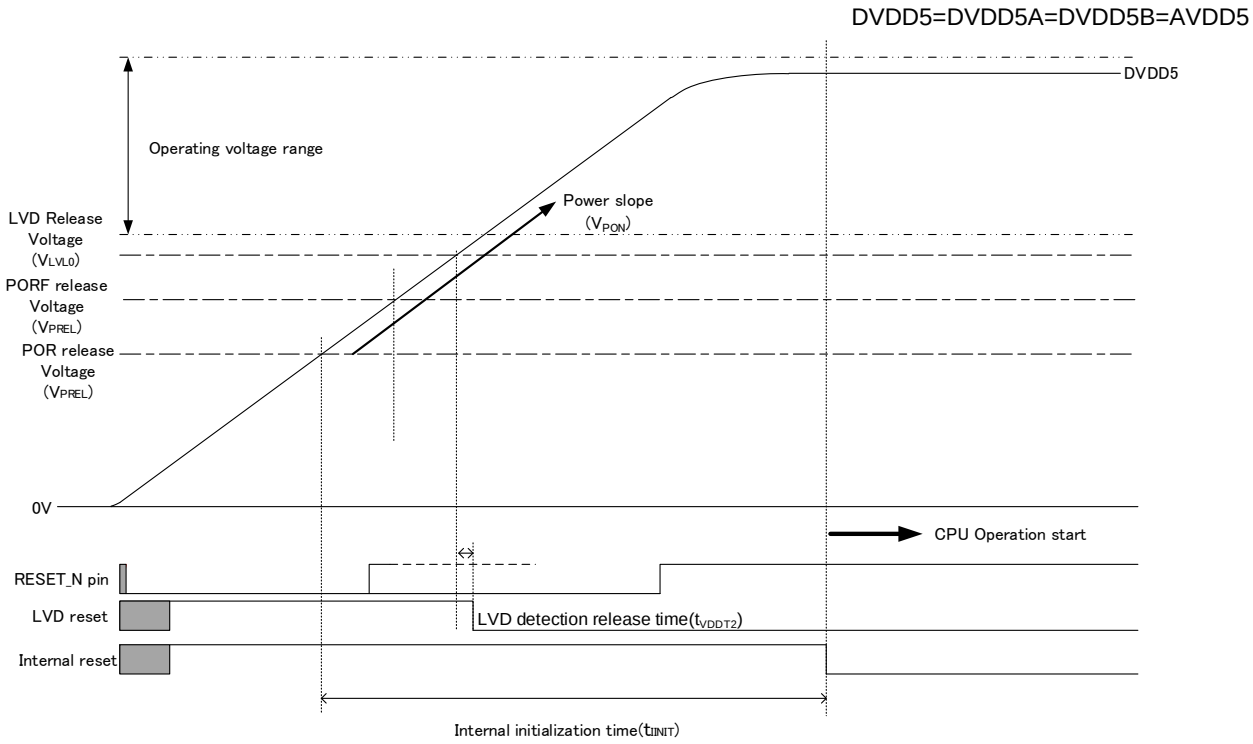

Figure 3.3 Reset operation by a RESET_N pin (2)

3.2.1.3. Continuation of reset by LVD

When the power supply voltage has not exceeded the LVD release voltage even after "Internal initialization time" elapsed, LVD generates the reset signal and the reset state continues. After the power supply voltage exceeds the LVD release voltage and "LVD detection release time" + "CPU operation wait time" elapses, the internal reset is released. And CPU starts operating. Refer to the reference manual "Voltage Detection Circuit" for details of LVD.

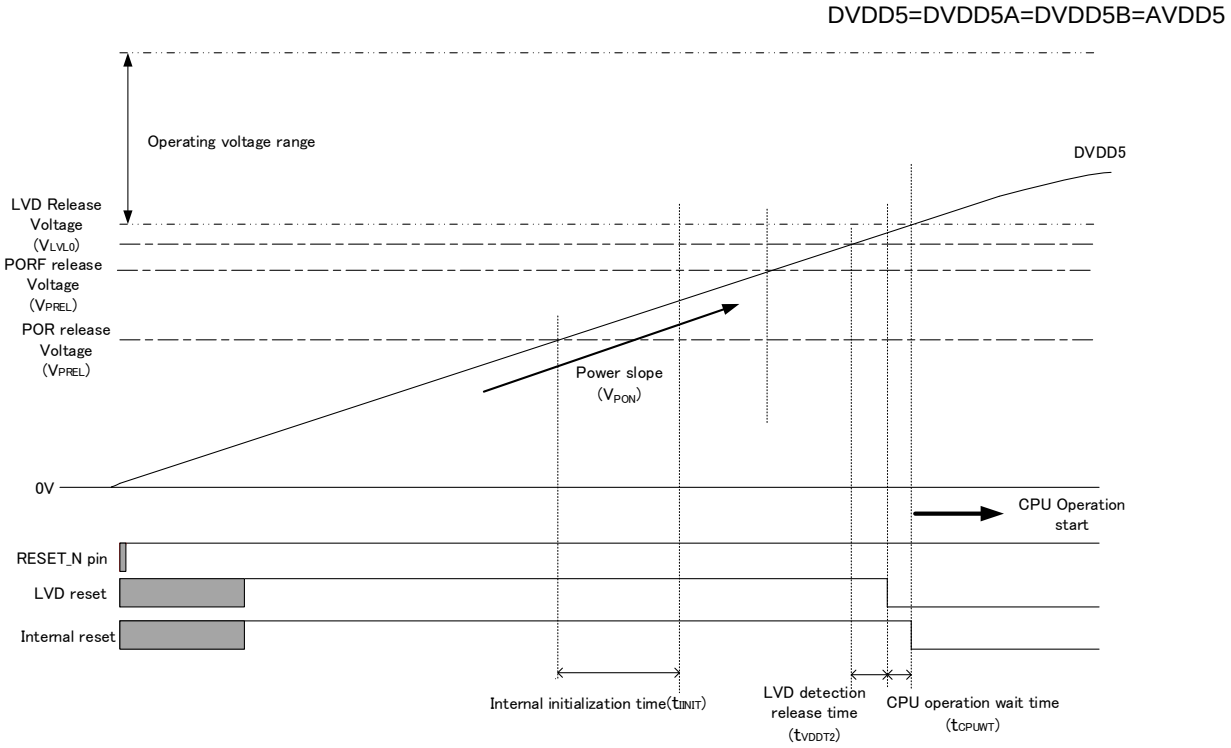

Figure 3.4 Reset operation by LVD reset

3.2.2. Warm reset

3.2.2.1. Warm reset by RESET_N pin

When resetting with the RESET_N pin, set the RESET_N pin to "Low" for 17.2 µs or more while the power supply voltage is within the operating range.

When the "Low" period of a RESET_N pin is longer than "Internal processing time", after a RESET_N pin changes to "High", Internal reset is released after "CPU operation wait time" elapsed.

When the "Low" period of a RESET_N pin is shorter than "Internal processing time", after internal reset is extended and from a RESET_N pin changes to "Low", Internal reset is released after "Internal processing time" + "CPU operation wait time" has elapsed.

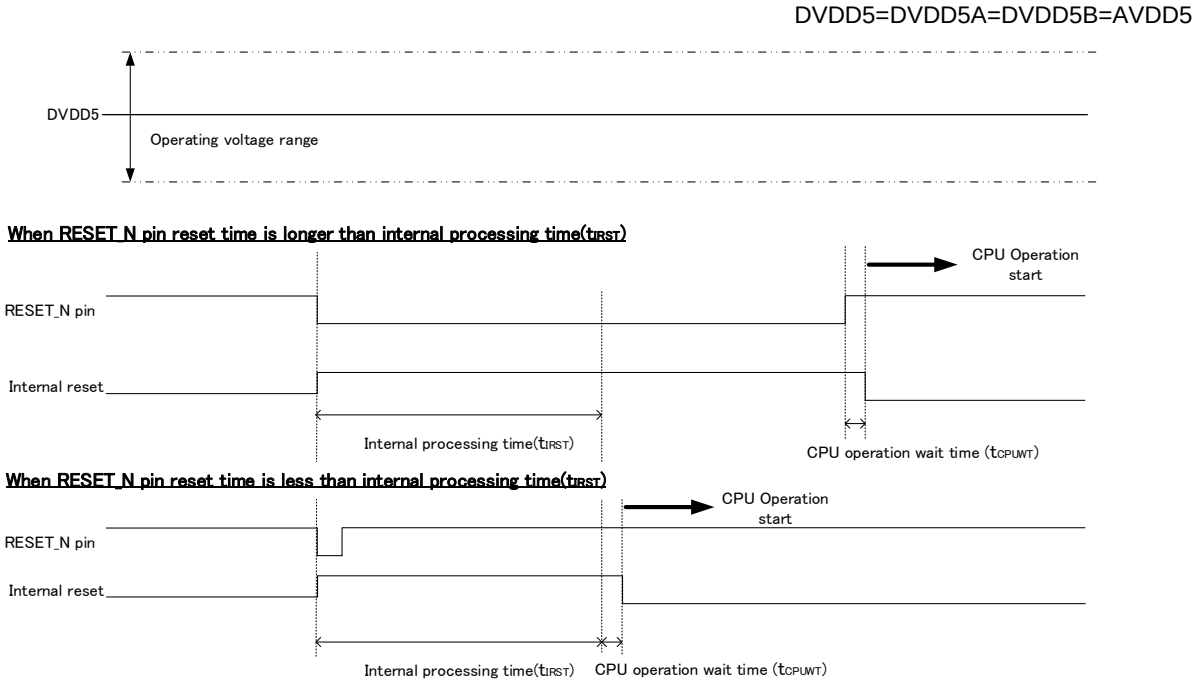

Figure 3.5 Warm reset operation

3.2.2.2. Warm reset by LVD

LVD reset is performed correctly when the LVD reset voltage or less and the power supply voltage is within the operating voltage range. When the power supply voltage drop period is longer than the "internal processing time", internal reset is released after "internal processing time" has elapsed, LVD release voltage has been exceeded, and "LVD detection release time" + "CPU operation wait time" has elapsed. When the power supply voltage drop period is shorter than the "internal processing time", internal reset is released after "internal processing time" + "CPU operation wait time" has elapsed from LVD reset is detected.

3.2.2.3. Warm reset by other internal reset

In case of reset asserted by internal factors, such as SIWDT, OFD, LOCKUP, and <SYSRESETREQ>, Internal reset is released after "Internal processing time" + "CPU operation wait time" elapsed.

3.2.3. Starting in Single Boot Mode

Refer to the reference manual "Flash Memory" for details of "Single Boot Mode".

3.2.3.1. Starting by the RESET_N pin

When "Low" is inputted to a BOOT_N pin, if reset is released (a RESET_N pin "Low" to "High"), "Single Boot Mode" is started.

When turn on power supply, input "Low" to the RESET_N pin longer than "Internal initialization time" to reset. And release reset, after a supply voltage goes up into an operating voltage range.

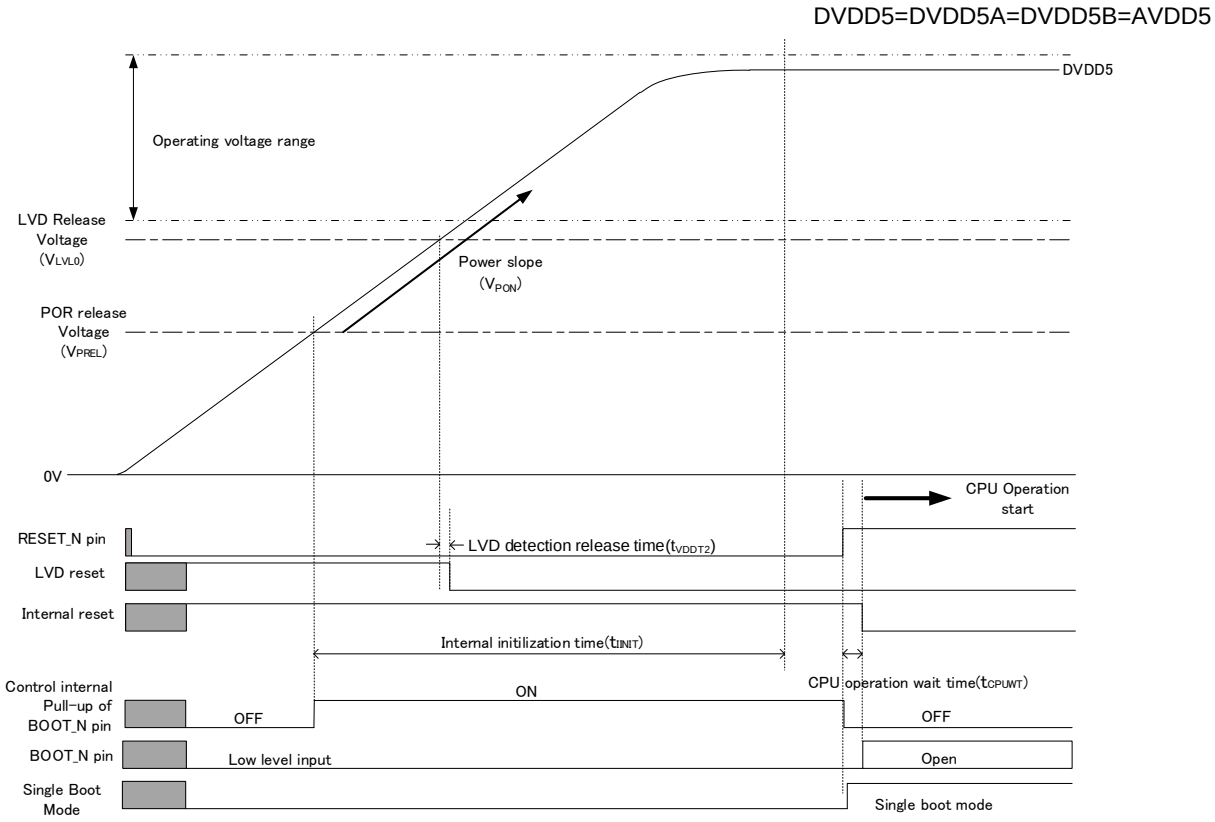

Figure 3.6 When the power supply is on, starting in Single Boot Mode by the RESET_N pin

3.2.3.2. Starting in Single Boot Mode when power supply is stable

When the supply voltage is stable within an operating voltage range, input "Low" to RESET_N pin for reset longer than "Internal processing time", while "Low" is inputted to the BOOT_N pin. And release reset (RESET_N pin to "High").

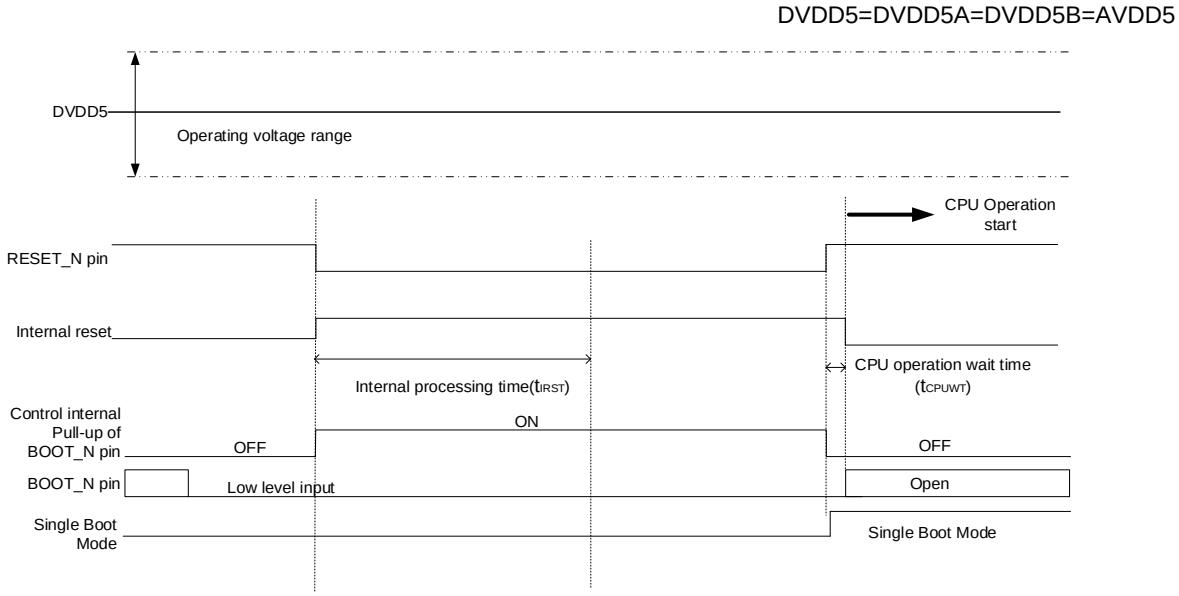

Figure 3.7 Starting in the Single Boot Mode when power supply is stable

3.2.4. Power On Reset Circuit

The Power On Reset Circuit (POR) generates a reset signal when the power is turned on or turned off.

Note: The Power On Reset Circuit may not operate correctly due to the fluctuation of the power supply. Equipment should be designed with full consideration of the electrical characteristics.

The Power On Reset Circuit consists of a Detection voltage generation circuit, a Reference voltage generation circuit, and a Comparator.

The supply voltage has referred to DVDD5 (=DVDD5A=DVDD5B).

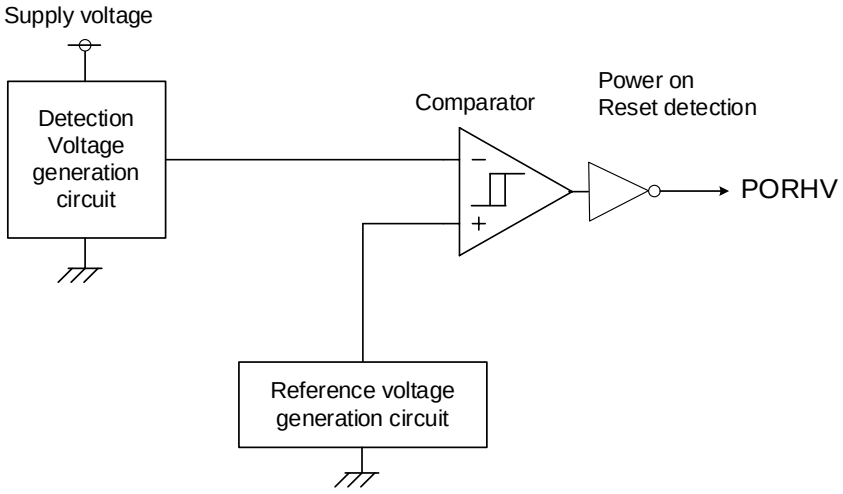

Figure 3.8 Power On Reset Circuit

3.2.4.1. Operation at the time of a power supply

When turn on power supply, while the power supply voltage is lower than Power On Reset Circuit release voltage (V_{PREL}), the Power On Reset detection signal is generated. Refer to "Figure 3.1 The reset operation by a Power On Reset Circuit" for details.

While the Power On Reset signal is generated, the reset is asserted to the CPU and the peripherals.

3.2.4.2. Operation at the time of turn off

When turn off power supply or when the power supply voltage is lower than Power On Reset detection voltage (V_{PDET}), the Power On Reset detection signal is generated.

While the Power On Reset signal is generated, the reset is asserted to the CPU and the peripherals.

3.2.5. Turning off and re-turning on power supply

When a power supply is turned off, a power supply voltage must be down gentler gradient than Max value of "Power gradient (V_{POFF})" specified in "Electrical Characteristics".

3.2.5.1. When using external reset circuit or internal LVD reset output

When the power supply is turned off and the power supply voltage drops below the operation guaranteed voltage, reset is performed with an external reset circuit or built-in LVD (when the voltage is less than the set voltage). After that, from the state where the reset is applied, please follow the same constraints as when turning on the power and turned on the power supply voltage.

3.2.5.2. When not using external reset circuit and internal LVD reset output

When the power supply is turned off and the power supply voltage drops below the operation guaranteed voltage, be sure to lower the power supply voltage below the Power On Reset detection voltage (V_{PDET}) and hold it for 200 µs or more. After that, please follow the same constraints as when turning on the power and turned on the power supply voltage.

When the power supply voltage drops below the Power On Reset detection voltage (V_{PDET}) and cannot be held for 200 µs or more, or when the same constraints as at power on cannot keep, the MCU may not operate properly.

3.2.6. After reset release

All of the control register of the Cortex-M4 processor with FPU and the peripheral function control register (SFR) are initialized by reset. But depend on the reset factor, initialized range is different.

Please refer to "Table 3.1 The reset factor and the range initialized" for the initialized range by each reset factor.

The reset factor when reset occurs can be checked by a reset flag register which are ***[RLMRSTFLG0]*** and ***[RLMRSTFLG1]***. For details of ***[RLMRSTFLG0]*** and ***[RLMRSTFLG1]***, please refer to the reference manual "Exception".

After reset is released, CPU starts operation by a clock of Internal High Speed Oscillator1 (IHOSC1). External clock and PLL multiple circuit should be set if necessary.

3.2.6.1. The reset factor and the reset range

Reset factors and the range initialized are shown in Table 3.1.

Table 3.1 The reset factor and the range initialized

Registers and Peripheral function		Reset factors							
		Cold Reset	Warm Reset						
		POR	Reset Pin	OFD Reset	SIWDT Reset	LVD Reset	CPU <SYS RESET REQ> Reset	CPU LOCKUP Reset	PORF Reset
	Reset signal name	PORHV	RESET_N	OFD RSTOUT	SIWDT RSTOUT	LVD RSTOUT	SYS RESET REQ	LOCKUP RESET REQ	PORF RESET
Reset flag	***[RLMRSTFLG0] [RLMRSTFLG1]***	✓	-	-	-	-	-	-	-
Interrupt control	***[IANIC00]***	✓	✓	✓	✓	✓	✓	✓	✓
	[IBIMCxxx] [IBNIC00]	✓	✓	✓	✓	✓	✓	✓	✓
Flash	***[FCSBMR]***	✓	(Note2)	-	-	(Note2)	-	-	✓
PORT	All the registers	✓	✓	✓	✓	✓	✓	✓	✓
OFD		✓	✓	✓	✓	✓	✓	✓	✓
LVD		✓	✓	-	-	-	-	-	-
Debugging interface		✓	(Note2)	-	-	(Note2)	-	-	✓
Except the above		✓	✓	✓	✓	✓	✓	✓	✓

✓: It is initialized.

-: It is not initialized.

Note1: When reset is performed, the data of built-in RAM will not be guaranteed.

Note2: ***[FCSBMR]*** and Debugging interface are not initialized by resetting in NORMAL and IDLE mode, but they are initialized by resetting in STOP1 mode.

4. Revision History

Table 4.1 Revision History

Revision	Date	Description
1.0	2021-02-09	- First release
1.1	2021-06-15	- 1.3.4.2 NORMAL >>> STOP1 >>> NORMAL Operation mode transition Added note. - 3.2.2.2. Warm reset by LVD Added chapter - 3.2.2.3. Warm reset by other internal reset Modified chapter title. Modified description. - 3.2.6.1. The reset factor and the reset range Modified "Table 3.1 The reset factor and the range initialized"., Added Note2.
1.2	2022-06-24	- 3.2.5. Turning off and re-turning on power supply Modified chapter title. Modified Chapter number. Added description.
1.3	2023-04-14	- Deleted TMPM4KHFYAUG and TMPM4KHFWAUG
3.0	2023-12-25	- Added the bellow products. (overall) TMPM4KNF10ADFG/TMPM4KNFDADFG TMPM4KNF10AFG/TMPM4KNFDAFG TMPM4KLF10AUG/TMPM4KLFDAUG TMPM4KLF10AFG/TMPM4KLFDAFG - 1.3.2.1. IDLE mode transition flow Added note - 2.2.1.1. Single Chip Mode Changed figure 2.5 - 2.2.1.2. Single Boot Mode Changed figure 2.6 - Table 2.9 Connection of peripheral function Changed the start address of TRM

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