32-bit RISC Microcontroller

TMPM4M Group(1)

Reference Manual
Input/Output Ports
(PORT-M4M(1))

Revision 1.3

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Contents

List of Figures

List of Tables

Preface

Related Document

Document name
Product Information
Clock Control and Operation Mode
Exception
Flash Memory
I^2C Interface
I^2C Interface Version A
Serial Peripheral Interface
12-bit Analog to Digital Converter
32-bit Timer Event Counter
Asynchronous Serial Communication Circuit
Advanced Programmable Motor Control Circuit
Advanced Encoder Input Circuit (32bit)
CAN Controller
Debug Interface
Non Break Debug Interface

Conventions

- Numeric formats follow the rules as shown below:
  Hexadecimal: 0xABC
  Decimal: 123 or 0d123 - Only when it needs to be explicitly shown that they are decimal numbers.
  Binary: 0b111 - It is possible to omit the "0b" when the number of bits can be distinctly understood from a sentence.
- "_N" is added to the end of signal names to indicate low active signals.
- It is called "assert" that a signal moves to its active level, "deassert" to its inactive level.
- When two or more signal names are referred, they are described like as [m:n].
  Example: S[3:0] shows four signal names S3, S2, S1 and S0 together.
- The characters surrounded by ***[ ]*** defines the register.
  Example: ***[ABCD]***
- "N" substitutes suffix number of two or more same kind of registers, fields, and bit names.
  Example: ***[XYZ1]***, ***[XYZ2]***, ***[XYZ3]*** → ***[XYZn]***
- "x" substitutes suffix number or character of units and channels in the register list.
- In case of unit, "x" means A, B, and C, ...
  Example: ***[ADACR0]***, ***[ADBCR0]***, ***[ADCCR0]*** → ***[ADxCR0]***
- In case of channel, "x" means 0, 1, and 2, ...
  Example: ***[T32A0RUNA]***, ***[T32A1RUNA]***, ***[T32A2RUNA]*** → ***[T32AxRUNA]***
- The bit range of a register is written like as [m: n].
  Example: Bit[3: 0] expresses the range of bit 3 to 0.
- The configuration value of a register is expressed by either the hexadecimal number or the binary number.
  Example: ***[ABCD]***<EFG> = 0x01 (hexadecimal), ***[XYZn]***<VW> = 1 (binary)
- Word and byte represent the following bit length.
  Byte: 8 bits
  Half word: 16 bits
  Word: 32 bits
  Double word: 64 bits
- Properties of each bit in a register are expressed as follows:
  R: Read only
  W: Write only
  R/W: Read and write are possible.
- Unless otherwise specified, register access supports only word access.
- The register defined as "Reserved" must not be rewritten. Moreover, do not use the read value.
- The value read from the bit having default value of "-" is unknown.
- When a register containing both of writable bits and read-only bits is written, read-only bits should be written with their default value, In the cases that default is "-", follow the definition of each register.
- Reserved bits of the write-only register should be written with their default value. In the cases that default is "-", follow the definition of each register.
- Do not use read-modified-write processing to the register of a definition which is different by writing and read out.

Terms and Abbreviations

Some of abbreviations used in this document are as follows:

CAN	Controller Area Network
I^2C	Inter-Integrated Circuit
JTAG	Joint Test Action Group
NBDIF	Non Break Debug Interface
SW	Serial Wire

1. Outlines

It is described the register and setting of port. A list of the functions is indicated below.

Function classification	Function	Description
Port	-	Programmable pull-up/Programmable pull-down/Open-drain output are possible.
Peripheral Function pins	Clock Output	System clock output is possible.
	External Interrupt	Interrupt pin has a noise filter(Filter width 30ns Typ.).
	32-bit Timer Event Counter	Input capture input pin. Timer output pin.
	Serial Peripheral Interface	Chip select Input 1pin, Chip select Output 2pin, Data input pin, Data output pin, Clock input/output pin
	Asynchronous Serial Communication Circuit	Data input pin, Data output pin, Handshake function pins.
	I2C Interface	Data input/output pin, Clock input/output pin
	I2C Interface Version A	Data input/output pin, Clock input/output pin
	CAN Controller	Data input pin, Data output pin
	Analog to Digital Converter	Analog input pin
	Advanced Programmable Motor Control Circuit	X/Y/Z phase output pins, U/V/W phase output pins, EMG detection input pin, Overvoltage detection input pin.
	Advanced Encoder Input Circuit (32-bit)	Encoder input pin
	Trigger Input	External trigger input pin
Debug pins	JTAG	Test select input pin, Serial clock input pin, Serial data output pin, Serial data input pin, Test reset pin
	SW	Serial wire data input/output pin, Serial wire clock input pin, Serial wire viewer output pin
	Trace	Trace clock output pin, Trace data output 4pins.
	NBDIF	NBD synchronous input pin, NBD clock input pin, NBD data output 4pins.
Control pins	Clock Control	High speed resonator connection pin, External High speed clock input
	BOOT mode control	BOOT mode control pin

2. Function

2.1. Clock Supply

When PORT is used, the corresponding clock enable bits should be set to "1" (Clock supply) in fsys supply stop register A (***[CGFSYSENA]*** and ***[CGFSYSMENA]***), fsys supply stop register B (***[CGFSYSENB]*** and ***[CGFSYSMENB])***, fsys supply stop register C (***[CGFSYSMENC]***), and fc supply stop register (***[CGFCEN]***).

The corresponding registers and the bit locations depend on a product. Some products do not have all registers. For the details, refer to "Clock Control and Operation Mode" in Reference manual.

3. Signal Connection List

This table is sorted the function pins by the signal name of the block diagram which is described each reference manual. Register setting of the peripherals function is being explained in the port order, so please use for a reverse lookup of port name.

The numerical value shows the pin number.

Table 3.1 Signal Connection List: UART ch0,1,2

Related reference manual	Function pin name	Port name	M4MN (QFP100)	M4MN (LQFP100)	M4MM (LQFP80)	M4ML (LQFP64)
Asynchronous Serial Communication Circuit	UT0RXD	PC0	49	46	39	31
		PC1	50	47	40	32
		PN0	12	9	9	-
		PN1	13	10	10	-
	UT0TXDA	PC1	50	47	40	32
		PC0	49	46	39	31
		PN1	13	10	10	-
		PN0	12	9	9	-
	UT0CTS_N	PD2	69	66	-	-
		PN2	14	11	11	-
	UT0RTS_N	PD3	70	67	-	-
		PV1	16	13	-	-
	UT1RXD	PC4	53	50	43	-
		PC5	54	51	44	-
		PU5	9	6	7	7
		PU6	10	7	8	8
	UT1TXDA	PC5	54	51	44	-
		PC4	53	50	43	-
		PU6	10	7	8	8
		PU5	9	6	7	7
	UT1CTS_N	PU4	8	5	6	6
	UT1RTS_N	PU3	7	4	5	5
	UT2RXD	PF0	3	100	1	1
		PF1	2	99	80	64
		PU0	4	1	2	2
		PU1	5	2	3	3
	UT2TXDA	PF1	2	99	80	64
		PF0	3	100	1	1
		PU1	5	2	3	3
		PU0	4	1	2	2

Table 3.2 Signal Connection List: UART ch3/I2C/EI2C/TSPI/CAN

Related reference manual	Function pin name	Port name	M4MN (QFP100)	M4MN (LQFP100)	M4MM (LQFP80)	M4ML (LQFP64)
Asynchronous Serial Communication Circuit	UT3RXD	PF3	100	97	79	-
		PF4	99	96	78	-
		PF6	97	94	77	-
		PF7	96	93	76	-
	UT3TXDA	PF4	99	96	78	-
		PF3	100	97	79	-
		PF7	96	93	76	-
		PF6	97	94	77	-
I^2C Interface	I2C0SDA	PC0	49	46	39	31
	I2C0SCL	PC1	50	47	40	32
	I2C1SDA	PD3	70	67	-	-
		PU0	4	1	2	2
	I2C1SCL	PD4	71	68	-	-
		PU1	5	2	3	3
I^2C Interface Version A	EI2C0SDA	PC0	49	46	39	31
	EI2C0SCL	PC1	50	47	40	32
	EI2C1SDA	PD3	70	67	-	-
		PU0	4	1	2	2
	EI2C1SCL	PD4	71	68	-	-
		PU1	5	2	3	3
Serial Peripheral Interface	TSPI0RXD	PA2	20	17	15	10
		PC3	52	49	42	34
	TSPI0TXD	PA3	21	18	16	11
		PC4	53	50	43	-
	TSPI0SCK	PA4	22	19	17	12
		PC5	54	51	44	-
	TSPI0CSIN	PA0	18	15	13	-
		PC7	56	53	-	-
	TSPI0CS0	PC2	51	48	41	33
	TSPI0CS1	PA1	19	16	14	-
		PC6	55	52	-	-
	TSPI1RXD	PG4	77	74	58	46
		PV1	16	13	-	-
	TSPI1TXD	PG5	78	75	59	47
	TSPI1SCK	PG6	79	76	60	48
	TSPI1CSIN	PG3	76	73	57	45
		PV0	15	12	-	-
	TSPI1CS0	PG2	75	72	56	44
	TSPI1CS1	PG1	74	71	55	-
CAN	CANARX	PA4	22	19	17	12
		PE1	81	78	62	50
	CANATX	PA3	21	18	16	11
		PE0	80	77	61	49

Table 3.3 Signal Connection List: T32A ch0,1

Related reference manual	Function pin name	Port name	M4MN (QFP100)	M4MN (LQFP100)	M4MM (LQFP80)	M4ML (LQFP64)
32-bit Timer Event Counter	T32A00INA0	PA2	20	17	15	10
	T32A00OUTA	PA3	21	18	16	11
	T32A00INB0	PA0	18	15	13	-
	T32A00INB1	PA1	19	16	14	-
	T32A00OUTB	PA4	22	19	17	12
	T32A00INC0	PA2	20	17	15	10
	T32A00OUTC	PA3	21	18	16	11
	T32A01INA0	PF3	100	97	79	-
	T32A01INA1	PF5	98	95	-	-
	T32A01OUTA	PF4	99	96	78	-
	T32A01INB0	PF6	97	94	77	-
	T32A01INB1	PF7	96	93	76	-
	T32A01OUTB	PV0	15	12	-	-
	T32A01INC0	PF3	100	97	79	-
	T32A01INC1	PF5	98	95	-	-
	T32A01OUTC	PF4	99	96	78	-

Table 3.4 Signal Connection List: T32A ch2,3

Related reference manual	Function pin name	Port name	M4MN (QFP100)	M4MN (LQFP100)	M4MM (LQFP80)	M4ML (LQFP64)
32-bit Timer Event Counter	T32A02INA0	PC0	49	46	39	31
		PU1	5	2	3	3
	T32A02INA1	PC6	55	52	-	-
		PU5	9	6	7	7
	T32A02OUTA	PC1	50	47	40	32
		PU2	6	3	4	4
	T32A02INB0	PC7	56	53	-	-
		PU3	7	4	5	5
	T32A02INB1	PD0	67	64	-	-
		PU0	4	1	2	2
	T32A02OUTB	PD1	68	65	-	-
		PU4	8	5	6	6
	T32A02INC0	PC0	49	46	39	31
		PU1	5	2	3	3
	T32A02INC1	PC6	55	52	-	-
		PU4	8	5	6	6
	T32A02OUTC	PC1	50	47	40	32
		PU2	6	3	4	4
	T32A03INA0	PD2	69	66	-	-
		PE1	81	78	62	50
	T32A03INA1	PD3	70	67	-	-
		PE3	83	80	64	52
	T32A03OUTA	PC2	51	48	41	33
		PE2	82	79	63	51
	T32A03INB0	PD4	71	68	-	-
		PE4	84	81	65	53
	T32A03INB1	PD5	72	69	-	-
		PE5	85	82	66	54
	T32A03OUTB	PC3	52	49	42	34
		PE6	86	83	67	55
	T32A03INC0	PD2	69	66	-	-
		PE1	81	78	62	50
	T32A03INC1	PD3	70	67	-	-
		PE3	83	80	64	52
	T32A03OUTC	PC2	51	48	41	33
		PE2	82	79	63	51

Table 3.5 Signal Connection List: T32A ch4,5

Related reference manual	Function pin name	Port name	M4MN (QFP100)	M4MN (LQFP100)	M4MM (LQFP80)	M4ML (LQFP64)
32-bit Timer Event Counter	T32A04INA0	PG0	73	70	54	-
	T32A04INA1	PG1	74	71	55	-
	T32A04OUTA	PG2	75	72	56	44
	T32A04INB0	PG4	77	74	58	46
	T32A04INB1	PG5	78	75	59	47
	T32A04OUTB	PG3	76	73	57	45
	T32A04INC0	PG0	73	70	54	-
	T32A04INC1	PG1	74	71	55	-
	T32A04OUTC	PG2	75	72	56	44
	T32A05INA0	PF0	3	100	1	1
		PN0	12	9	9	-
	T32A05INA1	PF2	1	98	-	-
		PN2	14	11	11	-
	T32A05OUTA	PF1	2	99	80	64
		PN1	13	10	10	-
	T32A05INC0	PF0	3	100	1	1
		PN0	12	9	9	-
	T32A05INC1	PF2	1	98	-	-
		PN2	14	11	11	-
	T32A05OUTC	PF1	2	99	80	64
		PN1	13	10	10	-

Table 3.6 Signal Connection List: ADC

Related reference manual	Function pin name	Port name	M4MN (QFP100)	M4MN (LQFP100)	M4MM (LQFP80)	M4ML (LQFP64)
12-bit Analog to Digital Converter	AINA05	PM2	33	30	-	-
	AINA06	PM1	32	29	-	-
	AINA07	PM0	31	28	-	-
	AINA08	PL7	30	27	25	20
	AINA09	PL6	29	26	24	19
	AINA13	PL5	28	25	23	18
	AINA14	PL3	26	23	21	16
	AINA15	PL1	24	21	19	14
	AINA16	PL0	23	20	18	13
	AINA17	PL2	25	22	20	15
	AINA18	PL4	27	24	22	17
	AINB00	PK0	42	39	34	27
	AINB01	PK1	41	38	33	26
	AINB02	PK2	40	37	32	25
	AINB03	PK3	39	36	31	-
	AINB04	PK4	38	35	30	-
	AINC00	PJ0	48	45	38	30
	AINC01	PJ1	47	44	37	29
	AINC02	PJ2	46	43	36	28
	AINC03	PJ3	45	42	35	-
	AINC04	PJ4	44	41	-	-
	AINC05	PJ5	43	40	-	-

Table 3.7 Signal Connection List: INT

Related reference manual	Function pin name	Port name	M4MN (QFP100)	M4MN (LQFP100)	M4MM (LQFP80)	M4ML (LQFP64)
Exception	INT00	PA2	20	17	15	10
	INT01b	PA3	21	18	16	11
	INT01a	PA4	22	19	17	12
	INT02a	PC1	50	47	40	32
	INT02b	PC6	55	52	-	-
	INT03a	PC3	52	49	42	34
	INT03b	PD2	69	66	-	-
	INT04b	PE1	81	78	62	50
	INT04a	PE3	83	80	64	52
	INT05a	PE5	85	82	66	54
	INT05b	PE6	86	83	67	55
	INT06a	PF1	2	99	80	64
	INT06b	PF2	1	98	-	-
	INT07a	PU1	5	2	3	3
	INT07b	PU2	6	3	4	4
	INT08a	PU3	7	4	5	5
	INT08b	PU4	8	5	6	6
	INT09	PU6	10	7	8	8
	INT10	PC2	51	48	41	33
	INT11a	PE4	84	81	65	53
	INT11b	PE5	85	82	66	54
	INT12	PU0	4	1	2	2
	INT13	PU5	9	6	7	7
	INT14a	PF4	99	96	78	-
	INT14b	PF5	98	95	-	-
	INT15	PA1	19	16	14	-
	INT16a	PN1	13	10	10	-
	INT16b	PN2	14	11	11	-
	INT17b	PD0	67	64	-	-
	INT17a	PD1	68	65	-	-
	INT18b	PD4	71	68	-	-
	INT18a	PD5	72	69	-	-
	INT21	PG3	76	73	57	45

Table 3.8 Signal Connection List: A-PMD/A-ENC32

Related reference manual	Function pin name	Port name	M4MN (QFP100)	M4MN (LQFP100)	M4MM (LQFP80)	M4ML (LQFP64)
Advanced Programmable Motor Control Circuit	EMG0	PB6	63	60	51	41
	OVV0	PB7	64	61	-	-
	UO0	PB0	57	54	45	35
	VO0	PB2	59	56	47	37
	WO0	PB4	61	58	49	39
	XO0	PB1	58	55	46	36
	YO0	PB3	60	57	48	38
	ZO0	PB5	62	59	50	40
	PMD0DBG	PB7	64	61	-	-
		PC2	51	48	41	33
	EMG1	PE6	86	83	67	55
	OVV1	PE7	87	84	-	-
	UO1	PE0	80	77	61	49
	VO1	PE2	82	79	63	51
	WO1	PE4	84	81	65	53
	XO1	PE1	81	78	62	50
	YO1	PE3	83	80	64	52
	ZO1	PE5	85	82	66	54
	PMD1DBG	PC3	52	49	42	34
		PE7	87	84	-	-
	EMG2	PU6	10	7	8	8
	OVV2	PU7	11	8	-	-
	UO2	PU0	4	1	2	2
	VO2	PU2	6	3	4	4
	WO2	PU4	8	5	6	6
	XO2	PU1	5	2	3	3
	YO2	PU3	7	4	5	5
	ZO2	PU5	9	6	7	7
	PMD2DBG	PA2	20	17	15	10
		PU7	11	8	-	-
Advanced Encoder Input Circuit(32-bit)	ENC0A	PN0	12	9	9	-
	ENC0B	PN1	13	10	10	-
	ENC0Z	PN2	14	11	11	-
	ENC1A	PF3	100	97	79	-
	ENC1B	PF4	99	96	78	-
	ENC1Z	PF5	98	95	-	-
	ENC2A	PD3	70	67	-	-
		PU3	7	4	5	5
	ENC2B	PD4	71	68	-	-
		PU5	9	6	7	7
	ENC2Z	PD5	72	69	-	-
		PU6	10	7	8	8

Table 3.9 Signal Connection List: TRGSEL/JTAG/SW/TRACE/NBDIF/Control Pin

Related reference manual	Function pin name	Port name	M4MN (QFP100)	M4MN (LQFP100)	M4MM (LQFP80)	M4ML (LQFP64)
Product Information (Trigger Selector)	TRGIN0	PA2	20	17	15	10
	TRGIN1	PA3	21	18	16	11
	TRGIN2	PA4	22	19	17	12
Debug Interface	TMS	PF0	3	100	-	-
	TCK	PF1	2	99	-	-
	TDO	PF2	1	98	-	-
	TDI	PF3	100	97	-	-
	TRST_N	PF4	99	96	-	-
	SWDIO	PF0	3	100	1	1
	SWCLK	PF1	2	99	80	64
	SWV	PF2	1	98	-	-
Debug Interface (Trace)	TRACECLK	PF5	98	95	-	-
	TRACEDATA0	PF6	97	94	-	-
	TRACEDATA1	PF7	96	93	-	-
	TRACEDATA2	PN0	12	9	-	-
	TRACEDATA3	PN1	13	10	-	-
Non Break Debug Interface	NBDSYNC	PF4	99	96	-	-
	NBDCLK	PF5	98	95	-	-
	NBDDATA0	PF6	97	94	-	-
	NBDDATA1	PF7	96	93	-	-
	NBDDATA2	PN0	12	9	-	-
	NBDDATA3	PN1	13	10	-	-
Clock Control and Operation Mode	X1	PH0	93	90	73	61
	EHCLKIN	PH0	93	90	73	61
	X2	PH1	94	91	74	62
Flash Memory	BOOT_N	PG2	75	72	56	44

4. Registers

The following registers should be set appropriately to use the ports.
Each register is 32 bits. The configuration of the register depends on the port count and its function assignment.
"x" and "n" in the following table show a port name and a function number, respectively.

Register name		Type	Setting value	Description
[PxDATA]	Data Register	R/W	0 or 1	Read from and write to a port.
[PxCR]	Output Control Register	R/W	0: Output disabled 1: Output enabled	Output control
[PxFRn]	Function Register n	R/W	0: PORT 1: Function	Function setting. When 1 is set, the assigned function becomes available. Each function assigned to a port has its own function register. If multiple functions are assigned to one port, only one function should be enabled.
[PxOD]	Open-Drain Control Register	R/W	0: CMOS 1: Open-drain	Programmable open-drain control. The programmable open-drain is a pseudo open- drain. An output buffer is disabled when the output data is 1, which is set by ***[PxOD]*** =1.
[PxPUP]	Pull-up Control Register	R/W	0: Pull-up disabled 1: Pull-up enabled	Programmable pull-up control.
[PxPDN]	Pull-down Control Register	R/W	0: Pull-down disabled 1: Pull-down enabled	Programmable pull-down control.
[PxIE]	Input Control Register	R/W	0: Input disabled 1: Input enabled	Input control. It takes 100ns(Max) that an external data is reflected on ***[PxDATA]*** after the ***[PxIE]*** is enabled.

4.1. List of Register

When the bit which is assigned to no functions is read, 0 is returned. The write to the bit is ignored.

Table 4.1 Ports Base Address

Peripheral function		Channel/unit	Base address
Input/Output ports	PA	-	0x400E0000
	PB	-	0x400E0100
	PC	-	0x400E0200
	PD	-	0x400E0300
	PE	-	0x400E0400
	PF	-	0x400E0500
	PG	-	0x400E0600
	PH	-	0x400E0700
	PJ	-	0x400E0800
	PK	-	0x400E0900
	PL	-	0x400E0A00
	PM	-	0x400E0B00
	PN	-	0x400E0C00
	PU	-	0x400E1000
	PV	-	0x400E1100

Table 4.2 Register List

Register name	Address (Base+)	Port A	Port B	Port C	Port D	Port E	Port F
Data Register	0x0000	*[PADATA]*	*[PBDATA]*	*[PCDATA]*	*[PDDATA]*	*[PEDATA]*	*[PFDATA]*
Output Control Register	0x0004	*[PACR]*	*[PBCR]*	*[PCCR]*	*[PDCR]*	*[PECR]*	*[PFCR]*
Function Register 1	0x0008	*[PAFR1]*	-	*[PCFR1]*	*[PDFR1]*	*[PEFR1]*	*[PFFR1]*
Function Register 2	0x000C	*[PAFR2]*	-	*[PCFR2]*	*[PDFR2]*	-	*[PFFR2]*
Function Register 3	0x0010	-	-	*[PCFR3]*	*[PDFR3]*	-	*[PFFR3]*
Function Register 4	0x0014	*[PAFR4]*	*[PBFR4]*	*[PCFR4]*	*[PDFR4]*	*[PEFR4]*	*[PFFR4]*
Function Register 5	0x0018	*[PAFR5]*	-	*[PCFR5]*	*[PDFR5]*	*[PEFR5]*	*[PFFR5]*
Function Register 6	0x001C	*[PAFR6]*	-	*[PCFR6]*	*[PDFR6]*	*[PEFR6]*	*[PFFR6]*
Function Register 7	0x0020	*[PAFR7]*	-	*[PCFR7]*	-	*[PEFR7]*	*[PFFR7]*
Open-Drain Control Register	0x0028	*[PAOD]*	*[PBOD]*	*[PCOD]*	*[PDOD]*	*[PEOD]*	*[PFOD]*
Pull-up Control Register	0x002C	*[PAPUP]*	*[PBPUP]*	*[PCPUP]*	*[PDPUP]*	*[PEPUP]*	*[PFPUP]*
Pull-down Control Register	0x0030	*[PAPDN]*	*[PBPDN]*	*[PCPDN]*	*[PDPDN]*	*[PEPDN]*	*[PFPDN]*
Input Control Register	0x0038	*[PAIE]*	*[PBIE]*	*[PCIE]*	*[PDIE]*	*[PEIE]*	*[PFIE]*

Register name	Address (Base+)	Port G	Port H	Port J	Port K	Port L	Port M
Data Register	0x0000	*[PGDATA]*	*[PHDATA]*	*[PJDATA]*	*[PKDATA]*	*[PLDATA]*	*[PMDATA]*
Output Control Register	0x0004	*[PGCR]*	-	*[PJCR]*	*[PKCR]*	*[PLCR]*	*[PMCR]*
Function Register 1	0x0008	*[PGFR1]*	-	-	-	-	-
Function Register 2	0x000C	-	-	-	-	-	-
Function Register 3	0x0010	-	-	-	-	-	-
Function Register 4	0x0014	*[PGFR4]*	-	-	-	-	-
Function Register 5	0x0018	*[PGFR5]*	-	-	-	-	-
Function Register 6	0x001C	-	-	-	-	-	-
Function Register 7	0x0020	-	-	-	-	-	-
Open-Drain Control Register	0x0028	*[PGOD]*	-	*[PJOD]*	*[PKOD]*	*[PLOD]*	*[PMOD]*
Pull-up Control Register	0x002C	*[PGPUP]*	-	*[PJPUP]*	*[PKPUP]*	*[PLPUP]*	*[PMPUP]*
Pull-down Control Register	0x0030	*[PGPDN]*	*[PHPDN]*	*[PJPDN]*	*[PKPDN]*	*[PLPDN]*	*[PMPDN]*
Input Control Register	0x0038	*[PGIE]*	*[PHIE]*	*[PJIE]*	*[PKIE]*	*[PLIE]*	*[PMIE]*

Register name	Address (Base+)	Port N	Port U	Port V
Data Register	0x0000	*[PNDATA]*	*[PUDATA]*	*[PVDATA]*
Output Control Register	0x0004	*[PNCR]*	*[PUCR]*	*[PVCR]*
Function Register 1	0x0008	*[PNFR1]*	*[PUFR1]*	*[PVFR1]*
Function Register 2	0x000C	*[PNFR2]*	*[PUFR2]*	*[PVFR2]*
Function Register 3	0x0010	*[PNFR3]*	*[PUFR3]*	-
Function Register 4	0x0014	*[PNFR4]*	*[PUFR4]*	*[PVFR4]*
Function Register 5	0x0018	*[PNFR5]*	*[PUFR5]*	-
Function Register 6	0x001C	*[PNFR6]*	*[PUFR6]*	-
Function Register 7	0x0020	*[PNFR7]*	*[PUFR7]*	-
Open-Drain Control Register	0x0028	*[PNOD]*	*[PUOD]*	*[PVOD]*
Pull-up Control Register	0x002C	*[PNPUP]*	*[PUPUP]*	*[PVPUP]*
Pull-down Control Register	0x0030	*[PNPDN]*	*[PUPDN]*	*[PVPDN]*
Input Control Register	0x0038	*[PNIE]*	*[PUIE]*	*[PVIE]*

Note: Do not access the address described as "-".

4.2. List of Port Functions and Settings

It is explained about the viewpoint of a port register setting table.

The column of ***[PxFRn]*** shows the function register which should be set. When this register is set to "1", the corresponding function is enabled. (x is a port name and n is a function number.)

The bit in the N/A in the tables returns "0" when it is read. The write to the bit is ignored.

"0" or "1" in the tables shows the value which should be set. "0/1" means either value can be set.

PORT	Reset statu / Function	Input/Output	PORT Type	Control register [PADATA]	[PACR]	[PAFRn]	[PAOD]	[PAPUP]	[PAPDN]	[PAIE]
PA0	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	TSPI0CSIN	Input	FTU1a	0/1	0	***[PAFR1]***	0/1	0/1	0/1	1
	T32A00INB0	Input	FTU1a	0/1	0	***[PAFR4]***	0/1	0/1	0/1	1
PA4	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT01a	Input	FTU4a	0/1	0	0	0/1	0/1	0/1	1
	TSPI0SCK	Input	FTU1a	0/1	0	***[PAFR1]***	0/1	0/1	0/1	1
		Output	FTU1a	0/1	1		0/1	0/1	0/1	0
	CANARX	Input	FTU1a	0/1	0	***[PAFR2]***	0/1	0/1	0/1	1
	T32A00OUTB	Output	FTU1a	0/1	1	***[PAFR4]***	0/1	0/1	0/1	0
	TRGIN2	Input	FTU1a	0/1	0	***[PAFR7]***	0/1	0/1	0/1	1

[PxFRn]	Pin						
	TSPI0CSIN	T32A00INB0	TSPI0SCK	CANARX	T32A00OUTB	TRGIN2	Input Port Output Port
[PAFR1]<bit0>	1	0	0	0	0	0	0
[PAFR4]<bit0>	0	1	0	0	0	0	0
[PAFR1]<bit4>	0	0	1	0	0	0	0
[PAFR2]<bit4>	0	0	0	1	0	0	0
[PAFR4]<bit4>	0	0	0	0	1	0	0
[PAFR7]<bit4>	0	0	0	0	0	1	0

4.2.1. Setting of Using Alternated Pin

To use the alternated pins as peripheral function output pins, set the peripheral function (***[PxFRn]***<bit m>=1) that uses the function register and enable output control register (***[PxCR]***<bit m>=1), and then set the peripheral functions. If output is enabled before setting the function register, the data register value of the port is output until the function register is set.

To use the alternated pins as input pins of the peripheral function, set the input control register of the port (***[PxIE]***<bit m>=1) and set the peripheral function that uses the function register (***[PxFRn]***<bit m>=1), and then set the peripheral functions.

To use peripheral functions such as I^2C, set the input control register of the port (***[PxIE]***<bit m>=1), set the peripheral function (***[PxFRn]***<bit m>=1) and set the output control register to output enable (***[PxCR]***<bit m>=1), and then set the peripheral function.

- When multiple functions are assigned same pin, please choose only one function for usage.
- When same function are assigned multiple pins, please the function use exclusively.

4.2.2. PORT A

Table 4.3 Port A Registers Setting

PORT	Reset status / Function	Input/output	PORT type	Control register						
				[PADATA]	*[PACR]*	*[PAFRn]*	*[PAOD]*	*[PAPUP]*	*[PAPDN]*	*[PAIE]*
PA0	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	TSPI0CSIN	Input	FTU1a	0/1	0	***[PAFR1]***	0/1	0/1	0/1	1
	T32A00INB0	Input	FTU1a	0/1	0	***[PAFR4]***	0/1	0/1	0/1	1
PA1	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT15	Input	FTU4a	0/1	0	0	0/1	0/1	0/1	1
	TSPI0CS1	Output	FTU1a	0/1	1	***[PAFR1]***	0/1	0/1	0/1	0
	T32A00INB1	Input	FTU1a	0/1	0	***[PAFR4]***	0/1	0/1	0/1	1
PA2	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT00	Input	FTU4a	0/1	0	0	0/1	0/1	0/1	1
	TSPI0RXD	Input	FTU1a	0/1	0	***[PAFR1]***	0/1	0/1	0/1	1
	T32A00INA0	Input	FTU1a	0/1	0	***[PAFR4]***	0/1	0/1	0/1	1
	T32A00INC0	Input	FTU1a	0/1	0	***[PAFR5]***	0/1	0/1	0/1	1
	PMD2DBG	Output	FTU1a	0/1	1	***[PAFR6]***	0/1	0/1	0/1	0
	TRGIN0	Input	FTU1a	0/1	0	***[PAFR7]***	0/1	0/1	0/1	1
PA3	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT01b	Input	FTU4a	0/1	0	0	0/1	0/1	0/1	1
	TSPI0TXD	Output	FTU2a	0/1	1	***[PAFR1]***	0/1	0/1	0/1	0
	CANATX	Output	FTU1a	0/1	1	***[PAFR2]***	0/1	0/1	0/1	0
	T32A00OUTA	Output	FTU1a	0/1	1	***[PAFR4]***	0/1	0/1	0/1	0
	T32A00OUTC	Output	FTU1a	0/1	1	***[PAFR5]***	0/1	0/1	0/1	0
	TRGIN1	Input	FTU1a	0/1	0	***[PAFR7]***	0/1	0/1	0/1	1
PA4	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT01a	Input	FTU4a	0/1	0	0	0/1	0/1	0/1	1
	TSPI0SCK	Input	FTU1a	0/1	0	***[PAFR1]***	0/1	0/1	0/1	1
		Output	FTU1a	0/1	1		0/1	0/1	0/1	0
	CANARX	Input	FTU1a	0/1	0	***[PAFR2]***	0/1	0/1	0/1	1
	T32A00OUTB	Output	FTU1a	0/1	1	***[PAFR4]***	0/1	0/1	0/1	0
	TRGIN2	Input	FTU1a	0/1	0	***[PAFR7]***	0/1	0/1	0/1	1

4.2.3. PORT B

Table 4.4 Port B Registers Setting

PORT	Reset status / Function	Input/output	PORT type	Control register						
				[PBDATA]	*[PBCR]*	*[PBFRn]*	*[PBOD]*	*[PBPUP]*	*[PBPDN]*	*[PBIE]*
PB0	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	UO0	Output	FTU2a	0/1	1	***[PBFR4]***	0/1	0/1	0/1	0
PB1	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	XO0	Output	FTU2a	0/1	1	***[PBFR4]***	0/1	0/1	0/1	0
PB2	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	VO0	Output	FTU2a	0/1	1	***[PBFR4]***	0/1	0/1	0/1	0
PB3	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	YO0	Output	FTU2a	0/1	1	***[PBFR4]***	0/1	0/1	0/1	0
PB4	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	WO0	Output	FTU2a	0/1	1	***[PBFR4]***	0/1	0/1	0/1	0
PB5	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	ZO0	Output	FTU2a	0/1	1	***[PBFR4]***	0/1	0/1	0/1	0
PB6	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	EMG0	Input	FTU1a	0/1	0	***[PBFR4]***	0/1	0/1	0/1	1
PB7	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	OVV0	Input	FTU1a	0/1	0	***[PBFR4]***	0/1	0/1	0/1	1
	PMD0DBG	Output	FTU1a	0/1	1	***[PBFR5]***	0/1	0/1	0/1	0

4.2.4. PORT C

Table 4.5 Port C Registers Setting

PORT	Reset status / Function	Input/output	PORT type	Control register						
				[PCDATA]	*[PCCR]*	*[PCFRn]*	*[PCOD]*	*[PCPUP]*	*[PCPDN]*	*[PCIE]*
PC0	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	UT0TXDA	Output	FTU1a	0/1	1	***[PCFR1]***	0/1	0/1	0/1	0
	UT0RXD	Input	FTU1a	0/1	0	***[PCFR2]***	0/1	0/1	0/1	1
	EI2C0SDA	Input/Output	FTU1a	0/1	1	***[PCFR3]***	1	0/1	0/1	1
	I2C0SDA	Input/Output	FTU1a	0/1	1	***[PCFR4]***	1	0/1	0/1	1
	T32A02INA0	Input	FTU1a	0/1	0	***[PCFR5]***	0/1	0/1	0/1	1
	T32A02INC0	Input	FTU1a	0/1	0	***[PCFR6]***	0/1	0/1	0/1	1
PC1	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT02a	Input	FTU4a	0/1	0	0	0/1	0/1	0/1	1
	UT0RXD	Input	FTU1a	0/1	0	***[PCFR1]***	0/1	0/1	0/1	1
	UT0TXDA	Output	FTU1a	0/1	1	***[PCFR2]***	0/1	0/1	0/1	0
	EI2C0SCL	Input/Output	FTU1a	0/1	1	***[PCFR3]***	1	0/1	0/1	1
	I2C0SCL	Input/Output	FTU1a	0/1	1	***[PCFR4]***	1	0/1	0/1	1
	T32A02OUTA	Output	FTU1a	0/1	1	***[PCFR5]***	0/1	0/1	0/1	0
	T32A02OUTC	Output	FTU1a	0/1	1	***[PCFR6]***	0/1	0/1	0/1	0
PC2	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT10	Input	FTU4a	0/1	0	0	0/1	0/1	0/1	1
	TSPI0CS0	Output	FTU1a	0/1	1	***[PCFR3]***	0/1	0/1	0/1	0
	T32A03OUTA	Output	FTU1a	0/1	1	***[PCFR5]***	0/1	0/1	0/1	0
	T32A03OUTC	Output	FTU1a	0/1	1	***[PCFR6]***	0/1	0/1	0/1	0
	PMD0DBG	Output	FTU1a	0/1	1	***[PCFR7]***	0/1	0/1	0/1	0
PC3	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT03a	Input	FTU4a	0/1	0	0	0/1	0/1	0/1	1
	TSPI0RXD	Input	FTU1a	0/1	0	***[PCFR3]***	0/1	0/1	0/1	1
	T32A03OUTB	Output	FTU1a	0/1	1	***[PCFR5]***	0/1	0/1	0/1	0
	PMD1DBG	Output	FTU1a	0/1	1	***[PCFR7]***	0/1	0/1	0/1	0
PC4	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	UT1TXDA	Output	FTU1a	0/1	1	***[PCFR1]***	0/1	0/1	0/1	0
	UT1RXD	Input	FTU1a	0/1	0	***[PCFR2]***	0/1	0/1	0/1	1
	TSPI0TXD	Output	FTU2a	0/1	1	***[PCFR3]***	0/1	0/1	0/1	0
PC5	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	UT1RXD	Input	FTU1a	0/1	0	***[PCFR1]***	0/1	0/1	0/1	1
	UT1TXDA	Output	FTU1a	0/1	1	***[PCFR2]***	0/1	0/1	0/1	0
	TSPI0SCK	Output	FTU1a	0/1	1	***[PCFR3]***	0/1	0/1	0/1	0
		Input	FTU1a	0/1	0		0/1	0/1	0/1	1

PORT	Reset status / Function	Input/output	PORT type	Control register						
				[PCDATA]	*[PCCR]*	*[PCFRn]*	*[PCOD]*	*[PCPUP]*	*[PCPDN]*	*[PCIE]*
PC6	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT02b	Input	FTU4a	0/1	0	0	0/1	0/1	0/1	1
	TSPI0CS1	Output	FTU1a	0/1	1	***[PCFR3]***	0/1	0/1	0/1	0
	T32A02INA1	Input	FTU1a	0/1	0	***[PCFR5]***	0/1	0/1	0/1	1
	T32A02INC1	Input	FTU1a	0/1	0	***[PCFR6]***	0/1	0/1	0/1	1
PC7	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	TSPI0CSIN	Input	FTU1a	0/1	0	***[PCFR3]***	0/1	0/1	0/1	1
	T32A02INB0	Input	FTU1a	0/1	0	***[PCFR5]***	0/1	0/1	0/1	1

4.2.5. PORT D

Table 4.6 Port D Registers Setting

PORT	Reset status / Function	Input/output	PORT type	Control register						
				[PDDATA]	*[PDCR]*	*[PDFRn]*	*[PDOD]*	*[PDPUP]*	*[PDPDN]*	*[PDIE]*
PD0	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT17b	Input	FTU4a	0/1	0	0	0/1	0/1	0/1	1
	T32A02INB1	Input	FTU1a	0/1	0	***[PDFR4]***	0/1	0/1	0/1	1
PD1	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT17a	Input	FTU4a	0/1	0	0	0/1	0/1	0/1	1
	T32A02OUTB	Output	FTU1a	0/1	1	***[PDFR4]***	0/1	0/1	0/1	0
PD2	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT03b	Input	FTU4a	0/1	0	0	0/1	0/1	0/1	1
	UT0CTS_N	Input	FTU1a	0/1	0	***[PDFR1]***	0/1	0/1	0/1	1
	T32A03INA0	Input	FTU1a	0/1	0	***[PDFR4]***	0/1	0/1	0/1	1
	T32A03INC0	Input	FTU1a	0/1	0	***[PDFR5]***	0/1	0/1	0/1	1
PD3	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	UT0RTS_N	Output	FTU1a	0/1	1	***[PDFR1]***	0/1	0/1	0/1	0
	I2C1SDA	Input/Output	FTU1a	0/1	1	***[PDFR2]***	1	0/1	0/1	1
	EI2C1SDA	Input/Output	FTU1a	0/1	1	***[PDFR3]***	1	0/1	0/1	1
	T32A03INA1	Input	FTU1a	0/1	0	***[PDFR4]***	0/1	0/1	0/1	1
	T32A03INC1	Input	FTU1a	0/1	0	***[PDFR5]***	0/1	0/1	0/1	1
	ENC2A	Input	FTU1a	0/1	0	***[PDFR6]***	0/1	0/1	0/1	1
PD4	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT18b	Input	FTU4a	0/1	0	0	0/1	0/1	0/1	1
	I2C1SCL	Input/Output	FTU1a	0/1	1	***[PDFR2]***	1	0/1	0/1	1
	EI2C1SCL	Input/Output	FTU1a	0/1	1	***[PDFR3]***	1	0/1	0/1	1
	T32A03INB0	Input	FTU1a	0/1	0	***[PDFR4]***	0/1	0/1	0/1	1
	ENC2B	Input	FTU1a	0/1	0	***[PDFR6]***	0/1	0/1	0/1	1
PD5	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT18a	Input	FTU4a	0/1	0	0	0/1	0/1	0/1	1
	T32A03INB1	Input	FTU1a	0/1	0	***[PDFR4]***	0/1	0/1	0/1	1
	ENC2Z	Input	FTU1a	0/1	0	***[PDFR6]***	0/1	0/1	0/1	1

4.2.6. PORT E

Table 4.7 Port E Registers Setting

PORT	Reset status / Function	Input/output	PORT type	Control register						
				[PEDATA]	*[PECR]*	*[PEFRn]*	*[PEOD]*	*[PEPUP]*	*[PEPDN]*	*[PEIE]*
PE0	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	CANATX	Output	FTU1a	0/1	1	***[PEFR1]***	0/1	0/1	0/1	0
	UO1	Output	FTU2a	0/1	1	***[PEFR6]***	0/1	0/1	0/1	0
PE1	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT04b	Input	FTU4a	0/1	0	0	0/1	0/1	0/1	1
	CANARX	Input	FTU1a	0/1	0	***[PEFR1]***	0/1	0/1	0/1	1
	T32A03INA0	Input	FTU1a	0/1	0	***[PEFR4]***	0/1	0/1	0/1	1
	T32A03INC0	Input	FTU1a	0/1	0	***[PEFR5]***	0/1	0/1	0/1	1
	XO1	Output	FTU2a	0/1	1	***[PEFR6]***	0/1	0/1	0/1	0
PE2	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	T32A03OUTA	Output	FTU1a	0/1	1	***[PEFR4]***	0/1	0/1	0/1	0
	T32A03OUTC	Output	FTU1a	0/1	1	***[PEFR5]***	0/1	0/1	0/1	0
	VO1	Output	FTU2a	0/1	1	***[PEFR6]***	0/1	0/1	0/1	0
PE3	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT04a	Input	FTU4a	0/1	0	0	0/1	0/1	0/1	1
	T32A03INA1	Input	FTU1a	0/1	0	***[PEFR4]***	0/1	0/1	0/1	1
	T32A03INC1	Input	FTU1a	0/1	0	***[PEFR5]***	0/1	0/1	0/1	1
	YO1	Output	FTU2a	0/1	1	***[PEFR6]***	0/1	0/1	0/1	0
PE4	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT11a	Input	FTU4a	0/1	0	0	0/1	0/1	0/1	1
	T32A03INB0	Input	FTU1a	0/1	0	***[PEFR4]***	0/1	0/1	0/1	1
	WO1	Output	FTU2a	0/1	1	***[PEFR6]***	0/1	0/1	0/1	0
PE5	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT05a	Input	FTU4a	0/1	0	0	0/1	0/1	0/1	1
	INT11b	Input	FTU4a	0/1	0	0	0/1	0/1	0/1	1
	T32A03INB1	Input	FTU1a	0/1	0	***[PEFR4]***	0/1	0/1	0/1	1
	ZO1	Output	FTU2a	0/1	1	***[PEFR6]***	0/1	0/1	0/1	0
PE6	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT05b	Input	FTU4a	0/1	0	0	0/1	0/1	0/1	1
	T32A03OUTB	Output	FTU1a	0/1	1	***[PEFR4]***	0/1	0/1	0/1	0
	EMG1	Input	FTU1a	0/1	0	***[PEFR6]***	0/1	0/1	0/1	1
PE7	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	OVV1	Input	FTU1a	0/1	0	***[PEFR6]***	0/1	0/1	0/1	1
	PMD1DBG	Output	FTU1a	0/1	1	***[PEFR7]***	0/1	0/1	0/1	0

4.2.7. PORT F

Table 4.8 Port F Registers Setting

PORT	Reset status / Function	Input/output	PORT type	Control register						
				[PFDATA]	*[PFCR]*	*[PFFRn]*	*[PFOD]*	*[PFPUP]*	*[PFPDN]*	*[PFIE]*
PF0	After reset (TMS/SWDIO)		FTU2a	0	1(Note)	***[PFFR7]***	0	1	0	1
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	UT2TXDA	Output	FTU1a	0/1	1	***[PFFR1]***	0/1	0/1	0/1	0
	UT2RXD	Input	FTU1a	0/1	0	***[PFFR2]***	0/1	0/1	0/1	1
	T32A05INA0	Input	FTU1a	0/1	0	***[PFFR4***	0/1	0/1	0/1	1
	T32A05INC0	Input	FTU1a	0/1	0	***[PFFR5]***	0/1	0/1	0/1	1
PF1	After reset (TCK/SWCLK)		FTU2a	0	0	***[PFFR7]***	0	0	1	1
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT06a	Input	FTU4a	0/1	0	0	0/1	0/1	0/1	1
	UT2RXD	Input	FTU1a	0/1	0	***[PFFR1]***	0/1	0/1	0/1	1
	UT2TXDA	Output	FTU1a	0/1	1	***[PFFR2]***	0/1	0/1	0/1	0
	T32A05OUTA	Output	FTU1a	0/1	1	***[PFFR4***	0/1	0/1	0/1	0
	T32A05OUTC	Output	FTU1a	0/1	1	***[PFFR5]***	0/1	0/1	0/1	0
PF2	After reset (TDO/SWV)		FTU2a	0	1(Note)	***[PFFR7]***	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT06b	Input	FTU4a	0/1	0	0	0/1	0/1	0/1	1
	T32A05INA1	Input	FTU1a	0/1	0	***[PFFR4]***	0/1	0/1	0/1	1
	T32A05INC1	Input	FTU1a	0/1	0	***[PFFR5]***	0/1	0/1	0/1	1
PF3	After reset (TDI)		FTU2a	0	0	***[PFFR7]***	0	1	0	1
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	UT3TXDA	Output	FTU1a	0/1	1	***[PFFR1]***	0/1	0/1	0/1	0
	UT3RXD	Input	FTU1a	0/1	0	***[PFFR2]***	0/1	0/1	0/1	1
	T32A01INA0	Input	FTU1a	0/1	0	***[PFFR4]***	0/1	0/1	0/1	1
	T32A01INC0	Input	FTU1a	0/1	0	***[PFFR5]***	0/1	0/1	0/1	1
	ENC1A	Input	FTU1a	0/1	0	***[PFFR6]***	0/1	0/1	0/1	1
PF4	After reset (TRST_N)		FTU3a	0	0	***[PFFR7]***	0	1	0	1
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT14a	Input	FTU4a	0/1	0	0	0/1	0/1	0/1	1
	UT3RXD	Input	FTU1a	0/1	0	***[PFFR1]***	0/1	0/1	0/1	1
	UT3TXDA	Output	FTU1a	0/1	1	***[PFFR2]***	0/1	0/1	0/1	0
	NBDSYNC	Input	FTU2c	0/1	0	***[PFFR3]***	0/1	0/1	0/1	1
	T32A01OUTA	Output	FTU1a	0/1	1	***[PFFR4]***	0/1	0/1	0/1	0
	T32A01OUTC	Output	FTU1a	0/1	1	***[PFFR5]***	0/1	0/1	0/1	0
	ENC1B	Input	FTU1a	0/1	0	***[PFFR6]***	0/1	0/1	0/1	1
PF5	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT14b	Input	FTU4a	0/1	0	0	0/1	0/1	0/1	1
	NBDCLK	Input	FTU2c	0/1	0	***[PFFR3]***	0/1	0/1	0/1	1
	T32A01INA1	Input	FTU1a	0/1	0	***[PFFR4]***	0/1	0/1	0/1	1
	T32A01INC1	Input	FTU1a	0/1	0	***[PFFR5]***	0/1	0/1	0/1	1
	ENC1Z	Input	FTU1a	0/1	0	***[PFFR6]***	0/1	0/1	0/1	1
	TRACECLK	Output	FTU1a	0/1	1	***[PFFR7]***	0/1	0/1	0/1	0

PORT	Reset status / Function	Input/output	PORT type	Control register						
				[PFDATA]	*[PFCR]*	*[PFFRn]*	*[PFOD]*	*[PFPUP]*	*[PFPDN]*	*[PFIE]*
PF6	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	UT3TXDA	Output	FTU1a	0/1	1	***[PFFR1]***	0/1	0/1	0/1	0
	UT3RXD	Input	FTU1a	0/1	0	***[PFFR2]***	0/1	0/1	0/1	1
	NBDDATA0	Input/Output	FTU2c	0/1	1	***[PFFR3]***	0/1	0/1	0/1	1
	T32A01INB0	Input	FTU1a	0/1	0	***[PFFR4]***	0/1	0/1	0/1	1
	TRACEDATA0	Output	FTU1a	0/1	1	***[PFFR7]***	0/1	0/1	0/1	0
PF7	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	UT3RXD	Input	FTU1a	0/1	0	***[PFFR1]***	0/1	0/1	0/1	1
	UT3TXDA	Output	FTU1a	0/1	1	***[PFFR2]***	0/1	0/1	0/1	0
	NBDDATA1	Input/Output	FTU2c	0/1	1	***[PFFR3]***	0/1	0/1	0/1	1
	T32A01INB1	Input	FTU1a	0/1	0	***[PFFR4]***	0/1	0/1	0/1	1
	TRACEDATA1	Output	FTU1a	0/1	1	***[PFFR7]***	0/1	0/1	0/1	0

Note: When receiving the command from TOOL, it becomes output.

4.2.8. PORT G

Table 4.9 Port G Registers Setting

PORT	Reset status / Function	Input/output	PORT type	Control register						
				[PGDATA]	*[PGCR]*	*[PGFRn]*	*[PGOD]*	*[PGPUP]*	*[PGPDN]*	*[PGIE]*
PG0	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	T32A04INA0	Input	FTU1a	0/1	0	***[PGFR4]***	0/1	0/1	0/1	1
	T32A04INC0	Input	FTU1a	0/1	0	***[PGFR5]***	0/1	0/1	0/1	1
PG1	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	TSPI1CS1	Output	FTU1a	0/1	1	***[PGFR1]***	0/1	0/1	0/1	0
	T32A04INA1	Input	FTU1a	0/1	0	***[PGFR4]***	0/1	0/1	0/1	1
	T32A04INC1	Input	FTU1a	0/1	0	***[PGFR5]***	0/1	0/1	0/1	1
PG2	During reset (BOOT_N)	Input	FTU16a	0	0	0	0	0 (Note)	0	N/A (Note)
	After reset			0	0	0	0	0	0	N/A
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	N/A
	TSPI1CS0	Output	FTU1a	0/1	1	***[PGFR1]***	0/1	0/1	0/1	N/A
	T32A04OUTA	Output	FTU1a	0/1	1	***[PGFR4]***	0/1	0/1	0/1	N/A
	T32A04OUTC	Output	FTU1a	0/1	1	***[PGFR5]***	0/1	0/1	0/1	N/A
PG3	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT21	Input	FTU4a	0/1	0	0	0/1	0/1	0/1	1
	TSPI1CSIN	Input	FTU1a	0/1	0	***[PGFR1]***	0/1	0/1	0/1	1
	T32A04OUTB	Output	FTU1a	0/1	1	***[PGFR4]***	0/1	0/1	0/1	0
PG4	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	TSPI1RXD	Input	FTU1a	0/1	0	***[PGFR1]***	0/1	0/1	0/1	1
	T32A04INB0	Input	FTU1a	0/1	0	***[PGFR4]***	0/1	0/1	0/1	1
PG5	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	TSPI1TXD	Output	FTU2a	0/1	1	***[PGFR1]***	0/1	0/1	0/1	0
	T32A04INB1	Input	FTU1a	0/1	0	***[PGFR4]***	0/1	0/1	0/1	1
PG6	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	TSPI1SCK	Input	FTU1a	0/1	0	***[PGFR1]***	0/1	0/1	0/1	1
		Output	FTU1a	0/1	1		0/1	0/1	0/1	0

Note: During the reset period by the reset pin (RESET_N), the state of the BOOT_N pin can be input to PG2 with pull-up enabled and input enabled.

4.2.9. PORT H

Table 4.10 Port H Registers Setting

PORT	Reset status / Function	Input/output	PORT type	Control register						
				[PHDATA]	*[PHCR]*	*[PHFRn]*	*[PHOD]*	*[PHPUP]*	*[PHPDN]*	*[PHIE]*
PH0	After reset			0	N/A	N/A	N/A	N/A	0	0
	Input Port	Input		0/1	N/A	N/A	N/A	N/A	0/1	1
	X1	Input	FTU11a	0/1	N/A	N/A	N/A	N/A	0	0
	EHCLKIN	input	FTU11a	0/1	N/A	N/A	N/A	N/A	0	0/1
PH1	After reset			0	N/A	N/A	N/A	N/A	0	0
	Input Port	Input		0/1	N/A	N/A	N/A	N/A	0/1	1
	X2	Output	FTU11a	0/1	N/A	N/A	N/A	N/A	0	0

4.2.10. PORT J

Table 4.11 Port J Registers Setting

PORT	Reset status / Function	Input/output	PORT type	Control register						
				[PJDATA]	*[PJCR]*	*[PJFRn]*	*[PJOD]*	*[PJPUP]*	*[PJPDN]*	*[PJIE]*
PJ0	After reset			0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0
	AINC00	Input	FTU5a	0/1	0	N/A	0/1	0	0	0
PJ1	After reset			0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0
	AINC01	Input	FTU5a	0/1	0	N/A	0/1	0	0	0
PJ2	After reset			0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0
	AINC02	Input	FTU5a	0/1	0	N/A	0/1	0	0	0
PJ3	After reset			0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0
	AINC03	Input	FTU5a	0/1	0	N/A	0/1	0	0	0
PJ4	After reset			0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0
	AINC04	Input	FTU5a	0/1	0	N/A	0/1	0	0	0
PJ5	After reset	Input		0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0
	AINC05	Input	FTU5a	0/1	0	N/A	0/1	0	0	0

Note: When using analog input(AINCx), ***[PJCR]*** should be output disable "0",***[PJIE]*** should be input disable "0", ***[PJPUP]*** should be pull-up disable"0" and ***[PJPDN]*** should be pull-down disable "0".

4.2.11. PORT K

Table 4.12 Port K Registers Setting

PORT	Reset status / Function	Input/output	PORT type	Control register						
				[PKDATA]	*[PKCR]*	*[PKFRn]*	*[PKOD]*	*[PKPUP]*	*[PKPDN]*	*[PKIE]*
PK0	After reset	Input		0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0
	AINB00	Input	FTU5a	0/1	0	N/A	0/1	0	0	0
PK1	After reset	Input		0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0
	AINB01	Input	FTU5a	0/1	0	N/A	0/1	0	0	0
PK2	After reset	Input		0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0
	AINB02	Input	FTU5a	0/1	0	N/A	0/1	0	0	0
PK3	After reset	Input		0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0
	AINB03	Input	FTU5a	0/1	0	N/A	0/1	0	0	0
PK4	After reset	Input		0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0
	AINB04	Input	FTU5a	0/1	0	N/A	0/1	0	0	0

Note: When using analog input(AINBx), ***[PKCR]*** should be output disable "0",***[PKIE]*** should be input disable "0", ***[PKPUP]*** should be pull-up disable"0" and ***[PKPDN]*** should be pull-down disable "0".

4.2.12. PORT L

Table 4.13 Port L Registers Setting

PORT	Reset status / Function	Input/output	PORT type	Control register						
				[PLDATA]	*[PLCR]*	*[PLFRn]*	*[PLOD]*	*[PLPUP]*	*[PLPDN]*	*[PLIE]*
PL0	After reset			0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0
	AINA16	Input	FTU5a	0/1	0	N/A	0/1	0	0	0
PL1	After reset			0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0
	AINA15	Input	FTU5a	0/1	0	N/A	0/1	0	0	0
PL2	After reset			0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0
	AINA17	Input	FTU5a	0/1	0	N/A	0/1	0	0	0
PL3	After reset			0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0
	AINA14	Input	FTU5a	0/1	0	N/A	0/1	0	0	0
PL4	After reset			0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0
	AINA18	Input	FTU5a	0/1	0	N/A	0/1	0	0	0
PL5	After reset			0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0
	AINA13	Input	FTU5a	0/1	0	N/A	0/1	0	0	0
PL6	After reset			0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0
	AINA09	Input	FTU5a	0/1	0	N/A	0/1	0	0	0
PL7	After reset			0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0
	AINA08	Input	FTU5a	0/1	0	N/A	0/1	0	0	0

Note: When using analog input(AINAx), ***[PLCR]*** should be output disable "0",***[PLIE]*** should be input disable "0", ***[PLPUP]*** should be pull-up disable"0" and ***[PLPDN]*** should be pull-down disable "0".

4.2.13. PORT M

Table 4.14 Port M Registers Setting

PORT	Reset status / Function	Input/output	PORT type	Control register						
				[PMDATA]	*[PMCR]*	*[PMFRn]*	*[PMOD]*	*[PMPUP]*	*[PMPDN]*	*[PMIE]*
PM0	After reset			0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0
	AINA07	Input	FTU5a	0/1	0	N/A	0/1	0	0	0
PM1	After reset			0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0
	AINA06	Input	FTU5a	0/1	0	N/A	0/1	0	0	0
PM2	After reset			0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0
	AINA05	Input	FTU5a	0/1	0	N/A	0/1	0	0	0

Note: When using analog input(AINAx), ***[PMCR]*** should be output disable "0",***[PMIE]*** should be input disable "0", ***[PMPUP]*** should be pull-up disable"0" and ***[PMPDN]*** should be pull-down disable "0".

4.2.14. PORT N

Table 4.15 Port N Registers Setting

PORT	Reset status / Function	Input/output	PORT type	Control register						
				[PNDATA]	*[PNCR]*	*[PNFRn]*	*[PNOD]*	*[PNPUP]*	*[PNPDN]*	*[PNIE]*
PN0	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	UT0TXDA	Output	FTU1a	0/1	1	***[PNFR1]***	0/1	0/1	0/1	0
	UT0RXD	Input	FTU1a	0/1	0	***[PNFR2]***	0/1	0/1	0/1	1
	NBDDATA2	Input/Output	FTU2c	0/1	1	***[PNFR3]***	0/1	0/1	0/1	1
	T32A05INA0	Input	FTU1a	0/1	0	***[PNFR4]***	0/1	0/1	0/1	1
	T32A05INC0	Input	FTU1a	0/1	0	***[PNFR5]***	0/1	0/1	0/1	1
	ENC0A	Input	FTU1a	0/1	0	***[PNFR6]***	0/1	0/1	0/1	1
	TRACEDATA2	Output	FTU1a	0/1	1	***[PNFR7]***	0/1	0/1	0/1	0
PN1	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT16a	Input	FTU4a	0/1	0	0	0/1	0/1	0/1	1
	UT0RXD	Input	FTU1a	0/1	0	***[PNFR1]***	0/1	0/1	0/1	1
	UT0TXDA	Output	FTU1a	0/1	1	***[PNFR2]***	0/1	0/1	0/1	0
	NBDDATA3	Input/Output	FTU2c	0/1	1	***[PNFR3]***	0/1	0/1	0/1	1
	T32A05OUTA	Output	FTU1a	0/1	1	***[PNFR4]***	0/1	0/1	0/1	0
	T32A05OUTC	Output	FTU1a	0/1	1	***[PNFR5]***	0/1	0/1	0/1	0
	ENC0B	Input	FTU1a	0/1	0	***[PNFR6]***	0/1	0/1	0/1	1
	TRACEDATA3	Output	FTU1a	0/1	1	***[PNFR7]***	0/1	0/1	0/1	0
PN2	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT16b	Input	FTU4a	0/1	0	0	0/1	0/1	0/1	1
	UT0CTS_N	Input	FTU1a	0/1	0	***[PNFR1]***	0/1	0/1	0/1	1
	T32A05INA1	Input	FTU1a	0/1	0	***[PNFR4]***	0/1	0/1	0/1	1
	T32A05INC1	Input	FTU1a	0/1	0	***[PNFR5]***	0/1	0/1	0/1	1
	ENC0Z	Input	FTU1a	0/1	0	***[PNFR6]***	0/1	0/1	0/1	1

4.2.15. PORT U

Table 4.16 Port U Registers Setting

PORT	Reset status / Function	Input/output	PORT type	Control register						
				[PUDATA]	*[PUCR]*	*[PUFRn]*	*[PUOD]*	*[PUPUP]*	*[PUPDN]*	*[PUIE]*
PU0	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT12	Input	FTU4a	0/1	0	0	0/1	0/1	0/1	1
	UT2TXDA	Output	FTU1a	0/1	1	***[PUFR1]***	0/1	0/1	0/1	0
	UT2RXD	Input	FTU1a	0/1	0	***[PUFR2]***	0/1	0/1	0/1	1
	I2C1SDA	Input/ Output	FTU1a	0/1	1	***[PUFR3]***	1	0/1	0/1	1
	T32A02INB1	Input	FTU1a	0/1	0	***[PUFR4]***	0/1	0/1	0/1	1
	UO2	Output	FTU2a	0/1	1	***[PUFR6]***	0/1	0/1	0/1	0
	EI2C1SDA	Input/ Output	FTU1a	0/1	1	***[PUFR7]***	1	0/1	0/1	1
PU1	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT07a	Input	FTU4a	0/1	0	0	0/1	0/1	0/1	1
	UT2RXD	Input	FTU1a	0/1	0	***[PUFR1]***	0/1	0/1	0/1	1
	UT2TXDA	Output	FTU1a	0/1	1	***[PUFR2]***	0/1	0/1	0/1	0
	I2C1SCL	Input/ Output	FTU1a	0/1	1	***[PUFR3]***	1	0/1	0/1	1
	T32A02INA0	Input	FTU1a	0/1	0	***[PUFR4]***	0/1	0/1	0/1	1
	T32A02INC0	Input	FTU1a	0/1	0	***[PUFR5]***	0/1	0/1	0/1	1
	XO2	Output	FTU2a	0/1	1	***[PUFR6]***	0/1	0/1	0/1	0
	EI2C1SCL	Input/ Output	FTU1a	0/1	1	***[PUFR7]***	1	0/1	0/1	1
PU2	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT07b	Input	FTU4a	0/1	0	0	0/1	0/1	0/1	1
	T32A02OUTA	Output	FTU1a	0/1	1	***[PUFR4]***	0/1	0/1	0/1	0
	T32A02OUTC	Output	FTU1a	0/1	1	***[PUFR5]***	0/1	0/1	0/1	0
	VO2	Output	FTU2a	0/1	1	***[PUFR6]***	0/1	0/1	0/1	0
PU3	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT08a	Input	FTU4a	0/1	0	0	0/1	0/1	0/1	1
	UT1RTS_N	Output	FTU1a	0/1	1	***[PUFR1]***	0/1	0/1	0/1	0
	T32A02INB0	Input	FTU1a	0/1	0	***[PUFR4]***	0/1	0/1	0/1	1
	ENC2A	Input	FTU1a	0/1	0	***[PUFR5]***	0/1	0/1	0/1	1
	YO2	Output	FTU2a	0/1	1	***[PUFR6]***	0/1	0/1	0/1	0
PU4	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT08b	Input	FTU4a	0/1	0	0	0/1	0/1	0/1	1
	UT1CTS_N	Input	FTU1a	0/1	0	***[PUFR1]***	0/1	0/1	0/1	1
	T32A02OUTB	Output	FTU1a	0/1	1	***[PUFR4]***	0/1	0/1	0/1	0
	T32A02INC1	Input	FTU1a	0/1	0	***[PUFR5]***	0/1	0/1	0/1	1
	WO2	Output	FTU2a	0/1	1	***[PUFR6]***	0/1	0/1	0/1	0

PORT	Reset status / Function	Input/output	PORT type	Control register						
				[PUDATA]	*[PUCR]*	*[PUFRn]*	*[PUOD]*	*[PUPUP]*	*[PUPDN]*	*[PUIE]*
PU5	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT13	Input	FTU4a	0/1	0	0	0/1	0/1	0/1	1
	UT1TXDA	Output	FTU1a	0/1	1	***[PUFR1]***	0/1	0/1	0/1	0
	UT1RXD	Input	FTU1a	0/1	0	***[PUFR2]***	0/1	0/1	0/1	1
	T32A02INA1	Input	FTU1a	0/1	0	***[PUFR4]***	0/1	0/1	0/1	1
	ENC2B	Input	FTU1a	0/1	0	***[PUFR5]***	0/1	0/1	0/1	1
	ZO2	Output	FTU2a	0/1	1	***[PUFR6]***	0/1	0/1	0/1	0
PU6	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT09	Input	FTU4a	0/1	0	0	0/1	0/1	0/1	1
	UT1RXD	Input	FTU1a	0/1	0	***[PUFR1]***	0/1	0/1	0/1	1
	UT1TXDA	Output	FTU1a	0/1	1	***[PUFR2]***	0/1	0/1	0/1	0
	ENC2Z	Input	FTU1a	0/1	0	***[PUFR5]***	0/1	0/1	0/1	1
	EMG2	Input	FTU1a	0/1	0	***[PUFR6]***	0/1	0/1	0/1	1
PU7	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	OVV2	Input	FTU1a	0/1	0	***[PUFR6]***	0/1	0/1	0/1	1
	PMD2DBG	Output	FTU1a	0/1	1	***[PUFR7]***	0/1	0/1	0/1	0

4.2.16. PORT V

Table 4.17 Port V Registers Setting

PORT	Reset status / Function	Input/output	PORT type	Control register						
				[PVDATA]	*[PVCR]*	*[PVFRn]*	*[PVOD]*	*[PVPUP]*	*[PVPDN]*	*[PVIE]*
PV0	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	TSPI1CSIN	Input	FTU1a	0/1	0	***[PVFR2]***	0/1	0/1	0/1	1
	T32A01OUTB	Output	FTU1a	0/1	1	***[PVFR4]***	0/1	0/1	0/1	0
PV1	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	UT0RTS_N	Output	FTU1a	0/1	1	***[PVFR1]***	0/1	0/1	0/1	0
	TSPI1RXD	Input	FTU1a	0/1	0	***[PVFR2]***	0/1	0/1	0/1	1

5. Block Diagrams of Ports

The port has eight types of circuits, FTU1a to FTU5a, FTU11a and FTU16a. Each circuit diagram is shown in the following page and after. The dot line block shows an equivalent circuit which is described in "Datasheet".

The "I/O Reset" shown in the circuit diagram is described the power on reset(POR) or the reset pin(RESET_N). Although, “I/O Reset” of debug pins(TMS/SWDIO.TDI,TDO/SWV,TCK/SWCLK,TRST_N) is the power on reset(POR) only.

5.1. Type FTU1a

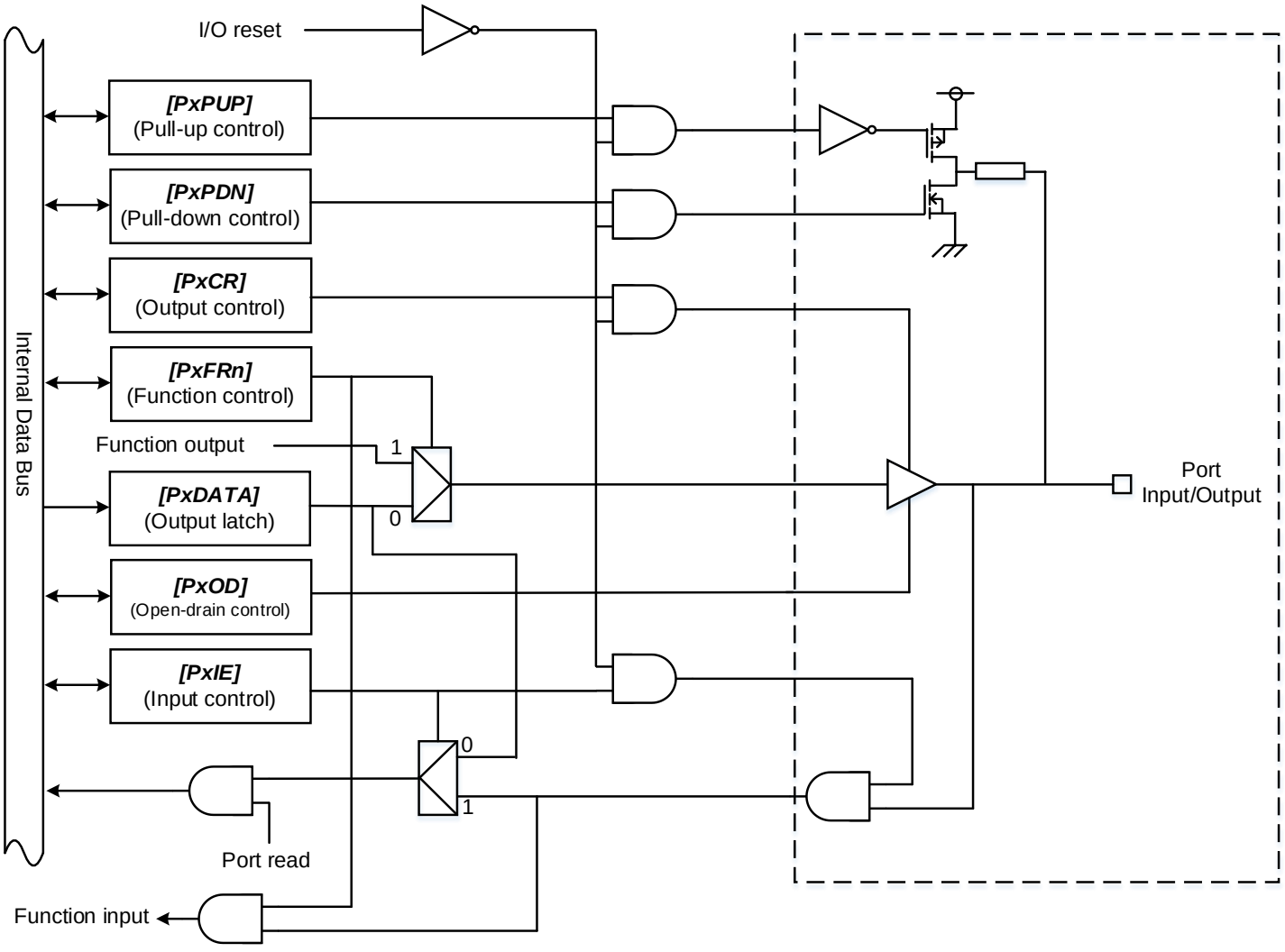

Figure 5.1 Port Type FTU1a

5.2. Type FTU2a

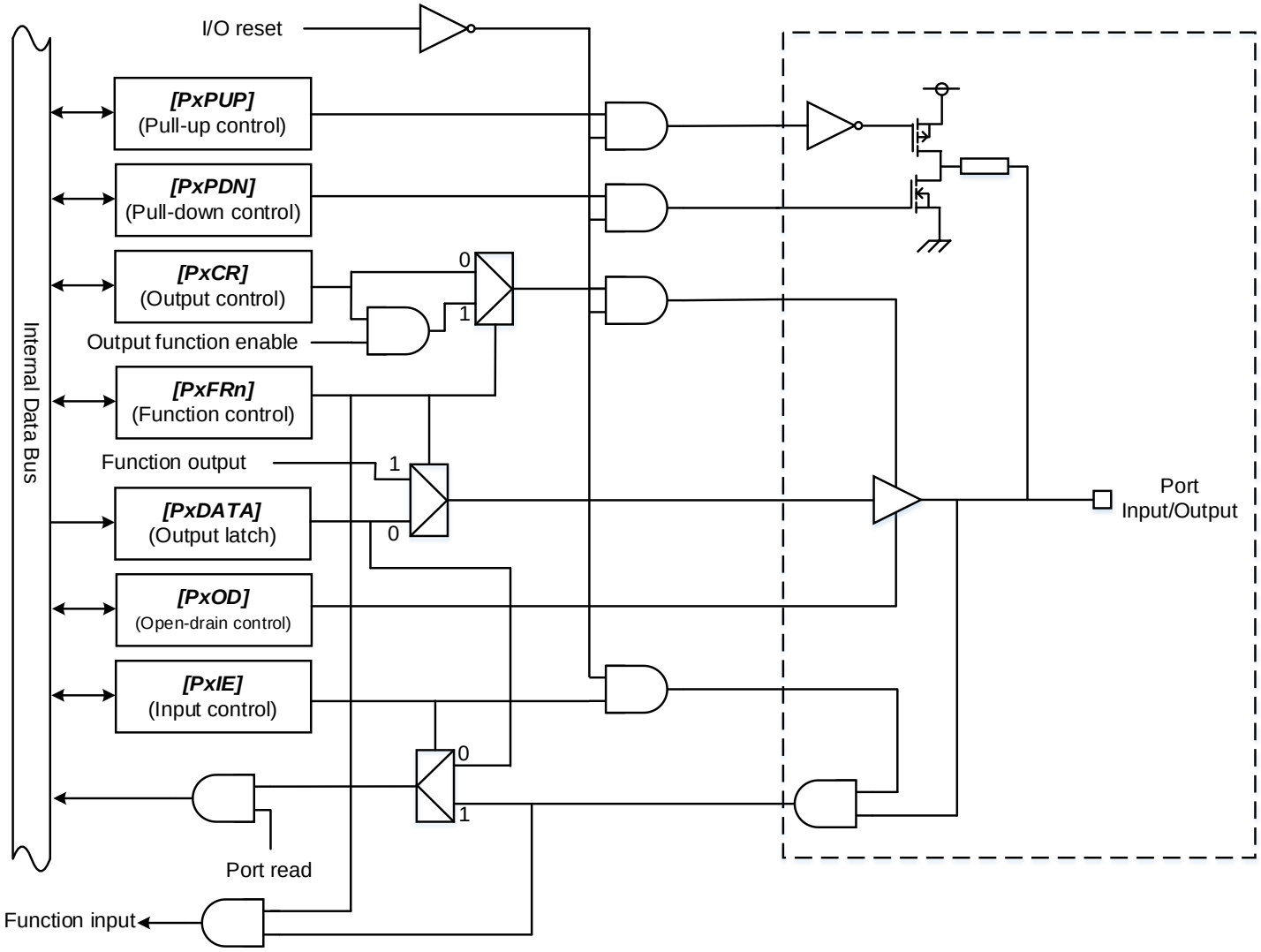

Figure 5.2 Port Type FTU2a

5.3. Type FTU2c

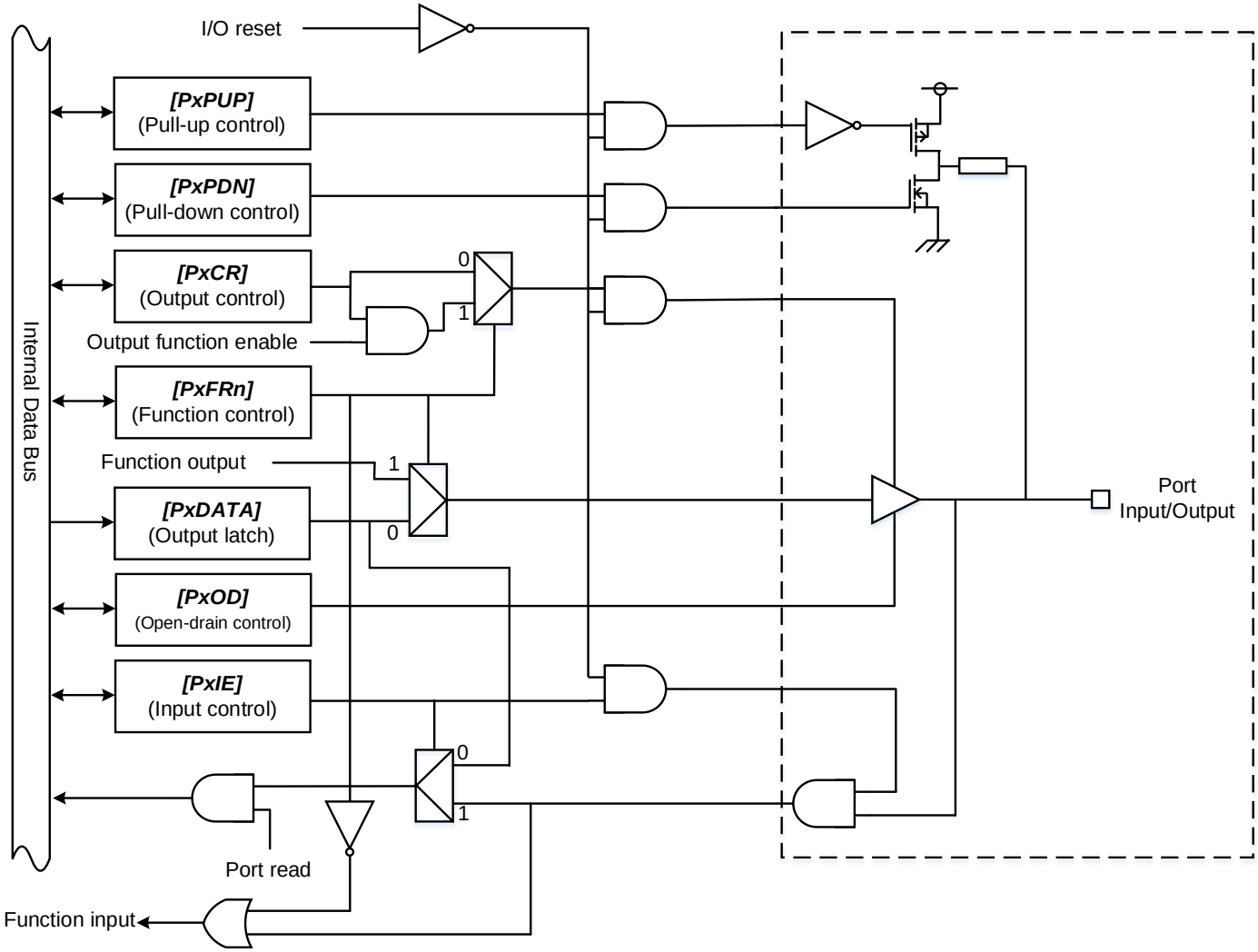

Figure 5.3 Port Type FTU2c

5.4. Type FTU3a

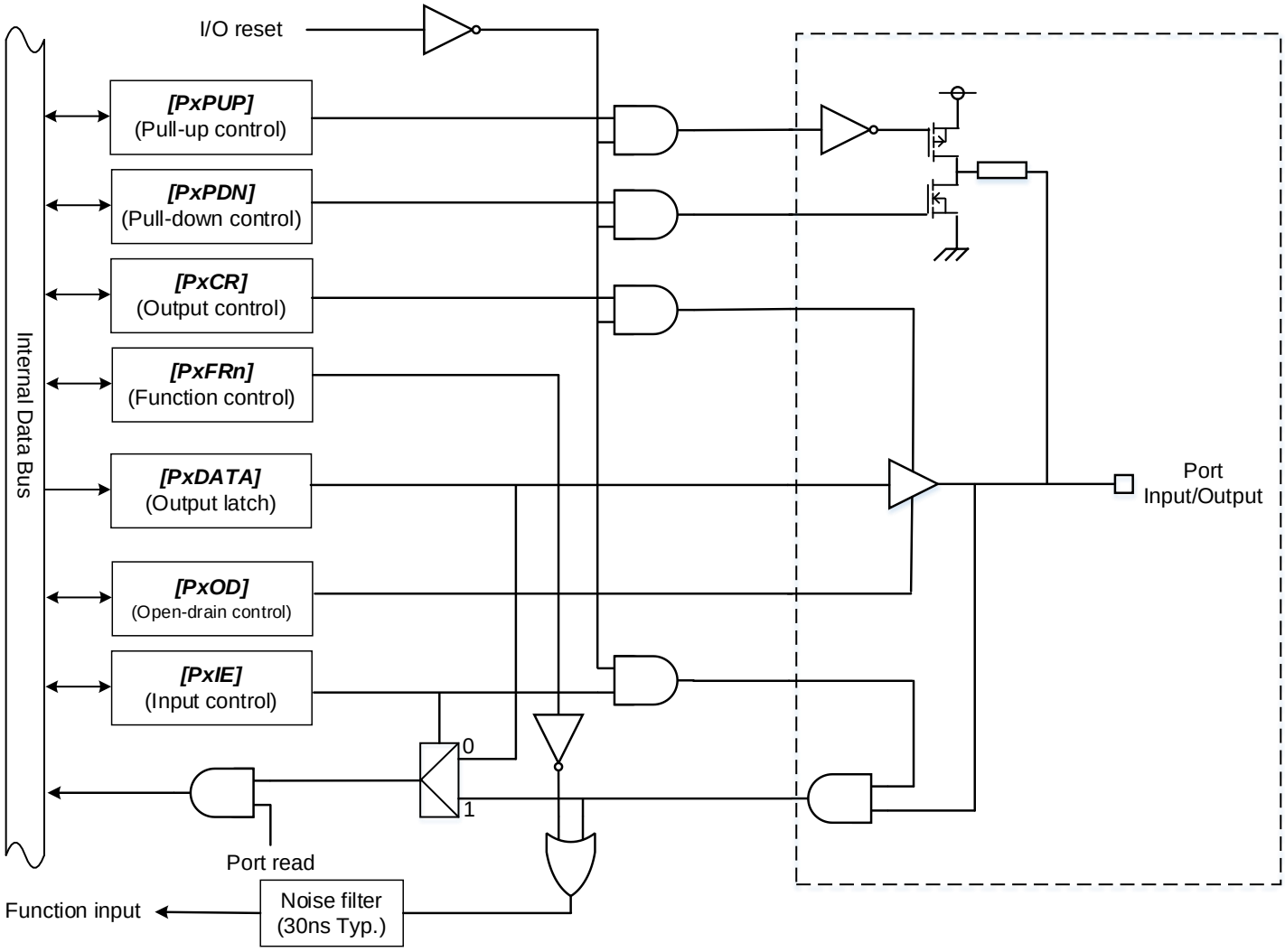

Figure 5.4 Port Type FTU3a

5.5. Type FTU4a

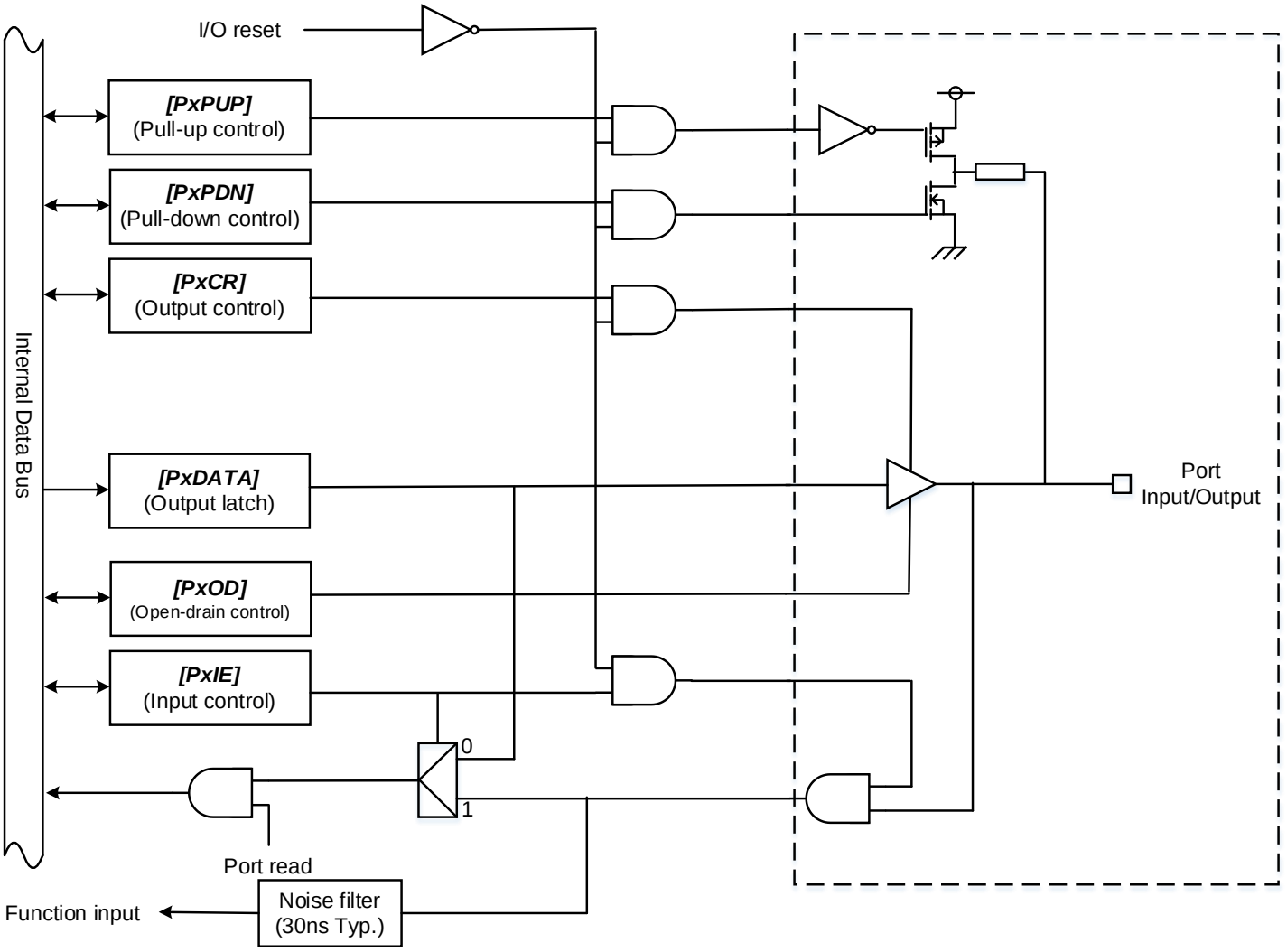

Figure 5.5 Port Type FTU4a

5.6. Type FTU5a

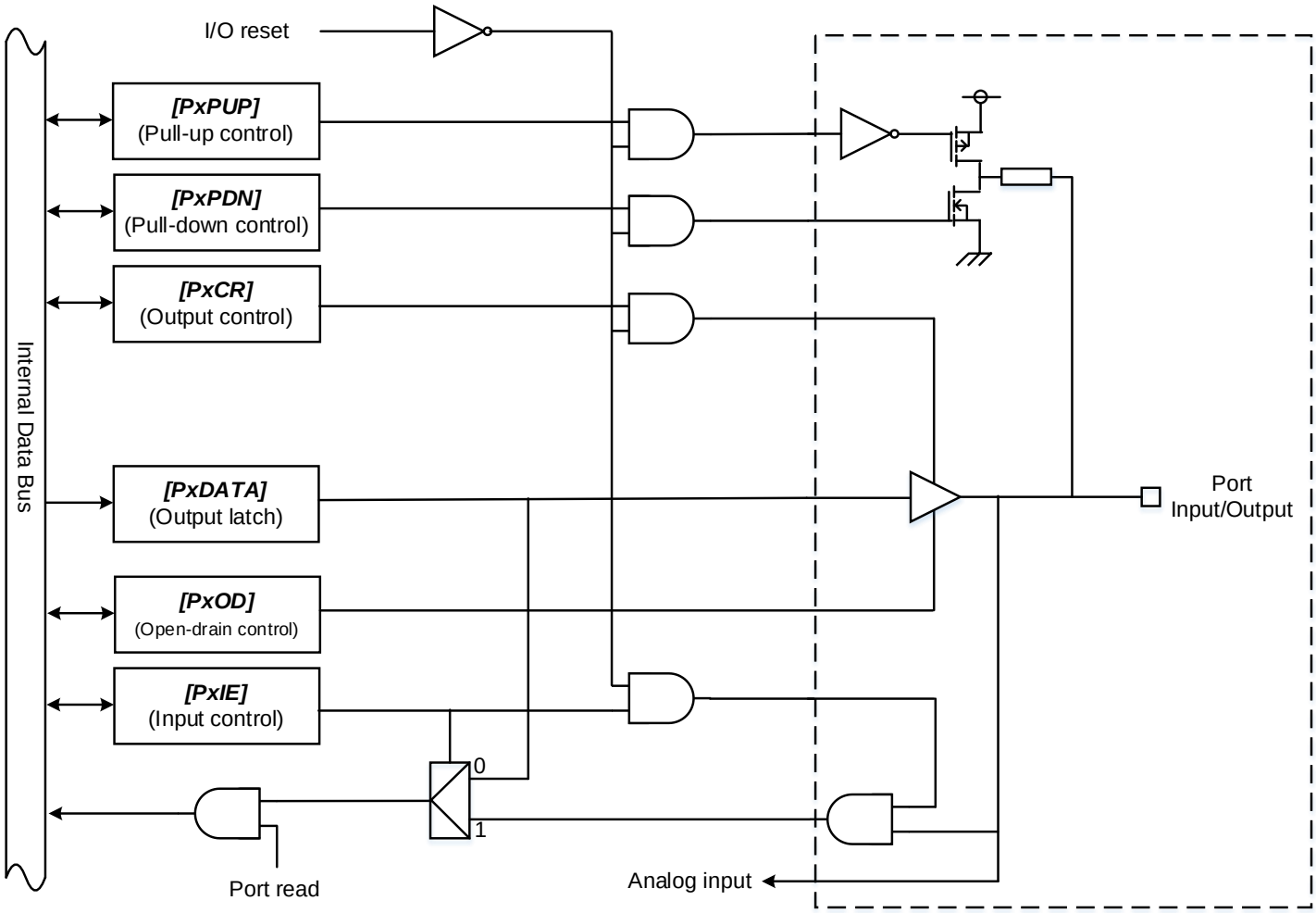

Figure 5.6 Port Type FTU5a

5.7. Type FTU11a

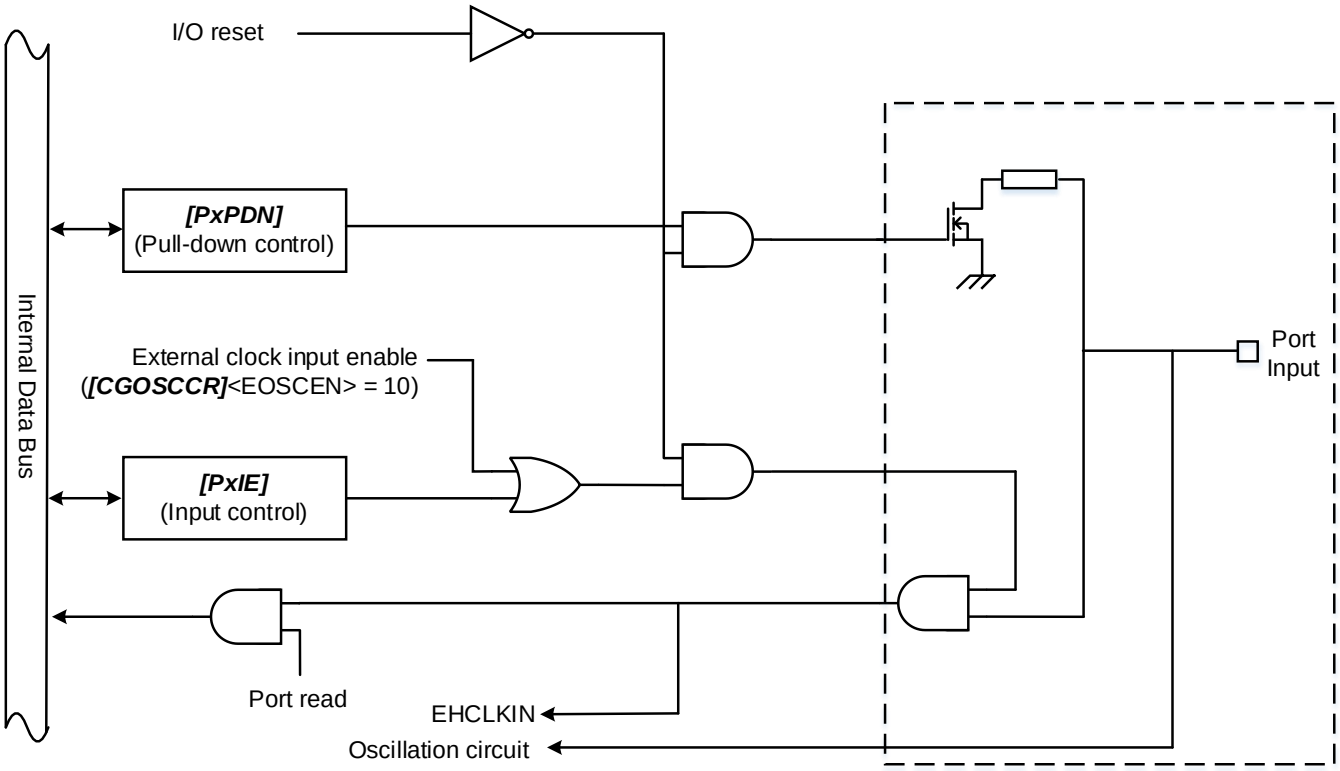

Figure 5.7 Port Type FTU11a

5.8. Type FTU16a

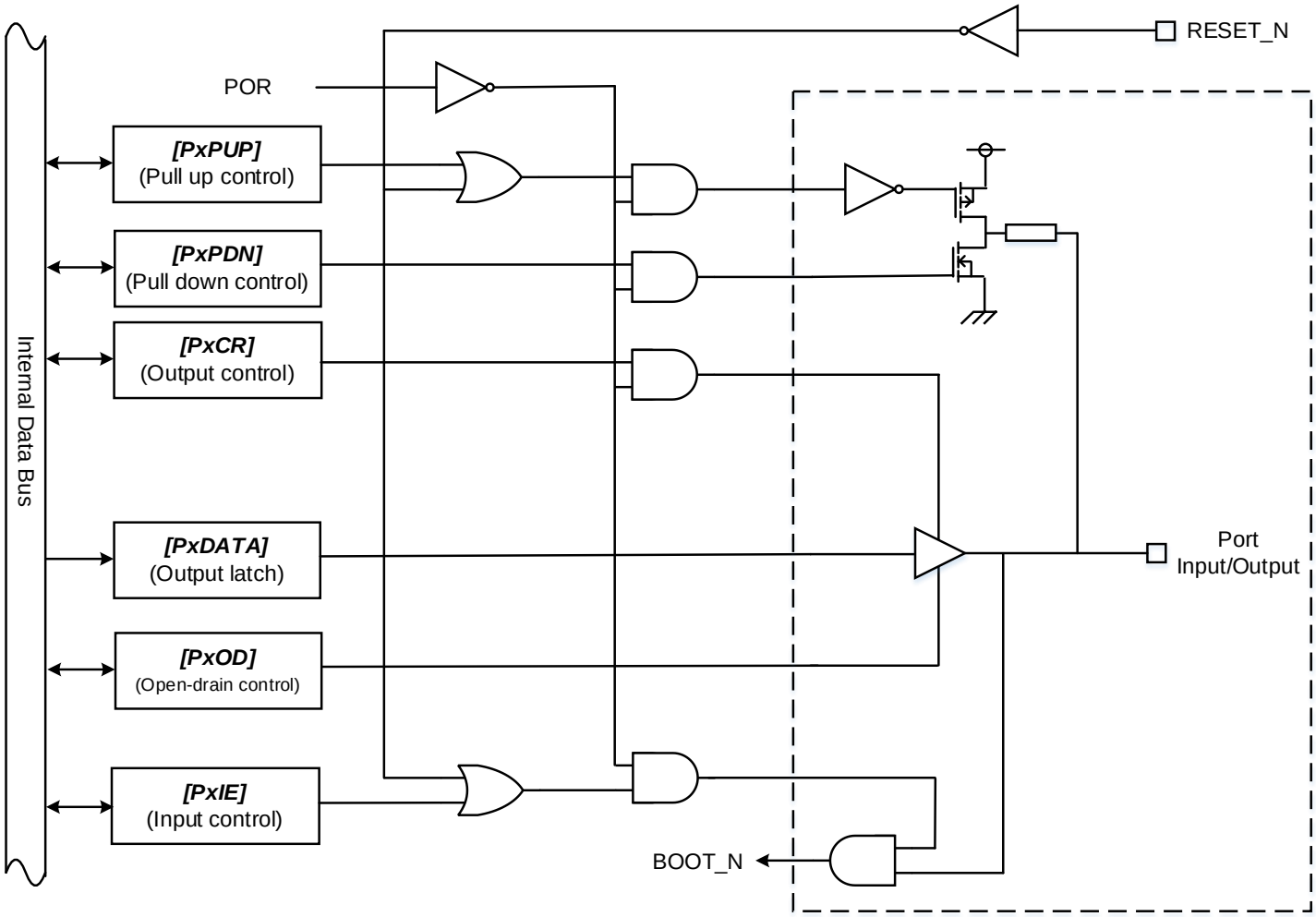

Figure 5.8 Port Type FTU16a

6. Precaution

6.1. Pin Status during Reset Period

During the reset period, the pin status is high impedance except for below pins. And, the pull-up/pull-down is invalid.

- The debug interface alternate pins (PF0 to PF4) are debugging pin status.
- PG2(BOOT_N) works as a BOOT function. It is enabled to be input and pulled-up during pin reset period. At the rising edge of the reset signal, if PG2 is "High", the device enters single chip mode and boots from the on chip flash memory. If PG2 is "Low", the device enters single BOOT mode and boots from the internal BOOT ROM program.

6.2. Unused Pin

We recommend that each unused pin should be connected to the power supply pins or GND pins via resistors.

Generally, if MCUs operate while the high-impedance pins left open, electrostatic damage or latch-up may occur in the internal LSI due to induced voltage influenced from external noise.

6.3. Important Points of Using Debug Interface Pins Used as General-purpose Ports

After releasing reset, if the debug interface pins are used as the general I/O ports by the user program, the debug tool cannot be connected

If the debug tool cannot be connected, it can recover debug connection to erase the flash memory using UART connection set as single BOOT mode from external. For details, please refer to the reference manual of "Flash memory".

7. Revision History

Table 7.1 Revision History

Revision	Date	Description
1.0	2020-11-30	New Release
1.1	2022-06-24	- Table 4.5 Port C registers setting Modified table (PC5)
1.2	2023-12-08	Changed Table 4.10 Changed Figure 5.7
1.3	2025-06-20	- 4.2.8. PORT G Changed table 4.9, changed note - 4.2.9. PORT H Changed table 4.10

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