32-Bit RISC Microcontroller

TXZ+ Family
TMPM4M Group(1)
Reference Manual
Exception
(EXCEPT-M4M(1))

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TOSHIBA ELECTRONIC DEVICES & STORAGE CORPORATION

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Related document

Document name
Oscillation Frequency Detector
Clock Selective Watchdog Timer
Voltage Detection Circuit
Clock Control and Operation Mode
Arm® Cortex®-M4 Processor Technical Reference Manual

Conventions

- Numeric formats follow the rules as shown below:
  Hexadecimal: 0xABC
  Decimal: 123 or 0d123 – Only when it needs to be explicitly shown that they are decimal numbers.
  Binary: 0b111 – It is possible to omit the "0b" when the number of bit can be distinctly understood from a sentence.
- "_N" is added to the end of signal names to indicate low active signals.
- It is called "assert" that a signal moves to its active level, "deassert" to its inactive level.
- When two or more signal names are referred, they are described like as [m: n].
  Example: S[3: 0] shows four signal names S3, S2, S1 and S0 together.
- The characters surrounded by *[ ]* defines the register.
  Example: *[ABCD]*
- "n" substitutes suffix number of two or more same kind of registers, fields, and bit names.
  Example: *[XYZ1], [XYZ2], [XYZ3]→ [XYZn]*
- "x" substitutes suffix number or character of units and channels in the Register List.
  In case of unit, "x" means A, B, and C ...
  Example: *[ADACR0], [ADBCR0], [ADCCR0]→ [ADxCR0]*
  In case of channel, "x" means 0, 1, and 2 ...
  Example: *[T32A0RUNA], [T32A1RUNA], [T32A2RUNA]→[T32AxRUNA]*
- The bit range of a register is written like as [m: n].
  Example: Bit[3: 0] expresses the range of bit 3 to 0.
- The configuration value of a register is expressed by either the hexadecimal number or the binary number.
  Example: *[ABCD]*<EFG> = 0x01 (hexadecimal), *[XYZn]*<VW> = 1 (binary)
- Word and Byte represent the following bit length.
  Byte: 8 bits
  Half word: 16 bits
  Word: 32 bits
  Double word: 64 bits
- Properties of each bit in a register are expressed as follows:
  R: Read only
  W: Write only
  R/W: Read and Write are possible
- Unless otherwise specified, register access supports only word access.
- The register defined as reserved must not be rewritten. Moreover, do not use the read value.
- The value read from the bit having default value of "-" is unknown.
- When a register containing both of writable bits and read-only bits is written, read-only bits should be written with their default value, In the cases that default is "-", follow the definition of each register.
- Reserved bits of the Write-only register should be written with their default value. In the cases that default is "-", follow the definition of each register.
- Do not use read-modified-write processing to the register of a definition which is different by writing and read out.

Terms and Abbreviations

Some of abbreviations used in this document are as follows:

ADC	Analog to Digital Converter
A-ENC32	Advanced Encoder Input Circuit(32-bit)
A-PMD	Advanced Programmable Motor Control Circuit
A-VE+	Advanced Vector Engine Plus
CAN	Controller Area Network
CG	Clock control and Operation mode
DMAC	Direct Memory Access Controller
EI2C	I^2C Interface Version A
IA	Interrupt control register A
IB	Interrupt control register B
IMCxx	Interrupt Mode Control xx
IMNFLGNMI	Interrupt Monitor Flag NMI
IMNFLGx	Interrupt Monitor Flag x
INTIF	Interrupt Interface Logic
ISR	Interrupt Service Routine
I2C	Inter-Integrated Circuit
LVD	Voltage Detection Circuit
NICxx	Non maskable Interrupt Control xx
OFD	Oscillation Frequency Detector
POR	Power On Reset Circuit
PORF	Power On Reset Circuit for FLASH and debug
RLMRSTFLGx	RLM Reset Flag x
SIWDT	Clock Selective Watchdog Timer
TSPI	Serial Peripheral Interface
T32A	32-bit Timer Event Counter
UART	Universal Asynchronous Receiver Transmitter

Exceptions have close relation to the CPU core. Refer to "Arm documentation set for the Arm Cortex-M4 processors" if needed.

1. Outlines

Exceptions require CPU to suspend the currently executing process, and to start another process.

There are two types of exceptions: those that are generated when some error condition occurs or when an instruction to generate an exception is executed; and those that are generated by hardware, such as an interrupt request signal from an external pin or peripheral function.

All exceptions are handled by the Nested Vectored Interrupt Controller (NVIC) in the CPU according to the respective priority levels. When an exception occurs, the CPU stores the current state to the stack and branches to the corresponding interrupt service routine (ISR). Upon completion of the ISR, the information stored to the stack is automatically restored.

1.1. Exception Types

The following types of exceptions exist in this product.

For detailed descriptions of each exception, refer to "Arm documentation set for the Arm Cortex-M4 processors".

- Reset
- Non-Maskable Interrupt(NMI)
- Hard Fault
- Memory Management
- Bus Fault
- Usage Fault
- SVCall (Supervisor Call)
- Debug Monitor
- PendSV
- SysTick
- External Interrupt

1.2. Exception Handling Flowchart

The following shows how an exception/interrupt is handled. In the following descriptions, exception handling by hardware and that by software are explained.

Each step is described later in this reference manual.

Process	Description	See
Detection by INTIF/CPU	The INTIF/CPU detects the exception request.	Section 1.2.1
⇩		
Handling by CPU	The CPU handles the exception request.	Section 1.2.2
⇩		
Branch to ISR	The CPU branches to the corresponding interrupt service routine (ISR).	Section 1.2.2
⇩		
Execution of ISR	Necessary processing is executed	Section 1.2.3
⇩		
Return from exception	The CPU branches to another ISR or returns to the previous program.	Section 1.2.4

1.2.1. Exception Request and Detection

(1) Exception Occurrence

Exception factors include instruction execution by the CPU, memory accesses, and interrupt requests from external interrupt pins or peripheral functions.

An exception by the instruction execution occurs when the CPU executes an instruction that causes an exception or when an error condition occurs during instruction execution.

An exception also occurs by an instruction fetch from the Execute Never region or an access violation to the Fault region.

The request of the exception by the external interrupt terminal or the peripheral function occurs by each functional factor. Regarding to interrupt which connected via INTIF, the setup of the interrupt control register is needed. For details, refer to the chapter, " 4. Interrupts "

(2) Exception Detection

If multiple exceptions occur simultaneously, the CPU takes the exception with the highest priority.

Table 1.1 shows the priority of exceptions. "Configurable" means that you can assign a priority level to that exception. Memory Management, Bus Fault and Usage Fault exceptions can be enabled or disabled. If a disabled exception occurs, it is handled as Hard Fault.

Table 1.1 Exception Types and Priority

Exception Type	Priority	Description	Offset
Reset	-3(highest)	Reset pin, POR , PORF, OFD, SIWDT, LVD, SYSRESETREQ, LOCKUP signal	0x00
Non-Maskable Interrupt	-2	SIWDT, LVD	0x08
Hard Fault	-1	Fault that cannot activate because a higher-priority fault is being handled or it is disabled	0x0C
Memory Management	Configurable	Exception from the Memory Protection Unit (MPU) Instruction fetch from the Execute Never (XN) region	0x10
Bus Fault	Configurable	Access violation to the Hard Fault region of the memory map	0x14
Usage Fault	Configurable	Undefined instruction execution or other faults related to instruction execution	0x18
Reserved	-		0x1C to 0x28
SVCall	Configurable	System service call with SVC instruction	0x2C
Debug Monitor	Configurable	Debug monitor when the CPU is not faulting	0x30
Reserved	-		0x34
PendSV	Configurable	Pending system service request	0x38
SysTick	Configurable	Notification from system timer	0x3C
External Interrupt	Configurable	External interrupt pin or peripheral function (Note)	0x40

Note: External interrupts have different factors and numbers in each product. For details, see "4.4. List of Interrupt Factors".

(3) Priority Setting

- Priority Level

The external interrupt priority is set to the Interrupt Priority Register and other exceptions are set to <PRI_n> bit in the System Handler Priority Register.
The configuration <PRI_n> can be changed, and the number of bits required for setting the priority varies from 3 bits to 8 bits depending on products. Thus, the range of priority values you can specify is different depending on products.
In the case of 8-bit configuration, the priority can be configured in the range from 0 to 255. The highest priority is "0". If multiple elements with the same priority exist, the smaller the number, the higher the priority becomes.

<PRI_n[7:0]> bit is defined as the upper 4-bit configuration with TMPM4M Group(1) products. The priority can be configured in the range from 0 to 15.

- Priority Grouping

The priority group can be split into groups. By setting the <PRIGROUP> of the Application Interrupt and Reset Control Register, <PRI_n> can be divided into the pre-emption priority and the sub priority.
A priority is compared with the pre-emption priority. If the priority is the same as the pre-emption priority, then it is compared with the sub priority. If the sub priority is the same as the priority, the smaller the exception number, the higher the priority.
Table 1.2 shows the priority group setting. The pre-emption priority and the sub priority in the table are the number in the case that <PRI_n> is defined as an 8-bit configuration.

Table 1.2 Priority grouping setting

<PRIGROUP[2:0]> setting	<PRI_n[7:0]>		Number of pre-emption priorities	Number of sub priorities
	Pre-emption field	Sub priority field		
000	[7:1]	[0]	128	2
001	[7:2]	[1:0]	64	4
010	[7:3]	[2:0]	32	8
011	[7:4]	[3:0]	16	16
100	[7:5]	[4:0]	8	32
101	[7:6]	[5:0]	4	64
110	[7]	[6:0]	2	128
111	-	[7:0]	1	256

Note: If the configuration of <PRI_n> is less than 8 bits, the lower bit is "0". For the example in the case of 4-bit configuration, the priority is set as <PRI_n[7:4]> and <PRI_n[3:0]> is "0000".

1.2.2. Exception Handling and Branch to Interrupt Service Routine (Pre-emption)

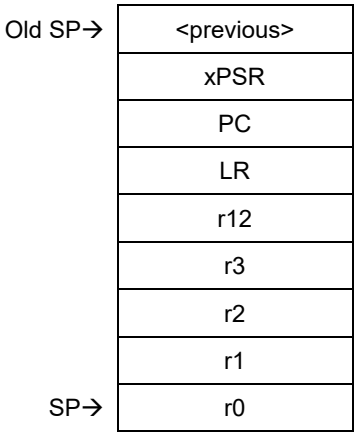
When an exception occurs, the CPU suspends the currently executing process and branches to the interrupt service routine. This is called "pre-emption".

(1) Stacking

When the CPU detects an exception, it pushes the contents of the following eight registers to the stack in the following order:

1. Program Counter (PC)
2. Program Status Register (xPSR)
3. r0 to r3
4. r12
5. Link Register (LR)

The SP is decremented by eight words by the completion of the stack push. The following shows the state of the stack after the register contents have been pushed.



(2) Fetching an ISR

The CPU performs the evacuation of the register. In addition, the CPU performs instruction fetch of the interrupt service routine at the same time.

Prepare a vector table containing the top addresses of ISRs for each exception. After reset, the vector table is located at address 0x00000000 in the Code area. By setting the Vector Table Offset Register, you can place the vector table at any address in the Code or SRAM space.
The vector table should also contain the initial value of the main stack.

(3) Late-arriving

If the CPU detects a higher priority exception before executing the ISR for a previous exception, the CPU handles the higher priority exception first. This is called "late-arriving".
A late-arriving exception causes the CPU to fetch a new vector address for branching to the corresponding ISR, but the CPU does not newly push the register contents to the stack.

(4) Vector Table

The vector table is configured as shown below.
You must always set the first four words (stack top address, reset ISR address, NMI ISR address, and Hard Fault ISR address). Set ISR addresses for other exceptions if necessary.

For other exceptions, you should prepare the ISR addresses if necessary.

Offset	Exception	Contents	Setting
0x00	Reset	Initial value of the main stack	Required
0x04	Reset	ISR address	Required
0x08	Non-Maskable Interrupt	ISR address	Required
0x0C	Hard Fault	ISR address	Required
0x10	Memory Management	ISR address	Optional
0x14	Bus Fault	ISR address	Optional
0x18	Usage Fault	ISR address	Optional
0x1C to 0x28	Reserved		
0x2C	SVCall	ISR address	Optional
0x30	Debug Monitor	ISR address	Optional
0x34	Reserved		
0x38	PendSV	ISR address	Optional
0x3C	SysTick	ISR address	Optional
0x40	External Interrupt	ISR address	Optional

1.2.3. Executing an ISR

An ISR performs necessary processing for the corresponding exception. ISRs must be prepared by the user.

An ISR may need to include code for clearing the interrupt request so that the same interrupt will not occur again upon return to normal program execution.
For details about interrupt handling, see "4. Interrupts".

If a higher priority exception occurs during ISR execution for the current exception, the CPU abandons the currently executing ISR and services the newly detected exception.

1.2.4. Exception Exit

(1) Execution after Returning from ISR

When returning from an ISR, the CPU takes one of the following actions:

- Tail-chaining

  If a pending exception exists and there are no stacked exceptions or the pending exception has higher priority than all stacked exceptions, the CPU returns to the ISR of the pending exception.
  In this case, the CPU skips the pop of eight registers and push of eight registers when exiting one ISR and entering another. This is called "tail-chaining".

- Returning to the last stacked ISR

  If there are no pending exceptions or if the highest priority stacked exception is of higher priority than the highest priority pending exception, the CPU returns to the last stacked ISR.

- Returning to the previous program

  If there are no pending or stacked exceptions, the CPU returns to the previous program.

(2) Exception Exit Sequence

When returning from an ISR, the CPU performs the following operations:

- Pop eight registers

  Pop eight registers (PC, xPSR, r0 to r3, r12, and LR) from the stack and adjust the SP.

- Load current active interrupt number

  Loads the current active interrupt number from the stacked xPSR. The CPU uses this to track which interrupt to return to.

- Select SP

  If returning to an exception (Handler Mode), SP is SP_main. If returning to Thread Mode, SP can be SP_main or SP_process.

2. Reset Exception

Reset exceptions are generated from the following factors.
Use the ***[RLMRSTFLGn]*** of the Reset Flag Register to identify the factor of a reset.

- Reset exception by external reset pin

  A reset exception occurs when an external reset pin changes from "Low" to "High".

- Reset exception by POR

  A reset exception occurs by POR. For details, refer to Reference Manual "Clock Control and Operation Mode".

- Reset exception by OFD

  The OFD has a reset generating feature. For details, refer to Reference Manual "Oscillation Frequency Detector".

- Reset exception by SIWDT

  The SIWDT has a reset generating feature. For details, refer to Reference Manual "Clock Selective Watchdog Timer".

- Reset exception by LVD

  The LVD has a reset generating feature. For details, refer to Reference Manual "Voltage Detector Circuit".

- Reset exception by PORF

  A reset exception occurs by PORF. For details, refer to Reference Manual "Clock Control and Operation Mode ".

- Reset exception by <SYSRESETREQ>

  A reset can be generated by setting the <SYSRESETREQ> bit in the NVIC's Application Interrupt and Reset Control Register.

- Reset exception by LOCKUP signal

  A reset can be generated by the LOCKUP signal which can be output from the CPU when the un-recoverable exception occurs. For details on the LOCKUP signal, please refer to "Arm Cortex-M4 Processor Technical Reference Manual".

3. SysTick

SysTick provides interrupt features using the CPU's system timer.

When you set a value in the SysTick Reload Value Register and enable the SysTick features in the SysTick Control and Status Register, the counter loads with the value set in the Reload Value Register and begins counting down. When the counter reaches "0", a SysTick exception occurs. You may be pending exceptions and use a flag to know when the timer reaches "0".

4. Interrupts

This chapter explains the route from which a factor and an interrupt request are transmitted, and a required setup.

4.1. Non-Maskable Interrupt (NMI)

Non-maskable interrupts are generated from the following factors.

- Non-maskable interrupt by SIWDT

  The SIWDT has a non-maskable interrupt generating feature. For details, refer to Reference Manual "Clock Selective Watchdog Timer".

- Non-maskable interrupt by LVD

  The LVD has a non-maskable interrupt generating feature. For details, refer to Reference Manual "Voltage Detector Circuit".

4.2. Maskable Interrupt

Please refer to interrupt control register A / interrupt control register B of the "4.4.List of Interrupt Factors " for the factor of the maskable interrupts.

4.3. Interrupt Request

The CPU is notified of interrupt requests by the interrupt signal from each interrupt factor. It sets priority on interrupts and handles an interrupt request with the highest priority.

4.3.1. Interrupt Route

The interrupt is available for the cancellation from a low power consumption mode, and a route varies according to a factor.

Figure 4.1 shows the interrupt transfer route diagram and Table 4.1 shows the explanation of each interrupt transfer route.

- The interrupt that is releasable from IDLE, STOP1 mode
  It has two Interrupt routes via INTIF that can release IDLE and STOP1 mode.

  (1) It is controlled by interrupt control register A in INTIF, and notified to CPU. (Route A, B, C)
  (2) It is controlled by interrupt control register B in INTIF, and notified to CPU. (Route D, E, F)

- The interrupt that is releasable from IDLE mode
  Although some factors of interrupt which can be released of IDLE mode are controlled by the interrupt control register B via INTIF (Route G), other factors are notified to CPU directly (Route H) not passing through INTIF.

When the interrupt factor that goes by way of INTIF regardless of low power consumption mode cancellation is used, setting of interrupt control register A or B is necessary.

Please refer to the chapter of "Release sources of a Low Power Consumption mode" of a reference manual "Clock Control and Operation Mode" for the details of a low-power-consumption mode release factor.

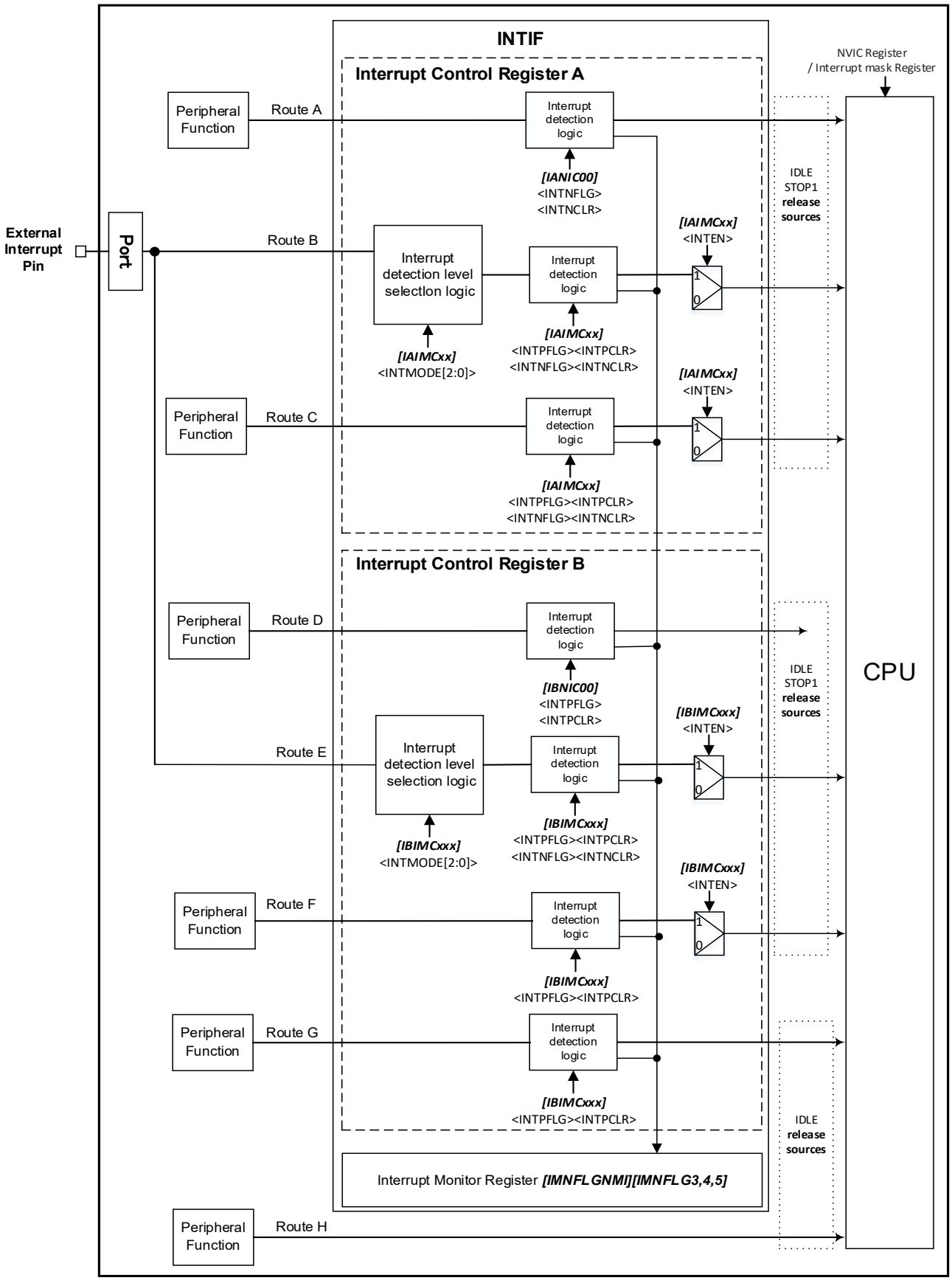


Figure 4.1 Interrupt transfer route Diagram

Table 4.1 Explanation of each interrupt transfer route

Route	Interrupt No.	Interrupt Request	Route Description
A	-	LVD interrupt	This route is NMI interrupt. It is a route input into CPU via INTIF. An interrupt release setup is carried out by the interrupt control register A (***[IANIC00]***).
B	-	-	The interrupt request of a port is a route input into CPU via INTIF. Permission/prohibition of selection of an Interrupt detection level, interrupt release, and an interrupt request are set up by the interrupt control register A (***[IAIMCxx]***) for every factor.
C	-	-	It is a route input into CPU via INTIF. Permission/prohibition of interrupt release and an interrupt request are set up by the interrupt control register A (***[IAIMCxx]***) for every factor.
D	-	WDT interrupt	It is non-maskable interrupt. It is a route input into CPU via INTIF. An interrupt release setup is carried out by the interrupt control register B (***[IBNIC00]***).
E	0 to 18, 21	External interrupts (00 to 18, 21)	The interrupt request of a port is a route input into CPU via INTIF. Permission/prohibition of selection of an Interrupt detection level, interrupt release, and an interrupt request are set up by the interrupt control register B (***[IBIMCxxx]***) for every factor.
F	-	-	It is a route input into CPU via INTIF. Permission/prohibition of interrupt are set up by the interrupt control register B (***[IBIMCxxx]***) for every factor.
G	121, 122	DMAC transfer completion interrupt (ch0 to 31), DMAC transfer error interrupt (Note)	It is a route input into CPU via INTIF. An interrupt release setup is carried out by the interrupt control register B (***[IBIMCxxx]***) for every factor.
H	22 to 120, 123, 124	Other interrupts	It is a route as which an interrupt request is directly input into CPU not passing through INTIF.

Note: DMAC transfer completion interrupt is an interrupt into which interrupts of two or more channels are combined. Please refer to "4.4.1. Joint interruption" for details.

4.3.2. Interrupt Request Generation

An interrupt request is generated from an external interrupt pin or peripheral function which are assigned as interrupt request factors, or by setting the relevant bit of NVIC's Interrupt Set-Pending Register for interrupt request factor.

- Interrupt from external interrupt pin
  Set the port control register so that the external pin can perform as an interrupt function pin.
- Interrupt from peripheral function
  Set the peripheral function to make it possible to output interrupt requests.
  See the chapter of each peripheral function for details.
- By setting Interrupt Set-Pending Register (forced pending)
  An interrupt request can be forced to be generated by setting the relevant bit of the Interrupt Set-Pending Register of NVIC.

CPU will recognize the "High" level of the interrupt request as an interrupt.

4.3.3. Monitor of the Interrupt Request

INTIF has the interrupt monitor flags. It can know that the interrupt request has occurred by monitoring the flag. If one request factor is representing several interrupt requests, Interrupt Monitor Register can be used to identify the actual interrupt request factor.

For detail, please refer to "4.4. List of Interrupt Factors".

4.3.4. Transmission of Interrupt Request

An interrupt request which is not passing through the Interrupt Control Register will be directly input to the CPU. The interrupts connected to the CPU through INTIF, which are used as interrupt request factors for releasing the low power consumption mode, will need a proper setting of the Interrupt Control Register in INTIF. A "High" level interrupt signal will be sent to the CPU, when the interrupt is used to release the low power consumption mode.

Please setup an interrupt detection level and interrupt enable/disable by INTIF.

By the way, please be cautious about external interrupt pin as in the next section.

4.3.5. Precautions When Using External Interrupt Pins

When using External interrupt, please care about the following points so that an unexpected interrupt does not occur.

If input is disabled (***[PxIE]***<PxmIE>=0), inputs from external interrupt pins are "Low". When the <INTMODE> bit of Interrupt Control Register A (***[IAIMCxx]***) is "Low", input signals from the external interrupt pins are sent to the CPU as is. Since the CPU recognizes "Low" input as an interrupt, interrupts occur if corresponding interrupts are enabled by the CPU.

The interrupt pins should be "High" and the inputs should be enabled. Then the interrupts should be enabled by the CPU.

4.4. List of Interrupt Factors

Table 4.2 shows the list of interrupt factors of non-maskable interrupts. The setting for clearing the NMI factors can be done by Interrupt Control Registers A and B

Table 4.2 List of Interrupt Factors (Non-Maskable Interrupt)

Interrupt Factor	Interrupt Request	Interrupt Control Register	Interrupt Monitor Register
INTLVD	LVD interrupt	***[IANIC00]***	***[IMNFLGNMI]*** <INT000FLG>
INTWDT0	WDT interrupt	***[IBNIC00]***	***[IMNFLGNMI]*** <INT016FLG>

There are no Interrupt factors of the Interrupt Control Register A in TMPM4M Group(1) products.

All Maskable Interrupt factors are in the Interrupt Control Register B.

Some interrupts can be the factors for releasing the low power consumption mode. The Interrupt Control Register B will perform several setting for detecting the release of the low power consumption mode, and interrupt detection enable/disable.

Table 4.3 List of Interrupt Factors (Interrupt Control Register B)(1/6)

Interrupt No.	Interrupt Factor	Interrupt Request	Interrupt Control Register	Interrupt Monitor Register
0	INT00	External interrupt 00	***[IBIMC033]***	***[IMNFLG4]*** <INT129FLG>
1	INT01	External interrupt 01a	***[IBIMC034]***	***[IMNFLG4]*** <INT130FLG>
		External interrupt 01b	***[IBIMC035]***	***[IMNFLG4]*** <INT131FLG>
2	INT02	External interrupt 02a	***[IBIMC036]***	***[IMNFLG4]*** <INT132FLG>
		External interrupt 02b	***[IBIMC037]***	***[IMNFLG4]*** <INT133FLG>
3	INT03	External interrupt 03a	***[IBIMC038]***	***[IMNFLG4]*** <INT134FLG>
		External interrupt 03b	***[IBIMC039]***	***[IMNFLG4]*** <INT135FLG>
4	INT04	External interrupt 04a	***[IBIMC040]***	***[IMNFLG4]*** <INT136FLG>
		External interrupt 04b	***[IBIMC041]***	***[IMNFLG4]*** <INT137FLG>
5	INT05	External interrupt 05a	***[IBIMC042]***	***[IMNFLG4]*** <INT138FLG>
		External interrupt 05b	***[IBIMC043]***	***[IMNFLG4]*** <INT139FLG>
6	INT06	External interrupt 06a	***[IBIMC044]***	***[IMNFLG4]*** <INT140FLG>
		External interrupt 06b	***[IBIMC045]***	***[IMNFLG4]*** <INT141FLG>
7	INT07	External interrupt 07a	***[IBIMC046]***	***[IMNFLG4]*** <INT142FLG>
		External interrupt 07b	***[IBIMC047]***	***[IMNFLG4]*** <INT143FLG>
8	INT08	External interrupt 08a	***[IBIMC048]***	***[IMNFLG4]*** <INT144FLG>
		External interrupt 08b	***[IBIMC049]***	***[IMNFLG4]*** <INT145FLG>

Table 4.4 List of Interrupt Factors (Interrupt Control Register B)(2/6)

Interrupt No.	Interrupt Factor	Interrupt Request	Interrupt Control Register	Interrupt Monitor Register
9	INT09	External interrupt 09	***[IBIMC050]***	***[IMNFLG4]*** <INT146FLG>
10	INT10	External interrupt 10	***[IBIMC051]***	***[IMNFLG4]*** <INT147FLG>
11	INT11	External interrupt 11a	***[IBIMC052]***	***[IMNFLG4]*** <INT148FLG>
		External interrupt 11b	***[IBIMC053]***	***[IMNFLG4]*** <INT149FLG>
12	INT12	External interrupt 12	***[IBIMC054]***	***[IMNFLG4]*** <INT150FLG>
13	INT13	External interrupt 13	***[IBIMC055]***	***[IMNFLG4]*** <INT151FLG>
14	INT14	External interrupt 14a	***[IBIMC056]***	***[IMNFLG4]*** <INT152FLG>
		External interrupt 14b	***[IBIMC057]***	***[IMNFLG4]*** <INT153FLG>
15	INT15	External interrupt 15	***[IBIMC058]***	***[IMNFLG4]*** <INT154FLG>
16	INT16	External interrupt 16a	***[IBIMC059]***	***[IMNFLG4]*** <INT155FLG>
		External interrupt 16b	***[IBIMC060]***	***[IMNFLG4]*** <INT156FLG>
17	INT17	External interrupt 17a	***[IBIMC061]***	***[IMNFLG4]*** <INT157FLG>
		External interrupt 17b	***[IBIMC062]***	***[IMNFLG4]*** <INT158FLG>
18	INT18	External interrupt 18a	***[IBIMC063]***	***[IMNFLG4]*** <INT159FLG>
		External interrupt 18b	***[IBIMC064]***	***[IMNFLG5]*** <INT160FLG>
19	Reserved			
20	Reserved			
21	INT21	External interrupt 21	***[IBIMC069]***	***[IMNFLG5]*** <INT165FLG>
22	INTVCN0	A-VE+ ch0 VE interrupt		
23	INTVCT0	A-VE+ ch0 VE task end interrupt		
24	INTEMG0	A-PMD ch0 EMG Interrupt		
25	INTEMG1	A-PMD ch1 EMG Interrupt		
26	INTEMG2	A-PMD ch2 EMG Interrupt		
27	INTOVV0	A-PMD ch0 OVV Interrupt		
28	INTOVV1	A-PMD ch1 OVV Interrupt		
29	INTOVV2	A-PMD ch2 OVV Interrupt		
30	INTPWM0	A-PMD ch0 PWM Interrupt		
31	INTPWM1	A-PMD ch1 PWM Interrupt		
32	INTPWM2	A-PMD ch2 PWM Interrupt		

Table 4.5 List of Interrupt Factors (Interrupt Control Register B)(3/6)

Interrupt No.	Interrupt Factor	Interrupt Request	Interrupt Control Register	Interrupt Monitor Register
33	INTENC00	A-ENC32 ch0 Encoder input interrupt 0		
34	INTENC01	A-ENC32 ch0 Encoder input interrupt 1		
35	INTENC10	A-ENC32 ch1 Encoder input interrupt 0		
36	INTENC11	A-ENC32 ch1 Encoder input interrupt 1		
37	INTENC20	A-ENC32 ch2 Encoder input interrupt 0		
38	INTENC21	A-ENC32 ch2 Encoder input interrupt 1		
39	INTADAPDA	ADC unit A PMD trigger program conversion complete A		
40	INTADAPDB	ADC unit A PMD trigger program conversion complete B		
41	INTADACP0	ADC unit A Monitor function 0 interrupt		
42	INTADACP1	ADC unit A Monitor function 1 interrupt		
43	INTADATRG	ADC unit A general trigger program conversion complete		
44	INTADASGL	ADC unit A single program conversion completion		
45	INTADACNT	ADC unit A continuous program conversion complete		
46	INTADBPDA	ADC unit B PMD trigger program conversion complete A		
47	INTADBPDB	ADC unit B PMD trigger program conversion complete B		
48	INTADBCP0	ADC unit B Monitor function 0 interrupt		
49	INTADBCP1	ADC unit B Monitor function 1 interrupt		
50	INTADBTRG	ADC unit B general trigger program conversion complete		
51	INTADBSGL	ADC unit B single program conversion completion		
52	INTADBCNT	ADC unit B continuous program conversion complete		
53	INTADCPDA	ADC unit C PMD trigger program conversion complete A		
54	INTADCPDB	ADC unit C PMD trigger program conversion complete B		
55	INTADCCP0	ADC unit C Monitor function 0 interrupt		
56	INTADCCP1	ADC unit C Monitor function 1 interrupt		
57	INTADCTRG	ADC unit C general trigger program conversion complete		
58	INTADCSGL	ADC unit C single program conversion completion		
59	INTADCCNT	ADC unit C continuous program conversion complete		

Table 4.6 List of Interrupt Factors (Interrupt Control Register B)(4/6)

Interrupt No.	Interrupt Factor	Interrupt Request	Interrupt Control Register	Interrupt Monitor Register
60	INTSC0RX (Note)	TSPI ch0 reception interrupt / UART ch0 reception interrupt		
61	INTSC0TX (Note)	TSPI ch0 transmit interrupt / UART ch0 transmit interrupt		
62	INTSC0ERR (Note)	TSPI ch0 error interrupt / UART ch0 error interrupt		
63	INTSC1RX (Note)	TSPI ch1 reception interrupt / UART ch1 reception interrupt		
64	INTSC1TX (Note)	TSPI ch1 transmit interrupt / UART ch1 transmit interrupt		
65	INTSC1ERR (Note)	TSPI ch1 error interrupt / UART ch1 error interrupt		
66	INTSC2RX (INTUART2RX)	UART ch2 reception interrupt		
67	INTSC2TX (INTUART2TX)	UART ch2 transmit interrupt		
68	INTSC2ERR (INTUART2ERR)	UART ch2 error interrupt		
69	INTSC3RX (INTUART3RX)	UART ch3 reception interrupt		
70	INTSC3TX (INTUART3TX)	UART ch3 transmit interrupt		
71	INTSC3ERR (INTUART3ERR)	UART ch3 error interrupt		
72	INTI2C0NST (Note)	I2C ch0 interrupt / EI2C ch0 status interrupt		
73	INTI2C0ATX (Note)	I2C ch0 arbitration lost detection interrupt / EI2C ch0 transmit buffer empty interrupt		
74	INTI2C0BRX (Note)	I2C ch0 bus free detection interrupt / EI2C ch0 receive buffer full interrupt		
75	INTI2C0NA	I2C ch0 NACK detection interrupt		
76	INTI2C1NST (Note)	I2C ch1 interrupt / EI2C ch1 status interrupt		
77	INTI2C1ATX (Note)	I2C ch1 arbitration lost detection interrupt / EI2C ch1 transmit buffer empty interrupt		
78	INTI2C1BRX (Note)	I2C ch1 bus free detection interrupt / EI2C ch1 receive buffer full interrupt		
79	INTI2C1NA	I2C ch1 NACK detection interrupt		
80	INTCANAGLB	CAN unit A global interrupt		
81	INTCANARXD	CAN unit A reception interrupt		
82	INTCANATXD	CAN unit A transmit interrupt		

Note: Please refer to "4.4.1. Joint interruption".

Table 4.7 List of Interrupt Factors (Interrupt Control Register B)(5/6)

Interrupt No.	Interrupt Factor	Interrupt Request	Interrupt Control Register	Interrupt Monitor Register
83	INTT32A00AC	T32A ch0 timer A/C match, overflow, and underflow		
84	INTT32A00ACCAP0	T32A ch0 timer A/C capture 0		
85	INTT32A00ACCAP1	T32A ch0 timer A/C capture 1		
86	INTT32A00B	T32A ch0 timer B match, overflow, and underflow		
87	INTT32A00BCAP0	T32A ch0 timer B capture 0		
88	INTT32A00BCAP1	T32A ch0 timer B capture 1		
89	INTT32A01AC	T32A ch1 timer A/C match, Overflow, and underflow		
90	INTT32A01ACCAP0	T32A ch1 timer A/C capture 0		
91	INTT32A01ACCAP1	T32A ch1 timer A/C capture 1		
92	INTT32A01B	T32A ch1 timer B match, overflow, and underflow		
93	INTT32A01BCAP0	T32A ch1 timer B capture 0		
94	INTT32A01BCAP0	T32A ch1 timer B capture 1		
95	INTT32A02AC	T32A ch2 timer A/C match, overflow, and underflow		
96	INTT32A02ACCAP0	T32A ch2 timer A/C capture 0		
97	INTT32A02ACCAP1	T32A ch2 timer A/C capture 1		
98	INTT32A02B	T32A ch2 timer B match, overflow, and underflow		
99	INTT32A02BCAP0	T32A ch2 timer B capture 0		
100	INTT32A02BCAP1	T32A ch2 timer B capture 1		
101	INTT32A03AC	T32A ch3 timer A/C match, overflow, and underflow		
102	INTT32A03ACCAP0	T32A ch3 timer A/C capture 0		
103	INTT32A03ACCAP1	T32A ch3 timer A/C capture 1		
104	INTT32A03B	T32A ch3 timer B match, overflow, and underflow		
105	INTT32A03BCAP0	T32A ch3 timer B capture 0		
106	INTT32A03BCAP1	T32A ch3 timer B capture 1		
107	INTT32A04AC	T32A ch4 timer A/C match, overflow, and underflow		
108	INTT32A04ACCAP0	T32A ch4 timer A/C capture 0		
109	INTT32A04ACCAP1	T32A ch4 timer A/C capture 1		
110	INTT32A04B	T32A ch4 timer B match, overflow, and underflow		
111	INTT32A04BCAP0	T32A ch4 timer B capture 0		
112	INTT32A04BCAP1	T32A ch4 timer B capture 1		

Table 4.8 List of Interrupt Factors (Interrupt Control Register B)(6/6)

Interrupt No.	Interrupt Factor	Interrupt Request	Interrupt Control Register	Interrupt Monitor Register
113	INTT32A05AC	T32A ch5 timer A/C match, overflow, and underflow		
114	INTT32A05ACCAP0	T32A ch5 timer A/C capture 0		
115	INTT32A05ACCAP1	T32A ch5 timer A/C capture 1		
116	INTT32A05B	T32A ch5 timer B match, overflow, and underflow		
117	INTT32A05BCAP0	T32A ch5 timer B capture 0		
118	INTT32A05BCAP1	T32A ch5 timer B capture 1		
119	INTPARI0	RAM Parity interrupt 0		
120	INTPARI1	RAM Parity interrupt 1		
121	INTDMAATC	DMAC transfer completion interrupt (ch0 to 31)	***[IBIMC000]*** to ***[IBIMC031]*** (Note1)	***[IMNFLG3]*** <INT096FLG> to <INT127FLG> (Note1)
122	INTDMAAERR	DMAC transfer error interrupt	***[IBIMC032]***	***[IMNFLG4]*** <INT128FLG>
123	INTFLCRDY	Code FLASH Ready interrupt		
124	INTFLDRDY	Data FLASH Ready interrupt		

Note1: Please refer to "4.4.1. Joint interruption".

Note2: The count interrupt (INTT32AxEVRYC) of 32-bit timer event counter (T32A) is not supported in this product.

4.4.1. Joint interruption

Details of interrupts that are coupled in TMPM4M Group(1) are as follows.

Table 4.9 Joint interruption list (1/2)

Interrupt No.	Interrupt Factor	Interrupt Request	Interrupt Control Register	Interrupt Monitor Register
1	INT01	External interrupt 01a	***[IBIMC034]***	***[IMNFLG4]***<INT130FLG>
		External interrupt 01b	***[IBIMC035]***	***[IMNFLG4]***<INT131FLG>
2	INT02	External interrupt 02a	***[IBIMC036]***	***[IMNFLG4]***<INT132FLG>
		External interrupt 02b	***[IBIMC037]***	***[IMNFLG4]***<INT133FLG>
3	INT03	External interrupt 03a	***[IBIMC038]***	***[IMNFLG4]***<INT134FLG>
		External interrupt 03b	***[IBIMC039]***	***[IMNFLG4]***<INT135FLG>
4	INT04	External interrupt 04a	***[IBIMC040]***	***[IMNFLG4]***<INT136FLG>
		External interrupt 04b	***[IBIMC041]***	***[IMNFLG4]***<INT137FLG>
5	INT05	External interrupt 05a	***[IBIMC042]***	***[IMNFLG4]***<INT138FLG>
		External interrupt 05b	***[IBIMC043]***	***[IMNFLG4]***<INT139FLG>
6	INT06	External interrupt 06a	***[IBIMC044]***	***[IMNFLG4]***<INT140FLG>
		External interrupt 06b	***[IBIMC045]***	***[IMNFLG4]***<INT141FLG>
7	INT07	External interrupt 07a	***[IBIMC046]***	***[IMNFLG4]***<INT142FLG>
		External interrupt 07b	***[IBIMC047]***	***[IMNFLG4]***<INT143FLG>
8	INT08	External interrupt 08a	***[IBIMC048]***	***[IMNFLG4]***<INT144FLG>
		External interrupt 08b	***[IBIMC049]***	***[IMNFLG4]***<INT145FLG>
11	INT11	External interrupt 11a	***[IBIMC052]***	***[IMNFLG4]***<INT148FLG>
		External interrupt 11b	***[IBIMC053]***	***[IMNFLG4]***<INT149FLG>
14	INT14	External interrupt 14a	***[IBIMC056]***	***[IMNFLG4]***<INT152FLG>
		External interrupt 14b	***[IBIMC057]***	***[IMNFLG4]***<INT153FLG>
16	INT16	External interrupt 16a	***[IBIMC059]***	***[IMNFLG4]***<INT155FLG>
		External interrupt 16b	***[IBIMC060]***	***[IMNFLG4]***<INT156FLG>
17	INT17	External interrupt 17a	***[IBIMC061]***	***[IMNFLG4]***<INT157FLG>
		External interrupt 17b	***[IBIMC062]***	***[IMNFLG4]***<INT158FLG>
18	INT18	External interrupt 18a	***[IBIMC063]***	***[IMNFLG4]***<INT159FLG>
		External interrupt 18b	***[IBIMC064]***	***[IMNFLG5]***<INT160FLG>

Table 4.10 Joint interruption list (2/2)

Interrupt No.	Interrupt Factor		Interrupt Control Register	Interrupt Monitor Register
121	DMAC transfer completion interrupt (INTDMAATC)	ch0	***[IBIMC000]***	***[IMNFLG3]***<INT096FLG>
		ch1	***[IBIMC001]***	***[IMNFLG3]***<INT097FLG>
		ch2	***[IBIMC002]***	***[IMNFLG3]***<INT098FLG>
		ch3	***[IBIMC003]***	***[IMNFLG3]***<INT099FLG>
		ch4	***[IBIMC004]***	***[IMNFLG3]***<INT100FLG>
		ch5	***[IBIMC005]***	***[IMNFLG3]***<INT101FLG>
		ch6	***[IBIMC006]***	***[IMNFLG3]***<INT102FLG>
		ch7	***[IBIMC007]***	***[IMNFLG3]***<INT103FLG>
		ch8	***[IBIMC008]***	***[IMNFLG3]***<INT104FLG>
		ch9	***[IBIMC009]***	***[IMNFLG3]***<INT105FLG>
		ch10	***[IBIMC010]***	***[IMNFLG3]***<INT106FLG>
		ch11	***[IBIMC011]***	***[IMNFLG3]***<INT107FLG>
		ch12	***[IBIMC012]***	***[IMNFLG3]***<INT108FLG>
		ch13	***[IBIMC013]***	***[IMNFLG3]***<INT109FLG>
		ch14	***[IBIMC014]***	***[IMNFLG3]***<INT110FLG>
		ch15	***[IBIMC015]***	***[IMNFLG3]***<INT111FLG>
		ch16	***[IBIMC016]***	***[IMNFLG3]***<INT112FLG>
		ch17	***[IBIMC017]***	***[IMNFLG3]***<INT113FLG>
		ch18	***[IBIMC018]***	***[IMNFLG3]***<INT114FLG>
		ch19	***[IBIMC019]***	***[IMNFLG3]***<INT115FLG>
		ch20	***[IBIMC020]***	***[IMNFLG3]***<INT116FLG>
		ch21	***[IBIMC021]***	***[IMNFLG3]***<INT117FLG>
		ch22	***[IBIMC022]***	***[IMNFLG3]***<INT118FLG>
		ch23	***[IBIMC023]***	***[IMNFLG3]***<INT119FLG>
		ch24	***[IBIMC024]***	***[IMNFLG3]***<INT120FLG>
		ch25	***[IBIMC025]***	***[IMNFLG3]***<INT121FLG>
		ch26	***[IBIMC026]***	***[IMNFLG3]***<INT122FLG>
		ch27	***[IBIMC027]***	***[IMNFLG3]***<INT123FLG>
		ch28	***[IBIMC028]***	***[IMNFLG3]***<INT124FLG>
		ch29	***[IBIMC029]***	***[IMNFLG3]***<INT125FLG>
		ch30	***[IBIMC030]***	***[IMNFLG3]***<INT126FLG>
		ch31	***[IBIMC031]***	***[IMNFLG3]***<INT127FLG>

Table 4.11 Combination interruption list

Interrupt No.	Coupled Interrupt factor	Interrupt Factor	Interrupt Request	Interrupt Control Register	Interrupt Monitor Register
60	INTSC0RX	INTT0RX	TSPI ch0 reception interrupt		
		INTUART0RX	UART ch0 reception interrupt		
61	INTSC0TX	INTT0TX	TSPI ch0 transmit interrupt		
		INTUART0TX	UART ch0 transmit interrupt		
62	INTSC0ERR	INTT0ERR	TSPI ch0 error interrupt		
		INTUART0ERR	UART ch0 error interrupt		
63	INTSC1RX	INTT1RX	TSPI ch1 reception interrupt		
		INTUART1RX	UART ch1 reception interrupt		
64	INTSC1TX	INTT1TX	TSPI ch1 transmit interrupt		
		INTUART1TX	UART ch1 transmit interrupt		
65	INTSC1ERR	INTT1ERR	TSPI ch1 error interrupt		
		INTUART1ERR	UART ch1 error interrupt		
72	INTI2C0NST	INTI2C0	I2C ch0 interrupt		
		INTI2C0ST	EI2C ch0 status interrupt		
73	INTI2C0ATX	INTI2C0AL	I2C ch0 arbitration lost detection interrupt		
		INTI2C0TBE	EI2C ch0 transmit buffer empty interrupt		
74	INTI2C0BRX	INTI2C0BF	I2C ch0 bus free detection interrupt		
		INTI2C0RBF	EI2C ch0 receive buffer full interrupt		
76	INTI2C1NST	INTI2C1	I2C ch1 interrupt		
		INTI2C1ST	EI2C ch1 status interrupt		
77	INTI2C1ATX	INTI2C1AL	I2C ch1 arbitration lost detection interrupt		
		INTI2C1TBE	EI2C ch1 transmit buffer empty interrupt		
78	INTI2C1BRX	INTI2C1BF	I2C ch1 bus free detection interrupt		
		INTI2C1RBF	EI2C ch1 receive buffer full interrupt		

Note: Select these interrupts on each IP side. Please select only one IP.

4.5. Interrupt detection level

When using interrupt via INTIF, interrupt detection level ("Low" level / "High" level / Rising edge / Falling edge) can be selected by interrupt control register A or B. The detected interrupt is output to the CPU with a "High" level signal.

The interrupt signals which are directly transmitted from the various peripheral functions to the CPU, a "High" pulse is output to the CPU as an interrupt request.

The CPU detects the interrupt signal "High" to be an interrupt factor.

4.5.1. Precautions When Releasing the Low Power Consumption Mode

The following setting should be done when releasing STOP1 mode.

- The setup of the interrupt control register. (***[IBIMCxxx]***)
  Interrupt detection level, Interrupt detection enable/disable.

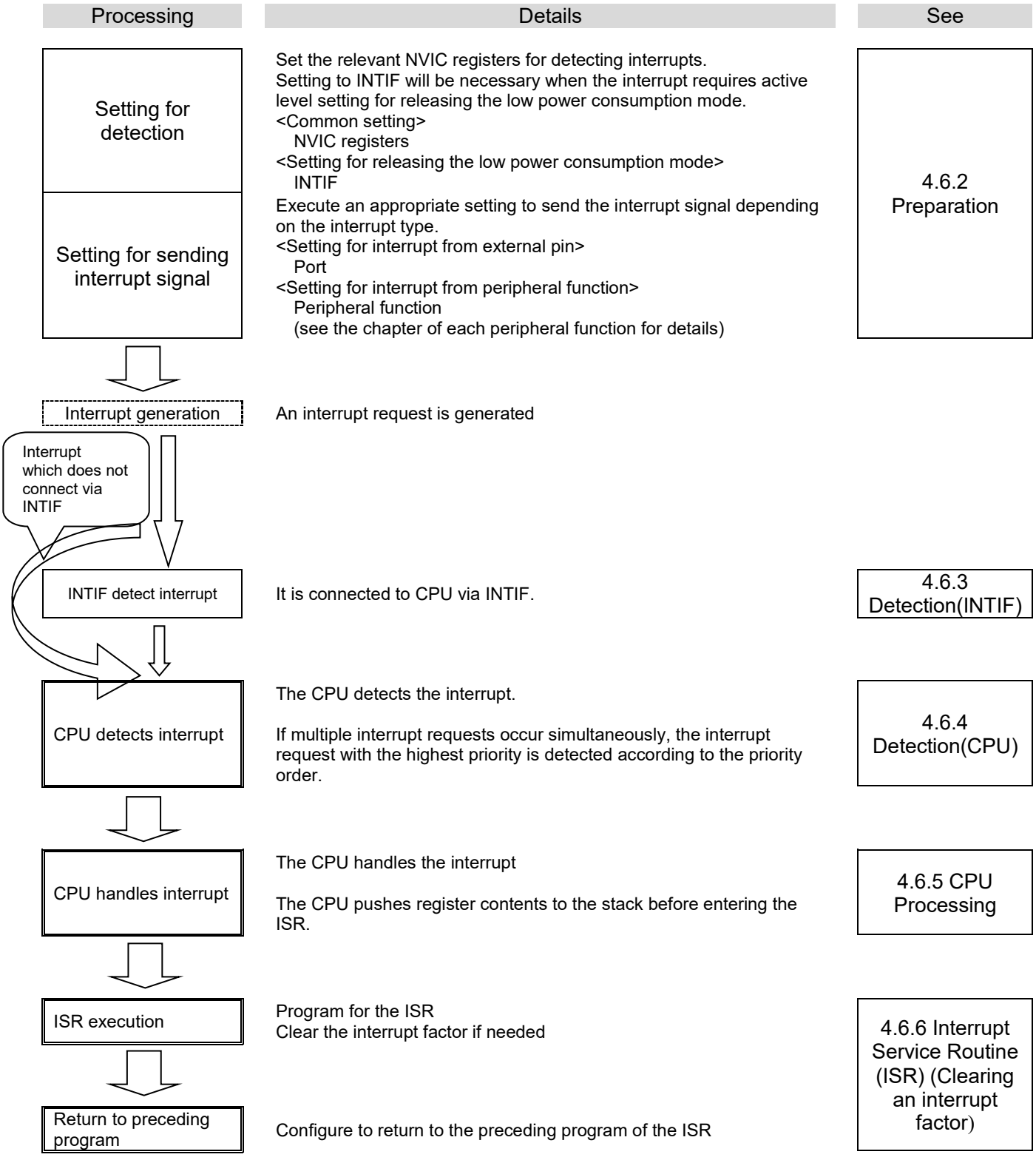
- The setup of the NVIC interrupt enable set register
  Enable setup.

In order to return to NORMAL mode from STOP1 mode, resume suspended instruction by jumping into interrupt after high speed clock oscillation.

4.6. Interrupt Handling

4.6.1. Flowchart

The following shows how an interrupt is handled.
The flowchart below explains the interrupt handling process by hardware and software.



4.6.2. Preparation

When preparing for an interrupt, you need to pay attention to the order of configuration to avoid any unexpected interrupt on the way.

Initiating an interrupt or changing its configuration must be implemented in the following order basically. First, disable the interrupt by the CPU. Then, configure from the farthest route from the CPU. Finally, enable the interrupt by the CPU.

To configure the INTIF, you must follow the order indicated here not to cause any unexpected interrupt. First, configure the precondition. Secondly, clear the data related to the interrupt in the INTIF and then enable the interrupt.

The following sections are listed in the order of interrupt handling and describe how to configure them.

1. Disabling interrupt by CPU
2. CPU registers setting
3. Preconfiguration (1) (Interrupt from external pin)
4. Preconfiguration (2) (Interrupt from peripheral function)
5. Preconfiguration (3) (Interrupt Set-Pending Register)
6. Configuring the INTIF
7. Enabling interrupt by CPU

(1) Disabling Interrupt by CPU

To make the CPU for not accepting any interrupt, write "1" to the corresponding bit of the ***[PRIMASK]*** Register. All interrupts and exceptions other than non-maskable interrupts and hard faults can be masked.

Use "MSR" instruction to set this register.

Interrupt Mask Register		
[PRIMASK]	←	"1" (interrupt disabled)

Note 1: ***[PRIMASK]*** Register cannot be modified in the user access level

Note 2: If a fault causes when "1" is set to the ***[PRIMASK]*** Register, it is treated as a hard fault.

(2) CPU Registers Setting

You can assign a priority level by writing to <PRI_n> field in an Interrupt Priority Register in the NVIC.

Each interrupt factor is provided with eight bits for assigning a priority level from 0 to 255, but the number of bits actually used varies with each product. Priority level 0 is the highest priority level. If multiple sources have the same priority, the smallest-numbered interrupt factor has the highest priority.

You can assign grouping priority by using the <PRIGROUP> in the Application Interrupt and Reset Control Register.

NVIC Register		
<PRI_n>	←	"Priority"
<PRIGROUP>	←	"group priority" (This is configurable if required)

Note: "n" indicates the number of the corresponding exceptions/interrupts. This product uses four bits for assigning a priority level.

(3) Preconfiguration (1) (Interrupt from external pin)

In order to use external interrupt pin, it is necessary to do proper setting to the port function register of the corresponding pin. Setting ***[PxIE]***<PxmIE> to "1" allows the pin to be used as the function pin and the input port.

Port Register		
[PxIE]<PxmIE>	←	"1"

Note: x: port number, m: corresponding bit of function register number. Be careful not to enable interrupts that are not used when performing interrupt setting. Also be aware of the description of "4.3.5 Precautions When Using External Interrupt Pins"

(4) Preconfiguration (2) (Interrupt from peripheral function)

The setting varies depending on the peripheral function to be used. See the reference manual of each peripheral function for details

(5) Preconfiguration (3) (Interrupt from Set-Pending Register)

To generate an interrupt by using the Interrupt Set-Pending Register, set the corresponding bit of this register to "1".

NVIC Register		
<SETPEND>	←	"1"

Note: <SETPEND>: corresponding bit

(6) Configuring the INTIF

The interrupt by way of INTIF sets the permission of the interrupt detection in interrupt control registers.

The ***[IANIC00]***/***[IBNIC00]***/***[IBIMCxxx]*** registers are capable of configuring each interrupt factor. Before enabling an interrupt detection, clear the interrupt request having active level in order to avoid unexpected interrupt.

For details of the interrupt control register, refer to the following.

Interrupt Control Register		
[IBIMCxxx]<INTMODE>	←	Value corresponding to the interrupt to be used (Only for the interrupt having interrupt detection level)
[IANIC00]<INTNCLR> ***[IBNIC00]***<INTPCLR> ***IBIMCxxx]***<INTPCLR><INTNCLR>	←	Interrupt request clear to use
[IBIMCxxx]<INTEN>	←	"1" (Interrupt detection enabled)

Note: xxx: number specific to the interrupt request

(7) Enabling Interrupt by CPU

Enable the interrupt by the CPU as shown below.

Clear the suspended interrupt in the Interrupt Clear-Pending Register. Enable the intended interrupt with the Interrupt Set-Enable Register. Each bit of the register is assigned to a single interrupt factor.

Writing "1" to the corresponding bit of the Interrupt Clear-Pending Register clears the suspended interrupt. Writing "1" to the corresponding bit of the Interrupt Set-Enable Register enables the intended interrupt.

To generate interrupts in the Interrupt Set-Pending Register setting, factors to trigger interrupts are lost if pending interrupts are cleared. Thus, this operation is not necessary.

At the end, ***[PRIMASK]*** register is zero cleared.

NVIC Register		
<CLRPEND>	←	"1"
<SETENA>	←	"1"
Interrupt Mask Register		
[PRIMASK]	←	"0"

Note 1: <CLRPEND>,<SETENA>: corresponding bit

Note 2: [PRIMASK] Register cannot be modified by the user access level;

4.6.3. Detection (INTIF)

When the INTIF detects an interrupt request, it sends the interrupt signal in "High" level to the CPU.

INTIF has the functions of the interrupt detection level selection logic, the functions of interrupt detection logic, and the function of the interrupt enable/disable. Each function of INTIF is set up by the interrupt control register A or B.

It keeps sending the interrupt signal in "High" level to the CPU until the interrupt detection flag is cleared in the Interrupt Control Register. If the ISR is exited without clearing the interrupt request, the same interrupt will be detected again when normal operation is resumed. Thus, be sure to clear each interrupt detection flag in the ISR.

At the same time, the corresponding Interrupt Monitor Register is also cleared

4.6.4. Detection (CPU)

The CPU detects an interrupt request with the highest priority.

4.6.5. CPU Processing

On detecting an interrupt, the CPU pushes the contents of xPSR, PC, LR, r12, and r3 to r0 to the stack then enter the ISR.

4.6.6. Interrupt Service Routine (ISR) (Clearing an interrupt factor)

An ISR requires specific programming according to the application to be used. This section describes what is recommended at the service routine programming and how the factor is cleared.

(1) Process in the Interrupt Service Routine

An ISR normally pushes register contents to the stack and handles an interrupt as required.

The Cortex-M4 processor with FPU automatically pushes the contents of xPSR, PC, LR, r12, and r3 to r0 to the stack. No extra programming is required for them.

Push the contents of other registers if needed.

Interrupt requests with higher priority and exceptions such as NMI are accepted even when an ISR is being executed. We recommend you to push the contents of general-purpose registers that might be rewritten.

(2) Clearing an Interrupt Factor

Some interrupt requests have to be cleared with the Interrupt Control Register.

If an interrupt detection level is set as level-sensitive, an interrupt request continues to exist until it is cleared at its factor. Therefore, the interrupt factor must be cleared. If a factor is withdrawn in level detection, the interrupt request signal from INTIF will be withdrawn automatically.

A factor is withdrawn by clearing the detection flag of the Interrupt Control Register of INTIF in the case of edge detection. When an effective edge occurs again, it is anew recognized as a factor.

Note: After clearing the interrupt flag of the Interrupt Control Register, please be sure to read the flag which was cleared.

5. Exception/Interrupt-Related Registers

5.1. Register List

Control Registers and their addresses are as follows;

Interrupt Control Register A

Peripheral function		Channel/Unit	Base Address
Interrupt control register A	IA	-	0x4003E000

Register name		Address(+BASE)
Non-Maskable Interrupt A Control Register 00	***[IANIC00]***	0x0000

Note: Byte access is needed for ***[IANIC00]***.

Interrupt Control Registers B

Peripheral function		Channel/Unit	Base address
Interrupt control register B	IB	-	0x40083200

Register name		Address(+BASE)
Non-Maskable Interrupt B Control Register 00	***[IBNIC00]***	0x0010
Interrupt B Mode Control Register 000	***[IBIMC000]***	0x0060
Interrupt B Mode Control Register 001	***[IBIMC001]***	0x0061
Interrupt B Mode Control Register 002	***[IBIMC002]***	0x0062
Interrupt B Mode Control Register 003	***[IBIMC003]***	0x0063
Interrupt B Mode Control Register 004	***[IBIMC004]***	0x0064
Interrupt B Mode Control Register 005	***[IBIMC005]***	0x0065
Interrupt B Mode Control Register 006	***[IBIMC006]***	0x0066
Interrupt B Mode Control Register 007	***[IBIMC007]***	0x0067
Interrupt B Mode Control Register 008	***[IBIMC008]***	0x0068
Interrupt B Mode Control Register 009	***[IBIMC009]***	0x0069
Interrupt B Mode Control Register 010	***[IBIMC010]***	0x006A
Interrupt B Mode Control Register 011	***[IBIMC011]***	0x006B
Interrupt B Mode Control Register 012	***[IBIMC012]***	0x006C
Interrupt B Mode Control Register 013	***[IBIMC013]***	0x006D
Interrupt B Mode Control Register 014	***[IBIMC014]***	0x006E
Interrupt B Mode Control Register 015	***[IBIMC015]***	0x006F
Interrupt B Mode Control Register 016	***[IBIMC016]***	0x0070
Interrupt B Mode Control Register 017	***[IBIMC017]***	0x0071
Interrupt B Mode Control Register 018	***[IBIMC018]***	0x0072
Interrupt B Mode Control Register 019	***[IBIMC019]***	0x0073
Interrupt B Mode Control Register 020	***[IBIMC020]***	0x0074
Interrupt B Mode Control Register 021	***[IBIMC021]***	0x0075
Interrupt B Mode Control Register 022	***[IBIMC022]***	0x0076
Interrupt B Mode Control Register 023	***[IBIMC023]***	0x0077
Interrupt B Mode Control Register 024	***[IBIMC024]***	0x0078
Interrupt B Mode Control Register 025	***[IBIMC025]***	0x0079
Interrupt B Mode Control Register 026	***[IBIMC026]***	0x007A
Interrupt B Mode Control Register 027	***[IBIMC027]***	0x007B
Interrupt B Mode Control Register 028	***[IBIMC028]***	0x007C
Interrupt B Mode Control Register 029	***[IBIMC029]***	0x007D
Interrupt B Mode Control Register 030	***[IBIMC030]***	0x007E
Interrupt B Mode Control Register 031	***[IBIMC031]***	0x007F
Interrupt B Mode Control Register 032	***[IBIMC032]***	0x0080
Interrupt B Mode Control Register 033	***[IBIMC033]***	0x0081
Interrupt B Mode Control Register 034	***[IBIMC034]***	0x0082
Interrupt B Mode Control Register 035	***[IBIMC035]***	0x0083
Interrupt B Mode Control Register 036	***[IBIMC036]***	0x0084
Interrupt B Mode Control Register 037	***[IBIMC037]***	0x0085
Interrupt B Mode Control Register 038	***[IBIMC038]***	0x0086
Interrupt B Mode Control Register 039	***[IBIMC039]***	0x0087
Interrupt B Mode Control Register 040	***[IBIMC040]***	0x0088
Interrupt B Mode Control Register 041	***[IBIMC041]***	0x0089
Interrupt B Mode Control Register 042	***[IBIMC042]***	0x008A
Interrupt B Mode Control Register 043	***[IBIMC043]***	0x008B
Interrupt B Mode Control Register 044	***[IBIMC044]***	0x008C
Interrupt B Mode Control Register 045	***[IBIMC045]***	0x008D
Interrupt B Mode Control Register 046	***[IBIMC046]***	0x008E
Interrupt B Mode Control Register 047	***[IBIMC047]***	0x008F

Interrupt B Mode Control Register 048	***[IBIMC048]***	0x0090
Interrupt B Mode Control Register 049	***[IBIMC049]***	0x0091
Interrupt B Mode Control Register 050	***[IBIMC050]***	0x0092
Interrupt B Mode Control Register 051	***[IBIMC051]***	0x0093
Interrupt B Mode Control Register 052	***[IBIMC052]***	0x0094
Interrupt B Mode Control Register 053	***[IBIMC053]***	0x0095
Interrupt B Mode Control Register 054	***[IBIMC054]***	0x0096
Interrupt B Mode Control Register 055	***[IBIMC055]***	0x0097
Interrupt B Mode Control Register 056	***[IBIMC056]***	0x0098
Interrupt B Mode Control Register 057	***[IBIMC057]***	0x0099
Interrupt B Mode Control Register 058	***[IBIMC058]***	0x009A
Interrupt B Mode Control Register 059	***[IBIMC059]***	0x009B
Interrupt B Mode Control Register 060	***[IBIMC060]***	0x009C
Interrupt B Mode Control Register 061	***[IBIMC061]***	0x009D
Interrupt B Mode Control Register 062	***[IBIMC062]***	0x009E
Interrupt B Mode Control Register 063	***[IBIMC063]***	0x009F
Interrupt B Mode Control Register 064	***[IBIMC064]***	0x00A0
Reserved		0x00A1
Reserved		0x00A2
Reserved		0x00A3
Reserved		0x00A4
Interrupt B Mode Control Register 069	***[IBIMC069]***	0x00A5

Note: Byte access is needed for ***[IBNIC00]*** and ***[IBIMCxxx]*** Registers

Reset Flag Registers

Peripheral function		Channel/Unit	Base address
Low-speed oscillation/power control/reset	RLM	-	0x4003E400

Register name		Address(+BASE)
Reset Flag Register 0	***[RLMRSTFLG0]***	0x0002
Reset Flag Register 1	***[RLMRSTFLG1]***	0x0003

Note: Byte access is needed for Reset Flag Registers.

Interrupt Monitor Registers

Peripheral function		Channel/Unit	Base address
Interrupt Monitor	IMN	-	0x40083300

Register name		Address(+BASE)
Non-Maskable Interrupt Monitor Flag Register	***[IMNFLGNMI]***	0x0000
Interrupt Monitor Flag Register 3	***[IMNFLG3]***	0x000C
Interrupt Monitor Flag Register 4	***[IMNFLG4]***	0x0010
Interrupt Monitor Flag Register 5	***[IMNFLG5]***	0x0014

NVIC Registers

Peripheral function		Channel/Unit	Base address
NVIC Register	-	-	0xE000E000

Register name	Address (+Base)
SysTick Control and Status Register	0x0010
SysTick Reload Value Register	0x0014
SysTick Current Value Register	0x0018
SysTick Calibration Value Register	0x001C
Interrupt Set-Enable Register 0	0x0100
Interrupt Set-Enable Register 1	0x0104
Interrupt Set-Enable Register 2	0x0108
Interrupt Set-Enable Register 3	0x010C
Interrupt Clear-Enable Register 0	0x0180
Interrupt Clear-Enable Register 1	0x0184
Interrupt Clear-Enable Register 2	0x0188
Interrupt Clear-Enable Register 3	0x018C
Interrupt Set-Pending Register 0	0x0200
Interrupt Set-Pending Register 1	0x0204
Interrupt Set-Pending Register 2	0x0208
Interrupt Set-Pending Register 3	0x020C
Interrupt Clear-Pending Register 0	0x0280
Interrupt Clear-Pending Register 1	0x0284
Interrupt Clear-Pending Register 2	0x0288
Interrupt Clear-Pending Register 3	0x028C
Interrupt Priority Register	0x0400 to 0x0457
Vector Table Offset Register	0x0D08
Application Interrupt and Reset Control Register	0x0D0C
System Handler Priority Register	0x0D18, 0x0D1C, 0x0D20
System Handler Control and Status Register	0x0D24

5.2. Interrupt Control Register A

5.2.1. *[IANIC00]* (Non-Maskable Interrupt A Control Register 00)

Bit	Bit Symbol	After reset	Type	Function
7	INTNCLR	0	W	Detection flag clear control 0: - 1: Clear Reading the bit returns "0"
6	-	0	R	Read as "0"
5	INTNFLG	0	R	Detection flag 0: Not detected 1: Detected
4:0	-	00101	R	Read as "00101"

5.3. Interrupt Control Registers B

5.3.1. *[IBNIC00]* (Non-Maskable Interrupt B Control Register 00)

Bit	Bit Symbol	After Reset	Type	Function
7	-	0	R	Read as "0"
6	INTPCLR	0	W	Detection flag clear control 0: - 1: Clear Reading the bit returns "0"
5	-	0	R	Read as "0"
4	INTPFLG	0	R	Detection flag 0: Not detected 1: Detected
3:0	-	0111	R	Read as "0111"

5.3.2. *[IBIMC000 to 064, 069]* (Interrupt B Mode Control Registers)

(1) *[IBIMC000* to *032]* Registers

Bit	Bit Symbol	After Reset	Type	Function
7	-	0	R	Read as "0"
6	INTPCLR	0	W	Detection flag clear control 0: - 1: Clear Reading the bit returns "0"
5	-	0	R	Read as "0"
4	INTPFLG	0	R	Detection flag 0: Not detected 1: Detected
3:0	-	0111	R	Read as "0111"

(2) *[IBIMC033* to *064, 069]* Register

Bit	Bit Symbol	After Reset	Type	Function
7	INTNCLR	0	W	Falling edge detection flag clear control 0: - 1: Clear Reading the bit returns "0"
6	INTPCLR	0	W	Rising edge detection flag clear control 0: - 1: Clear Reading the bit returns "0"
5	INTNFLG	0	R	Falling edge detection flag 0: Not detected 1: Detected
4	INTPFLG	0	R	Rising edge detection flag 0: Not detected 1: Detected
3:1	INTMODE[2:0]	000	R/W	Interrupt detection level selection 000: Low level 001: High level 010: Falling edge 011: Rising edge 100: Both edge 101: Reserved 110: Reserved 111: Reserved
0	INTEN	0	R/W	Interrupt control 0: Interrupt detection disabled 1: Interrupt detection enabled

5.4. Reset Flag Registers

5.4.1. *[RLMRSTFLG0]* (Reset Flag Register 0)

Bit	Bit Symbol	After power on reset	Type	Function
7:6	-	Undefined	R	Read as an undefined valule.
5	LVDRSTF	Undefined	R	LVD / PORF reset flag 0: - 1: Reset by LVD / PORF
			W	LVD / PORF reset flag 0: Clear 1: don't care
4	-	Undefined	R	Read as an undefined value.
3	PINRSTF	Undefined	R	Reset pin flag 0: - 1: Reset by reset pin
			W	Reset pin flag 0: Clear 1: don't care
2:1	-	Undefined	R	Read as an undefined value.
0	PORSTF	1	R	Power on reset flag 0: - 1: Reset by power on reset
			W	Power on reset flag 0: Clear 1: don't care

Note: Reset flags except <PORSTF> become undefined after power on reset release. When the release of power on reset is detected, please write "0" into all ~~the~~ reset flags for initializing.

5.4.2. *[RLMRSTFLG1]* (Reset Flag Register 1)

Bit	Bit Symbol	After power on reset	Type	Function
7:4	-	0	R	Read as "0"
3	OFDRSTF	0	R	OFD reset flag 0: - 1: Reset by OFD
			W	OFD reset flag 0: Clear 1: don't care
2	WDTRSTF	0	R	SIWDT reset flag 0: - 1: Reset by SIWDT
			W	SIWDT reset flag 0: Clear 1: don't care
1	LOCKRSTF	0	R	LOCKUP reset flag 0: - 1: Reset by LOCKUP
			W	LOCKUP reset flag 0: Clear 1: don't care
0	SYSRSTF	0	R	<SYSRESETREQ> reset flag 0: - 1: Reset by <SYSRESETREQ>
			W	<SYSRESETREQ> reset flag 0: Clear 1: don't care

5.5. Interrupt Monitor Registers

5.5.1. *[IMNFLGNMI]* (Non-Maskable Interrupt Monitor Flag Register)

Bit	Bit Symbol	After Reset	Type	Function
31:17	-	0	R	Read as "0"
16	INT016FLG	0	R	INTWDT0 Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
15:1	-	0	R	Read as "0"
0	INT000FLG	0	R	INTLVD Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected

5.5.2. *[IMNFLG3]* (Interrupt Monitor Flag Register 3)

Bit	Bit Symbol	After Reset	Type	Function
31	INT127FLG	0	R	INTDMAATC(ch31) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
30	INT126FLG	0	R	INTDMAATC(ch30) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
29	INT125FLG	0	R	INTDMAATC(ch29) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
28	INT124FLG	0	R	INTDMAATC(ch28) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
27	INT123FLG	0	R	INTDMAATC(ch27) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
26	INT122FLG	0	R	INTDMAATC(ch26) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
25	INT121FLG	0	R	INTDMAATC(ch25) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
24	INT120FLG	0	R	INTDMAATC(ch24) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
23	INT119FLG	0	R	INTDMAATC(ch23) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
22	INT118FLG	0	R	INTDMAATC(ch22) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
21	INT117FLG	0	R	INTDMAATC(ch21) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
20	INT116FLG	0	R	INTDMAATC(ch20) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
19	INT115FLG	0	R	INTDMAATC(ch19) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected

Bit	Bit Symbol	After Reset	Type	Function
18	INT114FLG	0	R	INTDMAATC(ch18) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
17	INT113FLG	0	R	INTDMAATC(ch17) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
16	INT112FLG	0	R	INTDMAATC(ch16) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
15	INT111FLG	0	R	INTDMAATC(ch15) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
14	INT110FLG	0	R	INTDMAATC(ch14) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
13	INT109FLG	0	R	INTDMAATC(ch13) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
12	INT108FLG	0	R	INTDMAATC(ch12) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
11	INT107FLG	0	R	INTDMAATC(ch11) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
10	INT106FLG	0	R	INTDMAATC(ch10) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
9	INT105FLG	0	R	INTDMAATC(ch9) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
8	INT104FLG	0	R	INTDMAATC(ch8) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
7	INT103FLG	0	R	INTDMAATC(ch7) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
6	INT102FLG	0	R	INTDMAATC(ch6) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
5	INT101FLG	0	R	INTDMAATC(ch5) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
4	INT100FLG	0	R	INTDMAATC(ch4) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
3	INT099FLG	0	R	INTDMAATC(ch3) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
2	INT098FLG	0	R	INTDMAATC(ch2) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
1	INT097FLG	0	R	INTDMAATC(ch1) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
0	INT096FLG	0	R	INTDMAATC(ch0) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected

5.5.3. *[IMNFLG4]* (Interrupt Monitor Flag Register 4)

Bit	Bit Symbol	After Reset	Type	Function
31	INT159FLG	0	R	INT18a(PD5) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
30	INT158FLG	0	R	INT17b(PD0) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
29	INT157FLG	0	R	INT17a(PD1) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
28	INT156FLG	0	R	INT16b(PN2) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
27	INT155FLG	0	R	INT16a(PN1) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
26	INT154FLG	0	R	INT15(PA1) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
25	INT153FLG	0	R	INT14b(PF5) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
24	INT152FLG	0	R	INT14a(PF4) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
23	INT151FLG	0	R	INT13(PU5) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
22	INT150FLG	0	R	INT12(PU0) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
21	INT149FLG	0	R	INT11b(PE5) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
20	INT148FLG	0	R	INT11a(PE4) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
19	INT147FLG	0	R	INT10(PC2) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
18	INT146FLG	0	R	INT09(PU6) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
17	INT145FLG	0	R	INT08b(PU4) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
16	INT144FLG	0	R	INT08a(PU3) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
15	INT143FLG	0	R	INT07b(PU2) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected

Bit	Bit Symbol	After Reset	Type	Function
14	INT142FLG	0	R	INT07a(PU1) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
13	INT141FLG	0	R	INT06b(PF2) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
12	INT140FLG	0	R	INT06a(PF1) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
11	INT139FLG	0	R	INT05b(PE6) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
10	INT138FLG	0	R	INT05a(PE5) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
9	INT137FLG	0	R	INT04b(PE1) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
8	INT136FLG	0	R	INT04a(PE3) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
7	INT135FLG	0	R	INT03b(PD2) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
6	INT134FLG	0	R	INT03a(PC3) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
5	INT133FLG	0	R	INT02b(PC6) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
4	INT132FLG	0	R	INT02a(PC1) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
3	INT131FLG	0	R	INT01b(PA3) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
2	INT130FLG	0	R	INT01a(PA4) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
1	INT129FLG	0	R	INT00(PA2) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
0	INT128FLG	0	R	INTDMAAERR Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected

5.5.4. *[IMNFLG5]* (Interrupt Monitor Flag Register 5)

Bit	Bit Symbol	After Reset	Type	Function
31:6	-	0	R	Read as "0"
5	INT165FLG	0	R	INT21(PG3) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
4	-	0	R	Read as "0"
3	-	0	R	Read as "0"
2	-	0	R	Read as "0"
1	-	0	R	Read as "0"
0	INT160FLG	0	R	INT18b(PD4) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected

5.6. NVIC Registers

5.6.1. SysTick Control and Status Register

Bit	Bit Symbol	After Reset	Type	Function
31:17	-	0	R	Read as "0"
16	COUNTFLAG	0	R/W	0: Timer not counted to 0 1: Timer counted to 0 Returns "1" if timer counted to "0" since last time this was read. Clears on read of any part of the SysTick Control and Status Register.
15:3	-	0	R	Read as "0"
2	CLKSOURCE	0	R/W	0: External reference clock (fosc/64) 1: CPU clock(fsys)
1	TICKINT	0	R/W	0: Do not pend SysTick 1: Pend SysTick
0	ENABLE	0	R/W	0: Disable 1: Enable If this bit is set to "1", the value of the Reload Value Register is loaded to counter and count starts.

5.6.2. SysTick Reload Value Register

Bit	Bit Symbol	After Reset	Type	Function
31:24	-	0	R	Read as "0"
23:0	RELOAD[23:0]	Undefined	R/W	Reload value Set the value to load into the SysTick Current Value Register when the timer reaches "0".

5.6.3. SysTick Current Value Register

Bit	Bit Symbol	After Reset	Type	Function
31:24	-	0	R	Read as "0"
23:0	CURRENT[23:0]	Undefined	R	Current SysTick timer value
			W	Clear Writing to this register with any value clears it to 0. Clearing this register also clears the <COUNTFLAG> bit of the SysTick Control and Status Register.

5.6.4. SysTick Calibration Value Register

Bit	Bit Symbol	After Reset	Type	Function
31	NOREF	0	R	0: Reference clock provided 1: No reference clock
30	SKEW	1	R	0: Calibration value is 10ms. 1: Calibration value is not 10ms.
29:24	-	0	R	Read as "0"
23:0	TENMS	0x000000	R	Calibration value (Note)

Note: This product does not prepare the calibration value.

5.6.5. Interrupt Control Registers

Following four registers will be used to control each interrupt factor; Interrupt Set-Enable Register, Interrupt Clear-Enable Register, Interrupt Set-Pending Register, and Interrupt Clear-Pending Register.

5.6.5.1. Interrupt Set-Enable Register

Each bit corresponds to the specified number of interrupt. It can enable interrupts and check if interrupts are enabled.

Writing "1" to a bit in this register enables the corresponding interrupt.

Writing "0" has no effect.

Reading the bits can see the enable/disable condition of the corresponding interrupts. Writing "1" to a corresponding bit in the Interrupt Clear-Enable Register clears the bit in this register.

(a) Interrupt Set-Enable Register 0

Bit	Bit Symbol	After Reset	Type	Function
31	SETENA (Interrupt31)	0	R/W	[Write] 1: Enable interrupt [Read] 0: Interrupt is disabled 1: Interrupt is enabled
30	SETENA (Interrupt 30)	0		
29	SETENA (Interrupt 29)	0		
28	SETENA (Interrupt 28)	0		
27	SETENA (Interrupt 27)	0		
26	SETENA (Interrupt 26)	0		
25	SETENA (Interrupt 25)	0		
24	SETENA (Interrupt 24)	0		
23	SETENA (Interrupt 23)	0		
22	SETENA (Interrupt 22)	0		
21	SETENA (Interrupt 21)	0		
20	-	0	R/W	Write as "0"
19	-	0	R/W	Write as "0"
18	SETENA (Interrupt 18)	0	R/W	[Write] 1: Enable interrupt [Read] 0: Interrupt is disabled 1: Interrupt is enabled
17	SETENA (Interrupt 17)	0		
16	SETENA (Interrupt 16)	0		
15	SETENA (Interrupt 15)	0		
14	SETENA (Interrupt 14)	0		
13	SETENA (Interrupt 13)	0		
12	SETENA (Interrupt 12)	0		
11	SETENA (Interrupt 11)	0		
10	SETENA (Interrupt 10)	0		
9	SETENA (Interrupt 9)	0		
8	SETENA (Interrupt 8)	0		
7	SETENA (Interrupt 7)	0		
6	SETENA (Interrupt 6)	0		
5	SETENA (Interrupt 5)	0		
4	SETENA (Interrupt 4)	0		
3	SETENA (Interrupt 3)	0		
2	SETENA (Interrupt 2)	0		
1	SETENA (Interrupt 1)	0		
0	SETENA (Interrupt 0)	0		

(b) Interrupt Set-Enable Register 1

Bit	Bit Symbol	After Reset	Type	Function
31	SETENA (Interrupt 63)	0	R/W	[Write] 1: Enable interrupt [Read] 0: Interrupt is disabled 1: Interrupt is enabled
30	SETENA (Interrupt 62)	0		
29	SETENA (Interrupt 61)	0		
28	SETENA (Interrupt 60)	0		
27	SETENA (Interrupt 59)	0		
26	SETENA (Interrupt 58)	0		
25	SETENA (Interrupt 57)	0		
24	SETENA (Interrupt 56)	0		
23	SETENA (Interrupt 55)	0		
22	SETENA (Interrupt 54)	0		
21	SETENA (Interrupt 53)	0		
20	SETENA (Interrupt 52)	0		
19	SETENA (Interrupt 51)	0		
18	SETENA (Interrupt 50)	0		
17	SETENA (Interrupt 49)	0		
16	SETENA (Interrupt 48)	0		
15	SETENA (Interrupt 47)	0		
14	SETENA (Interrupt 46)	0		
13	SETENA (Interrupt 45)	0		
12	SETENA (Interrupt 44)	0		
11	SETENA (Interrupt 43)	0		
10	SETENA (Interrupt 42)	0		
9	SETENA (Interrupt 41)	0		
8	SETENA (Interrupt 40)	0		
7	SETENA (Interrupt 39)	0		
6	SETENA (Interrupt 38)	0		
5	SETENA (Interrupt 37)	0		
4	SETENA (Interrupt 36)	0		
3	SETENA (Interrupt 35)	0		
2	SETENA (Interrupt 34)	0		
1	SETENA (Interrupt 33)	0		
0	SETENA (Interrupt 32)	0		

(c) Interrupt Set-Enable Register 2

Bit	Bit Symbol	After Reset	Type	Function
31	SETENA (Interrupt 95)	0	R/W	[Write] 1: Enable interrupt [Read] 0: Interrupt is disabled 1: Interrupt is enabled
30	SETENA (Interrupt 94)	0		
29	SETENA (Interrupt 93)	0		
28	SETENA (Interrupt 92)	0		
27	SETENA (Interrupt 91)	0		
26	SETENA (Interrupt 90)	0		
25	SETENA (Interrupt 89)	0		
24	SETENA (Interrupt 88)	0		
23	SETENA (Interrupt 87)	0		
22	SETENA (Interrupt 86)	0		
21	SETENA (Interrupt 85)	0		
20	SETENA (Interrupt 84)	0		
19	SETENA (Interrupt 83)	0		
18	SETENA (Interrupt 82)	0		
17	SETENA (Interrupt 81)	0		
16	SETENA (Interrupt 80)	0		
15	SETENA (Interrupt 79)	0		
14	SETENA (Interrupt 78)	0		
13	SETENA (Interrupt 77)	0		
12	SETENA (Interrupt 76)	0		
11	SETENA (Interrupt 75)	0		
10	SETENA (Interrupt 74)	0		
9	SETENA (Interrupt 73)	0		
8	SETENA (Interrupt 72)	0		
7	SETENA (Interrupt 71)	0		
6	SETENA (Interrupt 70)	0		
5	SETENA (Interrupt 69)	0		
4	SETENA (Interrupt 68)	0		
3	SETENA (Interrupt 67)	0		
2	SETENA (Interrupt 66)	0		
1	SETENA (Interrupt 65)	0		
0	SETENA (Interrupt 64)	0		

(d) Interrupt Set-Enable Register 3

Bit	Bit Symbol	After Reset	Type	Function
31:29	-	0	R	Read as "0"
28	SETENA (Interrupt 124)	0	R/W	[Write] 1: Enable interrupt [Read] 0: Interrupt is disabled 1: Interrupt is enabled
27	SETENA (Interrupt 123)	0		
26	SETENA (Interrupt 122)	0		
25	SETENA (Interrupt 121)	0		
24	SETENA (Interrupt 120)	0		
23	SETENA (Interrupt 119)	0		
22	SETENA (Interrupt 118)	0		
21	SETENA (Interrupt 117)	0		
20	SETENA (Interrupt 116)	0		
19	SETENA (Interrupt 115)	0		
18	SETENA (Interrupt 114)	0		
17	SETENA (Interrupt 113)	0		
16	SETENA (Interrupt 112)	0		
15	SETENA (Interrupt 111)	0		
14	SETENA (Interrupt 110)	0		
13	SETENA (Interrupt 109)	0		
12	SETENA (Interrupt 108)	0		
11	SETENA (Interrupt 107)	0		
10	SETENA (Interrupt 106)	0		
9	SETENA (Interrupt 105)	0		
8	SETENA (Interrupt 104)	0		
7	SETENA (Interrupt 103)	0		
6	SETENA (Interrupt 102)	0		
5	SETENA (Interrupt 101)	0		
4	SETENA (Interrupt 100)	0		
3	SETENA (Interrupt 99)	0		
2	SETENA (Interrupt 98)	0		
1	SETENA (Interrupt 97)	0		
0	SETENA (Interrupt 96)	0		

5.6.5.2. Interrupt Clear-Enable Register

Each bit corresponds to the specified number of interrupt. It can disable interrupts and check if interrupts are disabled.

Writing "1" to a bit in this register disables the corresponding interrupt.

Writing "0" has no effect.

Reading the bits can see the enable/disable condition of the corresponding interrupts.

(a) Interrupt Clear-Enable Register 0

Bit	Bit Symbol	After Reset	Type	Function
31	CLRENA (Interrupt 31)	0	R/W	[Write] 1: Disable Interrupt [Read] 0: Interrupt is disabled 1: Interrupt is enabled
30	CLRENA (Interrupt 30)	0		
29	CLRENA (Interrupt 29)	0		
28	CLRENA (Interrupt 28)	0		
27	CLRENA (Interrupt 27)	0		
26	CLRENA (Interrupt 26)	0		
25	CLRENA (Interrupt 25)	0		
24	CLRENA (Interrupt 24)	0		
23	CLRENA (Interrupt 23)	0		
22	CLRENA (Interrupt 22)	0		
21	CLRENA (Interrupt 21)	0		
20	-	0	R/W	Write as "1"
19	-	0	R/W	Write as "1"
18	CLRENA (Interrupt 18)	0	R/W	[Write] 1: Disable Interrupt [Read] 0: Interrupt is disabled 1: Interrupt is enabled
17	CLRENA (Interrupt 17)	0		
16	CLRENA (Interrupt 16)	0		
15	CLRENA (Interrupt 15)	0		
14	CLRENA (Interrupt 14)	0		
13	CLRENA (Interrupt 13)	0		
12	CLRENA (Interrupt 12)	0		
11	CLRENA (Interrupt 11)	0		
10	CLRENA (Interrupt 10)	0		
9	CLRENA (Interrupt 9)	0		
8	CLRENA (Interrupt 8)	0		
7	CLRENA (Interrupt 7)	0		
6	CLRENA (Interrupt 6)	0		
5	CLRENA (Interrupt 5)	0		
4	CLRENA (Interrupt 4)	0		
3	CLRENA (Interrupt 3)	0		
2	CLRENA (Interrupt 2)	0		
1	CLRENA (Interrupt 1)	0		
0	CLRENA (Interrupt 0)	0		

(b) Interrupt Clear-Enable Register 1

Bit	Bit Symbol	After Reset	Type	Function
31	CLRENA (Interrupt 63)	0	R/W	[Write] 1: Disable Interrupt [Read] 0: Interrupt is disabled 1: Interrupt is enabled
30	CLRENA (Interrupt 62)	0		
29	CLRENA (Interrupt 61)	0		
28	CLRENA (Interrupt 60)	0		
27	CLRENA (Interrupt 59)	0		
26	CLRENA (Interrupt 58)	0		
25	CLRENA (Interrupt 57)	0		
24	CLRENA (Interrupt 56)	0		
23	CLRENA (Interrupt 55)	0		
22	CLRENA (Interrupt 54)	0		
21	CLRENA (Interrupt 53)	0		
20	CLRENA (Interrupt 52)	0		
19	CLRENA (Interrupt 51)	0		
18	CLRENA (Interrupt 50)	0		
17	CLRENA (Interrupt 49)	0		
16	CLRENA (Interrupt 48)	0		
15	CLRENA (Interrupt 47)	0		
14	CLRENA (Interrupt 46)	0		
13	CLRENA (Interrupt 45)	0		
12	CLRENA (Interrupt 44)	0		
11	CLRENA (Interrupt 43)	0		
10	CLRENA (Interrupt 42)	0		
9	CLRENA (Interrupt 41)	0		
8	CLRENA (Interrupt 40)	0		
7	CLRENA (Interrupt 39)	0		
6	CLRENA (Interrupt 38)	0		
5	CLRENA (Interrupt 37)	0		
4	CLRENA (Interrupt 36)	0		
3	CLRENA (Interrupt 35)	0		
2	CLRENA (Interrupt 34)	0		
1	CLRENA (Interrupt 33)	0		
0	CLRENA (Interrupt 32)	0		

(c) Interrupt Clear-Enable Register 2

Bit	Bit Symbol	After Reset	Type	Function
31	CLRENA (Interrupt 95)	0	R/W	[[Write] 1: Disable Interrupt [Read] 0: Interrupt is disabled 1: Interrupt is enabled
30	CLRENA (Interrupt 94)	0		
29	CLRENA (Interrupt 93)	0		
28	CLRENA (Interrupt 92)	0		
27	CLRENA (Interrupt 91)	0		
26	CLRENA (Interrupt 90)	0		
25	CLRENA (Interrupt 89)	0		
24	CLRENA (Interrupt 88)	0		
23	CLRENA (Interrupt 87)	0		
22	CLRENA (Interrupt 86)	0		
21	CLRENA (Interrupt 85)	0		
20	CLRENA (Interrupt 84)	0		
19	CLRENA (Interrupt 83)	0		
18	CLRENA (Interrupt 82)	0		
17	CLRENA (Interrupt 81)	0		
16	CLRENA (Interrupt 80)	0		
15	CLRENA (Interrupt 79)	0		
14	CLRENA (Interrupt 78)	0		
13	CLRENA (Interrupt 77)	0		
12	CLRENA (Interrupt 76)	0		
11	CLRENA (Interrupt 75)	0		
10	CLRENA (Interrupt 74)	0		
9	CLRENA (Interrupt 73)	0		
8	CLRENA (Interrupt 72)	0		
7	CLRENA (Interrupt 71)	0		
6	CLRENA (Interrupt 70)	0		
5	CLRENA (Interrupt 69)	0		
4	CLRENA (Interrupt 68)	0		
3	CLRENA (Interrupt 67)	0		
2	CLRENA (Interrupt 66)	0		
1	CLRENA (Interrupt 65)	0		
0	CLRENA (Interrupt 64)	0		

(d) Interrupt Clear-Enable Register 3

Bit	Bit Symbol	After Reset	Type	Function
31:29	-	0	R	Read as "0"
28	CLRENA (Interrupt 124)	0	R/W	[Write] 1: Disable Interrupt [Read] 0: Interrupt is disabled 1: Interrupt is enabled
27	CLRENA (Interrupt 123)	0		
26	CLRENA (Interrupt 122)	0		
25	CLRENA (Interrupt 121)	0		
24	CLRENA (Interrupt 120)	0		
23	CLRENA (Interrupt 119)	0		
22	CLRENA (Interrupt 118)	0		
21	CLRENA (Interrupt 117)	0		
20	CLRENA (Interrupt 116)	0		
19	CLRENA (Interrupt 115)	0		
18	CLRENA (Interrupt 114)	0		
17	CLRENA (Interrupt 113)	0		
16	CLRENA (Interrupt 112)	0		
15	CLRENA (Interrupt 111)	0		
14	CLRENA (Interrupt 110)	0		
13	CLRENA (Interrupt 109)	0		
12	CLRENA (Interrupt 108)	0		
11	CLRENA (Interrupt 107)	0		
10	CLRENA (Interrupt 106)	0		
9	CLRENA (Interrupt 105)	0		
8	CLRENA (Interrupt 104)	0		
7	CLRENA (Interrupt 103)	0		
6	CLRENA (Interrupt 102)	0		
5	CLRENA (Interrupt 101)	0		
4	CLRENA (Interrupt 100)	0		
3	CLRENA (Interrupt 99)	0		
2	CLRENA (Interrupt 98)	0		
1	CLRENA (Interrupt 97)	0		
0	CLRENA (Interrupt 96)	0		

5.6.5.3. Interrupt Set-Pending Register

Each bit corresponds to the specified number of interrupt. It can force interrupts into the pending state and determines which interrupts are currently pending.

Writing "1" to a bit in this register pends the corresponding interrupt. However, writing "1" has no effect on an interrupt that is already pending or is disabled.

Writing "0" has no effect.

Reading the bit returns the current state of the corresponding interrupt.

Writing "1" to a corresponding bit in the Interrupt Clear-Pending Register clears the bit in this register.

(a) Interrupt Set-Pending Register 0

Bit	Bit Symbol	After Reset	Type	Function
31	SETPEND (Interrupt 31)	Undefined	R/W	[Write] 1: Pend interrupt [Read] 0: Not pending 1: Pending
30	SETPEND (Interrupt 30)	Undefined		
29	SETPEND (Interrupt 29)	Undefined		
28	SETPEND (Interrupt 28)	Undefined		
27	SETPEND (Interrupt 27)	Undefined		
26	SETPEND (Interrupt 26)	Undefined		
25	SETPEND (Interrupt 25)	Undefined		
24	SETPEND (Interrupt 24)	Undefined		
23	SETPEND (Interrupt 23)	Undefined		
22	SETPEND (Interrupt 22)	Undefined		
21	SETPEND (Interrupt 21)	Undefined		
20	-	Undefined	R/W	Write as "0"
19	-	Undefined	R/W	Write as "0"
18	SETPEND (Interrupt 18)	Undefined	R/W	[Write] 1: Pend interrupt [Read] 0: Not pending 1: Pending
17	SETPEND (Interrupt 17)	Undefined		
16	SETPEND (Interrupt 16)	Undefined		
15	SETPEND (Interrupt 15)	Undefined		
14	SETPEND (Interrupt 14)	Undefined		
13	SETPEND (Interrupt 13)	Undefined		
12	SETPEND (Interrupt 12)	Undefined		
11	SETPEND (Interrupt 11)	Undefined		
10	SETPEND (Interrupt 10)	Undefined		
9	SETPEND (Interrupt 9)	Undefined		
8	SETPEND (Interrupt 8)	Undefined		
7	SETPEND (Interrupt 7)	Undefined		
6	SETPEND (Interrupt 6)	Undefined		
5	SETPEND (Interrupt 5)	Undefined		
4	SETPEND (Interrupt 4)	Undefined		
3	SETPEND (Interrupt 3)	Undefined		
2	SETPEND (Interrupt 2)	Undefined		
1	SETPEND (Interrupt 1)	Undefined		
0	SETPEND (Interrupt 0)	Undefined		

(b) Interrupt Set-Pending Register 1

Bit	Bit Symbol	After Reset	Type	Function
31	SETPEND (Interrupt 63)	Undefined	R/W	[Write] 1: Pend interrupt [Read] 0: Not pending 1: Pending
30	SETPEND (Interrupt 62)	Undefined		
29	SETPEND (Interrupt 61)	Undefined		
28	SETPEND (Interrupt 60)	Undefined		
27	SETPEND (Interrupt 59)	Undefined		
26	SETPEND (Interrupt 58)	Undefined		
25	SETPEND (Interrupt 57)	Undefined		
24	SETPEND (Interrupt 56)	Undefined		
23	SETPEND (Interrupt 55)	Undefined		
22	SETPEND (Interrupt 54)	Undefined		
21	SETPEND (Interrupt 53)	Undefined		
20	SETPEND (Interrupt 52)	Undefined		
19	SETPEND (Interrupt 51)	Undefined		
18	SETPEND (Interrupt 50)	Undefined		
17	SETPEND (Interrupt 49)	Undefined		
16	SETPEND (Interrupt 48)	Undefined		
15	SETPEND (Interrupt 47)	Undefined		
14	SETPEND (Interrupt 46)	Undefined		
13	SETPEND (Interrupt 45)	Undefined		
12	SETPEND (Interrupt 44)	Undefined		
11	SETPEND (Interrupt 43)	Undefined		
10	SETPEND (Interrupt 42)	Undefined		
9	SETPEND (Interrupt 41)	Undefined		
8	SETPEND (Interrupt 40)	Undefined		
7	SETPEND (Interrupt 39)	Undefined		
6	SETPEND (Interrupt 38)	Undefined		
5	SETPEND (Interrupt 37)	Undefined		
4	SETPEND (Interrupt 36)	Undefined		
3	SETPEND (Interrupt 35)	Undefined		
2	SETPEND (Interrupt 34)	Undefined		
1	SETPEND (Interrupt 33)	Undefined		
0	SETPEND (Interrupt 32)	Undefined		

(c) Interrupt Set-Pending Register 2

Bit	Bit Symbol	After Reset	Type	Function
31	SETPEND (Interrupt 95)	Undefined	R/W	[Write] 1: Pend interrupt [Read] 0: Not pending 1: Pending
30	SETPEND (Interrupt 94)	Undefined		
29	SETPEND (Interrupt 93)	Undefined		
28	SETPEND (Interrupt 92)	Undefined		
27	SETPEND (Interrupt 91)	Undefined		
26	SETPEND (Interrupt 90)	Undefined		
25	SETPEND (Interrupt 89)	Undefined		
24	SETPEND (Interrupt 88)	Undefined		
23	SETPEND (Interrupt 87)	Undefined		
22	SETPEND (Interrupt 86)	Undefined		
21	SETPEND (Interrupt 85)	Undefined		
20	SETPEND (Interrupt 84)	Undefined		
19	SETPEND (Interrupt 83)	Undefined		
18	SETPEND (Interrupt 82)	Undefined		
17	SETPEND (Interrupt 81)	Undefined		
16	SETPEND (Interrupt 80)	Undefined		
15	SETPEND (Interrupt 79)	Undefined		
14	SETPEND (Interrupt 78)	Undefined		
13	SETPEND (Interrupt 77)	Undefined		
12	SETPEND (Interrupt 76)	Undefined		
11	SETPEND (Interrupt 75)	Undefined		
10	SETPEND (Interrupt 74)	Undefined		
9	SETPEND (Interrupt 73)	Undefined		
8	SETPEND (Interrupt 72)	Undefined		
7	SETPEND (Interrupt 71)	Undefined		
6	SETPEND (Interrupt 70)	Undefined		
5	SETPEND (Interrupt 69)	Undefined		
4	SETPEND (Interrupt 68)	Undefined		
3	SETPEND (Interrupt 67)	Undefined		
2	SETPEND (Interrupt 66)	Undefined		
1	SETPEND (Interrupt 65)	Undefined		
0	SETPEND (Interrupt 64)	Undefined		

(d) Interrupt Set-Pending Register 3

Bit	Bit Symbol	After Reset	Type	Function
31:29	-	0	R	Read as "0"
28	SETPEND (Interrupt 124)	Undefined	R/W	[Write] 1: Pend interrupt [Read] 0: Not pending 1: Pending
27	SETPEND (Interrupt 123)	Undefined		
26	SETPEND (Interrupt 122)	Undefined		
25	SETPEND (Interrupt 121)	Undefined		
24	SETPEND (Interrupt 120)	Undefined		
23	SETPEND (Interrupt 119)	Undefined		
22	SETPEND (Interrupt 118)	Undefined		
21	SETPEND (Interrupt 117)	Undefined		
20	SETPEND (Interrupt 116)	Undefined		
19	SETPEND (Interrupt 115)	Undefined		
18	SETPEND (Interrupt 114)	Undefined		
17	SETPEND (Interrupt 113)	Undefined		
16	SETPEND (Interrupt 112)	Undefined		
15	SETPEND (Interrupt 111)	Undefined		
14	SETPEND (Interrupt 110)	Undefined		
13	SETPEND (Interrupt 109)	Undefined		
12	SETPEND (Interrupt 108)	Undefined		
11	SETPEND (Interrupt 107)	Undefined		
10	SETPEND (Interrupt 106)	Undefined		
9	SETPEND (Interrupt 105)	Undefined		
8	SETPEND (Interrupt 104)	Undefined		
7	SETPEND (Interrupt 103)	Undefined		
6	SETPEND (Interrupt 102)	Undefined		
5	SETPEND (Interrupt 101)	Undefined		
4	SETPEND (Interrupt 100)	Undefined		
3	SETPEND (Interrupt 99)	Undefined		
2	SETPEND (Interrupt 98)	Undefined		
1	SETPEND (Interrupt 97)	Undefined		
0	SETPEND (Interrupt 96)	Undefined		

5.6.5.4. Interrupt Clear-Pending Register

Each bit corresponds to the specified number of interrupt. It can clear pending interrupts and determines which interrupts are currently pending.

Writing "1" to a bit in this register clears the corresponding pending interrupt. However, writing "1" has no effect on an interrupt that is already being serviced. Writing "0" has no effect.

Reading the bit returns the current state of the corresponding interrupt.

(a) Interrupt Clear-Pending Register 0

Bit	Bit Symbol	After Reset	Type	function
31	CLRPEND (Interrupt 31)	Undefined	R/W	[Write] 1: Clear pending interrupt [Read] 0: Not pending 1: Pending
30	CLRPEND (Interrupt 30)	Undefined		
29	CLRPEND (Interrupt 29)	Undefined		
28	CLRPEND (Interrupt 28)	Undefined		
27	CLRPEND (Interrupt 27)	Undefined		
26	CLRPEND (Interrupt 26)	Undefined		
25	CLRPEND (Interrupt 25)	Undefined		
24	CLRPEND (Interrupt 24)	Undefined		
23	CLRPEND (Interrupt 23)	Undefined		
22	CLRPEND (Interrupt 22)	Undefined		
21	CLRPEND (Interrupt 21)	Undefined		
20	-	Undefined	R/W	Write as "1"
19	-	Undefined	R/W	Write as "1"
18	CLRPEND (Interrupt 18)	Undefined	R/W	[Write] 1: Clear pending interrupt [Read] 0: Not pending 1: Pending
17	CLRPEND (Interrupt 17)	Undefined		
16	CLRPEND (Interrupt 16)	Undefined		
15	CLRPEND (Interrupt 15)	Undefined		
14	CLRPEND (Interrupt 14)	Undefined		
13	CLRPEND (Interrupt 13)	Undefined		
12	CLRPEND (Interrupt 12)	Undefined		
11	CLRPEND (Interrupt 11)	Undefined		
10	CLRPEND (Interrupt 10)	Undefined		
9	CLRPEND (Interrupt 9)	Undefined		
8	CLRPEND (Interrupt 8)	Undefined		
7	CLRPEND (Interrupt 7)	Undefined		
6	CLRPEND (Interrupt 6)	Undefined		
5	CLRPEND (Interrupt 5)	Undefined		
4	CLRPEND (Interrupt 4)	Undefined		
3	CLRPEND (Interrupt 3)	Undefined		
2	CLRPEND (Interrupt 2)	Undefined		
1	CLRPEND (Interrupt 1)	Undefined		
0	CLRPEND (Interrupt 0)	Undefined		

(b) Interrupt Clear-Pending Register 1

Bit	Bit Symbol	After Reset	Type	function
31	CLRPEND (Interrupt 63)	Undefined	R/W	[Write] 1: Clear pending interrupt [Read] 0: Not pending 1: Pending
30	CLRPEND (Interrupt 62)	Undefined		
29	CLRPEND (Interrupt 61)	Undefined		
28	CLRPEND (Interrupt 60)	Undefined		
27	CLRPEND (Interrupt 59)	Undefined		
26	CLRPEND (Interrupt 58)	Undefined		
25	CLRPEND (Interrupt 57)	Undefined		
24	CLRPEND (Interrupt 56)	Undefined		
23	CLRPEND (Interrupt 55)	Undefined		
22	CLRPEND (Interrupt 54)	Undefined		
21	CLRPEND (Interrupt 53)	Undefined		
20	CLRPEND (Interrupt 52)	Undefined		
19	CLRPEND (Interrupt 51)	Undefined		
18	CLRPEND (Interrupt 50)	Undefined		
17	CLRPEND (Interrupt 49)	Undefined		
16	CLRPEND (Interrupt 48)	Undefined		
15	CLRPEND (Interrupt 47)	Undefined		
14	CLRPEND (Interrupt 46)	Undefined		
13	CLRPEND (Interrupt 45)	Undefined		
12	CLRPEND (Interrupt 44)	Undefined		
11	CLRPEND (Interrupt 43)	Undefined		
10	CLRPEND (Interrupt 42)	Undefined		
9	CLRPEND (Interrupt 41)	Undefined		
8	CLRPEND (Interrupt 40)	Undefined		
7	CLRPEND (Interrupt 39)	Undefined		
6	CLRPEND (Interrupt 38)	Undefined		
5	CLRPEND (Interrupt 37)	Undefined		
4	CLRPEND (Interrupt 36)	Undefined		
3	CLRPEND (Interrupt 35)	Undefined		
2	CLRPEND (Interrupt 34)	Undefined		
1	CLRPEND (Interrupt 33)	Undefined		
0	CLRPEND (Interrupt 32)	Undefined		

(c) Interrupt Clear-Pending Register 2

Bit	Bit Symbol	After Reset	Type	function
31	CLRPEND (Interrupt 95)	Undefined	R/W	[Write] 1: Clear pending interrupt [Read] 0: Not pending 1: Pending
30	CLRPEND (Interrupt 94)	Undefined		
29	CLRPEND (Interrupt 93)	Undefined		
28	CLRPEND (Interrupt 92)	Undefined		
27	CLRPEND (Interrupt 91)	Undefined		
26	CLRPEND (Interrupt 90)	Undefined		
25	CLRPEND (Interrupt 89)	Undefined		
24	CLRPEND (Interrupt 88)	Undefined		
23	CLRPEND (Interrupt 87)	Undefined		
22	CLRPEND (Interrupt 86)	Undefined		
21	CLRPEND (Interrupt 85)	Undefined		
20	CLRPEND (Interrupt 84)	Undefined		
19	CLRPEND (Interrupt 83)	Undefined		
18	CLRPEND (Interrupt 82)	Undefined		
17	CLRPEND (Interrupt 81)	Undefined		
16	CLRPEND (Interrupt 80)	Undefined		
15	CLRPEND (Interrupt 79)	Undefined		
14	CLRPEND (Interrupt 78)	Undefined		
13	CLRPEND (Interrupt 77)	Undefined		
12	CLRPEND (Interrupt 76)	Undefined		
11	CLRPEND (Interrupt 75)	Undefined		
10	CLRPEND (Interrupt 74)	Undefined		
9	CLRPEND (Interrupt 73)	Undefined		
8	CLRPEND (Interrupt 72)	Undefined		
7	CLRPEND (Interrupt 71)	Undefined		
6	CLRPEND (Interrupt 70)	Undefined		
5	CLRPEND (Interrupt 69)	Undefined		
4	CLRPEND (Interrupt 68)	Undefined		
3	CLRPEND (Interrupt 67)	Undefined		
2	CLRPEND (Interrupt 66)	Undefined		
1	CLRPEND (Interrupt 65)	Undefined		
0	CLRPEND (Interrupt 64)	Undefined		

(d) Interrupt Clear-Pending Register 3

Bit	Bit Symbol	After Reset	Type	function
31:29	-	0	R	Read as "0"
28	CLRPEND (Interrupt 124)	Undefined	R/W	[Write] 1: Clear pending interrupt [Read] 0: Not pending 1: Pending
27	CLRPEND (Interrupt 123)	Undefined		
26	CLRPEND (Interrupt 122)	Undefined		
25	CLRPEND (Interrupt 121)	Undefined		
24	CLRPEND (Interrupt 120)	Undefined		
23	CLRPEND (Interrupt 119)	Undefined		
22	CLRPEND (Interrupt 118)	Undefined		
21	CLRPEND (Interrupt 117)	Undefined		
20	CLRPEND (Interrupt 116)	Undefined		
19	CLRPEND (Interrupt 115)	Undefined		
18	CLRPEND (Interrupt 114)	Undefined		
17	CLRPEND (Interrupt 113)	Undefined		
16	CLRPEND (Interrupt 112)	Undefined		
15	CLRPEND (Interrupt 111)	Undefined		
14	CLRPEND (Interrupt 110)	Undefined		
13	CLRPEND (Interrupt 109)	Undefined		
12	CLRPEND (Interrupt 108)	Undefined		
11	CLRPEND (Interrupt 107)	Undefined		
10	CLRPEND (Interrupt 106)	Undefined		
9	CLRPEND (Interrupt 105)	Undefined		
8	CLRPEND (Interrupt 104)	Undefined		
7	CLRPEND (Interrupt 103)	Undefined		
6	CLRPEND (Interrupt 102)	Undefined		
5	CLRPEND (Interrupt 101)	Undefined		
4	CLRPEND (Interrupt 100)	Undefined		
3	CLRPEND (Interrupt 99)	Undefined		
2	CLRPEND (Interrupt 98)	Undefined		
1	CLRPEND (Interrupt 97)	Undefined		
0	CLRPEND (Interrupt 96)	Undefined		

5.6.6. Interrupt Priority Register

Each interrupt is provided with eight bits of an Interrupt Priority Register.
The following shows the addresses of the Interrupt Priority Registers corresponding to interrupt numbers.

Address	31 24	23 16	15 8	7 0
0xE000E400	PRI_3	PRI_2	PRI_1	PRI_0
0xE000E404	PRI_7	PRI_6	PRI_5	PRI_4
0xE000E408	PRI_11	PRI_10	PRI_9	PRI_8
0xE000E40C	PRI_15	PRI_14	PRI_13	PRI_12
0xE000E410	-	PRI_18	PRI_17	PRI_16
0xE000E414	PRI_23	PRI_22	PRI_21	-
0xE000E418	PRI_27	PRI_26	PRI_25	PRI_24
0xE000E41C	PRI_31	PRI_30	PRI_29	PRI_28
0xE000E420	PRI_35	PRI_34	PRI_33	PRI_32
0xE000E424	PRI_39	PRI_38	PRI_37	PRI_36
0xE000E428	PRI_43	PRI_42	PRI_41	PRI_40
0xE000E42C	PRI_47	PRI_46	PRI_45	PRI_44
0xE000E430	PRI_51	PRI_50	PRI_49	PRI_48
0xE000E434	PRI_55	PRI_54	PRI_53	PRI_52
0xE000E438	PRI_59	PRI_58	PRI_57	PRI_56
0xE000E43C	PRI_63	PRI_62	PRI_61	PRI_60
0xE000E440	PRI_67	PRI_66	PRI_65	PRI_64
0xE000E444	PRI_71	PRI_70	PRI_69	PRI_68
0xE000E448	PRI_75	PRI_74	PRI_73	PRI_72
0xE000E44C	PRI_79	PRI_78	PRI_77	PRI_76
0xE000E450	PRI_83	PRI_82	PRI_81	PRI_80
0xE000E454	PRI_87	PRI_86	PRI_85	PRI_84
0xE000E458	PRI_91	PRI_90	PRI_89	PRI_88
0xE000E45C	PRI_95	PRI_94	PRI_93	PRI_92
0xE000E460	PRI_99	PRI_98	PRI_97	PRI_96
0xE000E464	PRI_103	PRI_102	PRI_101	PRI_100
0xE000E468	PRI_107	PRI_106	PRI_105	PRI_104
0xE000E46C	PRI_111	PRI_110	PRI_109	PRI_108
0xE000E470	PRI_115	PRI_114	PRI_113	PRI_112
0xE000E474	PRI_119	PRI_118	PRI_117	PRI_116
0xE000E478	PRI_123	PRI_122	PRI_121	PRI_120
0xE000E47C	-	-	-	PRI_124

The number of bits to be used for assigning a priority varies with each product. This product uses four bits for assigning a priority.

The following shows the fields of the Interrupt Priority Registers for interrupt numbers 0 to 3. The Interrupt Priority Registers for all other interrupt numbers have the identical fields. Unused bits return "0" when read, and writing to unused bits has no effect.

Bit	Bit Symbol	After Reset	Type	Function
31:28	PRI_3[3:0]	0000	R/W	Priority of interrupt number 3
27:24	-	0	R	Read as "0"
23:20	PRI_2[3:0]	0000	R/W	Priority of interrupt number 2
19:16	-	0	R	Read as "0"
15:12	PRI_1[3:0]	0000	R/W	Priority of interrupt number 1
11:8	-	0	R	Read as "0"
7:4	PRI_0[3:0]	0000	R/W	Priority of interrupt number 0
3:0	-	0	R	Read as "0"

5.6.7. Vector Table Offset Register

Bit	Bit Symbol	After Reset	Type	Function
31:7	TBLOFF[24:0]	0x0000000	R/W	Offset value Set the offset value from the address of "0x00000000". The offset must be aligned based on the number of exceptions in the table. This means that the minimum alignment is 32 words that you can use for up to 16 interrupts. For more interrupts, you must adjust the alignment by rounding up to the next power of two.
6:0	-	0	R	Read as "0"

5.6.8. Application Interrupt and Reset Control Register

Bit	Bit Symbol	After Reset	Type	Function
31:16	VECTKEY/ VECTKEYSTAT[15:0]	Undefined	W	Register key Writing to this register requires 0x05FA in the <VECTKEY> field.
			R	Register key Read as "0xFA05".
15	ENDIANESS	0	R/W	Endianness bit: (Note 1) 1: Big endian 0: Little endian
14:11	-	0	R	Read as "0"
10:8	PRIGROUP[2:0]	000	R/W	Interrupt priority grouping 000: 7-bit of pre-emption priority, 1-bit of sub priority 001: 6-bit of pre-emption priority, 2-bit of sub priority 010: 5-bit of pre-emption priority, 3-bit of sub priority 011: 4-bit of pre-emption priority, 4-bit of sub priority 100: 3-bit of pre-emption priority, 5-bit of sub priority 101: 2-bit of pre-emption priority, 6-bit of sub priority 110: 1-bit of pre-emption priority, 7-bit of sub priority 111: no pre-emption priority, 8-bit of sub priority This field configures to split the interrupt priority register <PRI_n> into pre-emption priority and sub priority.
7:3	-	0	R	Read as "0"
2	SYSRESETREQ	0	R/W	System Reset Request 1: CPU outputs a SYSRESETREQ signal. (Note 2)
1	VECTCLRACTIVE	0	R/W	Clear active vector bit 1: clear all state information for active NMI, fault, and interrupts. 0: do not clear This bit self-clears. It is the responsibility of the application to reinitialize the stack.
0	VECTRESET	0	R/W	System Reset bit 1: reset system 0: do not reset system Resets the system, with the exception of debug components (FPB, DWT and ITM) by setting this bit to "1" and this bit is also zero cleared

Note 1: Little-endian is the default memory format for this product.

Note 2: When SYSRESETREQ is output, warm reset is performed on this product. <SYSRESETREQ> is cleared by warm reset.

5.6.9. System Handler Priority Register

Each exception is provided with eight bits of a System Handler Priority Register.
The following shows the addresses of the System Handler Priority Registers corresponding to each exception.

Address	31 24	23 16	15 8	7 0
0xE000ED18	PRI_7	PRI_6 (Usage Fault)	PRI_5 (Bus Fault)	PRI_4 (Memory Management)
0xE000ED1C	PRI_11 (SVCall)	PRI_10	PRI_9	PRI_8
0xE000ED20	PRI_15 (SysTick)	PRI_14 (PendSV)	PRI_13	PRI_12 (Debug Monitor)

The number of bits to be used for assigning a priority varies with each product. This product uses four bits for assigning a priority.

The following shows the fields of the System Handler Priority Registers for Usage Fault, Bus Fault, and Memory Management. Unused bits return "0" when read, and writing to unused bits has no effect.

Bit	Bit Symbol	After Reset	Type	Function
31:28	PRI_7[3:0]	0000	R/W	Reserved
27:24	-	0	R	Read as "0"
23:20	PRI_6[3:0]	0000	R/W	Priority of Usage Fault
19:16	-	0	R	Read as "0"
15:12	PRI_5[3:0]	0000	R/W	Priority of Bus Fault
11:8	-	0	R	Read as "0"
7:4	PRI_4[3:0]	0000	R/W	Priority of Memory Management
3:0	-	0	R	Read as "0"

5.6.10. System Handler Control and Status Register

Bit	Bit Symbol	After Reset	Type	Function
31:19	-	0	R	Read as "0"
18	USGFAULT ENA	0	R/W	Usage Fault 0: Disabled 1: Enabled
17	BUSFAULT ENA	0	R/W	Bus Fault 0: Disabled 1: Enabled
16	MEMFAULT ENA	0	R/W	Memory Management 0: Disabled 1: Enabled
15	SVCALL PENDED	0	R/W	SVCall 0: Not pended 1: Pended
14	BUSFAULT PENDED	0	R/W	Bus Fault 0: Not pended 1: Pended
13	MEMFAULT PENDED	0	R/W	Memory Management 0: Not pended 1: Pended
12	USGFAULT PENDED	0	R/W	Usage fault 0: Not pended 1: Pended
11	SYSTICKACT	0	R/W	SysTick 0: Inactive 1: Active
10	PENDSVACT	0	R/W	PendSV 0: Inactive 1: Active
9	-	0	R	Read as "0"
8	MONITOR ACT	0	R/W	Debug Monitor 0: Inactive 1: Active
7	SVCALLACT	0	R/W	SVCall 0: Inactive 1: Active
6:4	-	0	R	Read as "0"
3	USGFAULT ACT	0	R/W	Usage Fault 0: Inactive 1: Active
2	-	0	R	Read as "0"
1	BUSFAULT ACT	0	R/W	Bus Fault 0: Inactive 1: Active
0	MEMFAULT ACT	0	R/W	Memory Management 0: Inactive 1: Active

Note: You must clear or set the active bits with extreme caution because clearing or setting these bits does not repair stack contents.

6. List of Interrupt Factors for Each Product

6.1. TMPM4MN/TMPM4MM/TMPM4ML

Table 6.1 List of Interrupt Factors

M4MN	M4MM	M4ML	Interrupt No	Interrupt Factor	Interrupt Request	Interrupt Control Register	Interrupt Monitor Register
✓	✓	✓	NMI	INTLVD	LVD interrupt	***[IANIC00]***	***[IMNFLGNMI]*** <INT000FLG>
✓	✓	✓		INTWDT0	WDT interrupt	***[IBNIC00]***	***[IMNFLGNMI]*** <INT016FLG>
✓	✓	✓	0	INT00	External interrupt 00	***[IBIMC033]***	***[IMNFLG4]*** <INT129FLG>
✓	✓	✓	1	INT01	External interrupt 01a	***[IBIMC034]***	***[IMNFLG4]*** <INT130FLG>
✓	✓	✓			External interrupt 01b	***[IBIMC035]***	***[IMNFLG4]*** <INT131FLG>
✓	✓	✓	2	INT02	External interrupt 02a	***[IBIMC036]***	***[IMNFLG4]*** <INT132FLG>
✓	-	-			External interrupt 02b	***[IBIMC037]***	***[IMNFLG4]*** <INT133FLG>
✓	✓	✓	3	INT03	External interrupt 03a	***[IBIMC038]***	***[IMNFLG4]*** <INT134FLG>
✓	-	-			External interrupt 03b	***[IBIMC039]***	***[IMNFLG4]*** <INT135FLG>
✓	✓	✓	4	INT04	External interrupt 04a	***[IBIMC040]***	***[IMNFLG4]*** <INT136FLG>
✓	✓	✓			External interrupt 04b	***[IBIMC041]***	***[IMNFLG4]*** <INT137FLG>
✓	✓	✓	5	INT05	External interrupt 05a	***[IBIMC042]***	***[IMNFLG4]*** <INT138FLG>
✓	✓	✓			External interrupt 05b	***[IBIMC043]***	***[IMNFLG4]*** <INT139FLG>
✓	✓	✓	6	INT06	External interrupt 06a	***[IBIMC044]***	***[IMNFLG4]*** <INT140FLG>
✓	-	-			External interrupt 06b	***[IBIMC045]***	***[IMNFLG4]*** <INT141FLG>
✓	✓	✓	7	INT07	External interrupt 07a	***[IBIMC046]***	***[IMNFLG4]*** <INT142FLG>
✓	✓	✓			External interrupt 07b	***[IBIMC047]***	***[IMNFLG4]*** <INT143FLG>
✓	✓	✓	8	INT08	External interrupt 08a	***[IBIMC048]***	***[IMNFLG4]*** <INT144FLG>
✓	✓	✓			External interrupt 08b	***[IBIMC049]***	***[IMNFLG4]*** <INT145FLG>
✓	✓	✓	9	INT09	External interrupt 09	***[IBIMC050]***	***[IMNFLG4]*** <INT146FLG>
✓	✓	✓	10	INT10	External interrupt 10	***[IBIMC051]***	***[IMNFLG4]*** <INT147FLG>
✓	✓	✓	11	INT11	External interrupt 11a	***[IBIMC052]***	***[IMNFLG4]*** <INT148FLG>
✓	✓	✓			External interrupt 11b	***[IBIMC053]***	***[IMNFLG4]*** <INT149FLG>
✓	✓	✓	12	INT12	External interrupt 12	***[IBIMC054]***	***[IMNFLG4]*** <INT150FLG>
✓	✓	✓	13	INT13	External interrupt 13	***[IBIMC055]***	***[IMNFLG4]*** <INT151FLG>
✓	✓	-	14	INT14	External interrupt 14a	***[IBIMC056]***	***[IMNFLG4]*** <INT152FLG>
✓	-	-			External interrupt 14b	***[IBIMC057]***	***[IMNFLG4]*** <INT153FLG>
✓	✓	-	15	INT15	External interrupt 15	***[IBIMC058]***	***[IMNFLG4]*** <INT154FLG>
✓	✓	-	16	INT16	External interrupt 16a	***[IBIMC059]***	***[IMNFLG4]*** <INT155FLG>
✓	✓	-			External interrupt 16b	***[IBIMC060]***	***[IMNFLG4]*** <INT156FLG>

M4MN	M4MM	M4ML	Interrupt No	Interrupt Factor	Interrupt Request	Interrupt Control Register	Interrupt Monitor Register
✓	-	-	17	INT17	External interrupt 17a	***[IBIMC061]***	***[IMNFLG4]*** <INT157FLG>
✓	-	-			External interrupt 17b	***[IBIMC062]***	***[IMNFLG4]*** <INT158FLG>
✓	-	-	18	INT18	External interrupt 18a	***[IBIMC063]***	***[IMNFLG4]*** <INT159FLG>
✓	-	-			External interrupt 18b	***[IBIMC064]***	***[IMNFLG5]*** <INT160FLG>
-	-	-	19	Reserved			
-	-	-	20	Reserved			
✓	✓	✓	21	INT21	External interrupt 21	***[IBIMC069]***	***[IMNFLG5]*** <INT165FLG>
✓	✓	✓	22	INTVCN0	A-VE+ ch0 VE interrupt		
✓	✓	✓	23	INTVCT0	A-VE+ ch0 VE task end interrupt		
✓	✓	✓	24	INTEMG0	A-PMD ch0 EMG interrupt		
✓	✓	✓	25	INTEMG1	A-PMD ch1 EMG interrupt		
✓	✓	✓	26	INTEMG2	A-PMD ch2 EMG interrupt		
✓	✓	✓	27	INTOVV0	A-PMD ch0 OVV interrupt		
✓	✓	✓	28	INTOVV1	A-PMD ch1 OVV interrupt		
✓	✓	✓	29	INTOVV2	A-PMD ch2 OVV interrupt		
✓	✓	✓	30	INTPWM0	A-PMD ch0 PWM interrupt		
✓	✓	✓	31	INTPWM1	A-PMD ch1 PWM interrupt		
✓	✓	✓	32	INTPWM2	A-PMD ch2 PWM interrupt		
✓	✓	-	33	INTENC00	A-ENC32 ch0 Encoder input interrupt 0		
✓	✓	-	34	INTENC01	A-ENC32 ch0 Encoder input interrupt 1		
✓	✓	-	35	INTENC10	A-ENC32 ch1 Encoder input interrupt 0		
✓	✓	-	36	INTENC11	A-ENC32 ch1 Encoder input interrupt 1		
✓	✓	✓	37	INTENC20	A-ENC32 ch2 Encoder input interrupt 0		
✓	✓	✓	38	INTENC21	A-ENC32 ch2 Encoder input interrupt 1		
✓	✓	✓	39	INTADAPDA	ADC unit A PMD trigger program conversion complete A		
✓	✓	✓	40	INTADAPDB	ADC unit A PMD trigger program conversion complete B		
✓	✓	✓	41	INTADACP0	ADC unit A Monitor function 0 interrupt		
✓	✓	✓	42	INTADACP1	ADC unit A Monitor function 1 interrupt		
✓	✓	✓	43	INTADATRG	ADC unit A general trigger program conversion complete		
✓	✓	✓	44	INTADASGL	ADC unit A single program conversion completion		
✓	✓	✓	45	INTADACNT	ADC unit A continuous program conversion complete		
✓	✓	✓	46	INTADBPDA	ADC unit B PMD trigger program conversion complete A		
✓	✓	✓	47	INTADBPDB	ADC unit B PMD trigger program conversion complete B		
✓	✓	✓	48	INTADBCP0	ADC unit B Monitor function 0 interrupt		

M4MN	M4MM	M4ML	Interrupt No	Interrupt Factor	Interrupt Request	Interrupt Control Register	Interrupt Monitor Register
✓	✓	✓	49	INTADBCP1	ADC unit B Monitor function 1 interrupt		
✓	✓	✓	50	INTADBTRG	ADC unit B general trigger program conversion complete		
✓	✓	✓	51	INTADBSGL	ADC unit B single program conversion completion		
✓	✓	✓	52	INTADBCNT	ADC unit B continuous program conversion complete		
✓	✓	✓	53	INTADCPDA	ADC unit C PMD trigger program conversion complete A		
✓	✓	✓	54	INTADCPDB	ADC unit C PMD trigger program conversion complete B		
✓	✓	✓	55	INTADCCP0	ADC unit C Monitor function 0 interrupt		
✓	✓	✓	56	INTADCCP1	ADC unit C Monitor function 1 interrupt		
✓	✓	✓	57	INTADCTRG	ADC unit C general trigger program conversion complete		
✓	✓	✓	58	INTADCSGL	ADC unit C single program conversion completion		
✓	✓	✓	59	INTADCCNT	ADC unit C continuous program conversion complete		
✓	✓	✓	60	INTSC0RX (Note2)	TSPI ch0 reception interrupt / UART ch0 reception interrupt		
✓	✓	✓	61	INTSC0TX (Note2)	TSPI ch0 transmit interrupt / UART ch0 transmit interrupt		
✓	✓	✓	62	INTSC0ERR (Note2)	TSPI ch0 error interrupt / UART ch0 error interrupt		
✓	✓	✓	63	INTSC1RX (Note2)	TSPI ch1 reception interrupt / UART ch1 reception interrupt		
✓	✓	✓	64	INTSC1TX (Note2)	TSPI ch1 transmit interrupt / UART ch1 transmit interrupt		
✓	✓	✓	65	INTSC1ERR (Note2)	TSPI ch1 error interrupt / UART ch1 error interrupt		
✓	✓	✓	66	INTSC2RX (INTUART2RX)	UART ch2 reception interrupt		
✓	✓	✓	67	INTSC2TX (INTUART2TX)	UART ch2 transmit interrupt		
✓	✓	✓	68	INTSC2ERR (INTUART2ERR)	UART ch2 error interrupt		
✓	✓	-	69	INTSC3RX (INTUART3RX)	UART ch3 reception interrupt		
✓	✓	-	70	INTSC3TX (INTUART3TX)	UART ch3 transmit interrupt		
✓	✓	-	71	INTSC3ERR (INTUART3ERR)	UART ch3 error interrupt		
✓	✓	✓	72	INTI2C0NST (Note2)	I2C ch0 interrupt / EI2C ch0 status interrupt		
✓	✓	✓	73	INTI2C0ATX (Note2)	I2C ch0 arbitration lost detection interrupt / EI2C ch0 transmit buffer empty interrupt		
✓	✓	✓	74	INTI2C0BRX (Note2)	I2C ch0 bus free detection interrupt / EI2C ch0 receive buffer full interrupt		
✓	✓	✓	75	INTI2C0NA	I2C ch0 NACK detection interrupt		
✓	✓	✓	76	INTI2C1NST (Note2)	I2C ch1 interrupt / EI2C ch1 status interrupt		
✓	✓	✓	77	INTI2C1ATX (Note2)	I2C ch1 arbitration lost detection interrupt / EI2C ch1 transmit buffer empty interrupt		
✓	✓	✓	78	INTI2C1BRX (Note2)	I2C ch1 bus free detection interrupt / EI2C ch1 receive buffer full interrupt		
✓	✓	✓	79	INTI2C1NA	I2C ch1 NACK detection interrupt		
✓	✓	✓	80	INTCANAGLB	CAN unit A global interrupt		
✓	✓	✓	81	INTCANARXD	CAN unit A reception interrupt		
✓	✓	✓	82	INTCANATXD	CAN unit A transmit interrupt		
✓	✓	✓	83	INTT32A00AC	T32A ch0 timer A/C match, overflow, and underflow		

M4MN	M4MM	M4ML	Interrupt No	Interrupt Factor	Interrupt Request	Interrupt Control Register	Interrupt Monitor Register
✓	✓	✓	84	INTT32A00ACCAP0	T32A ch0 timer A/C capture 0		
✓	✓	✓	85	INTT32A00ACCAP1	T32A ch0 timer A/C capture 1		
✓	✓	✓	86	INTT32A00B	T32A ch0 timer B match, overflow, and underflow		
✓	✓	✓	87	INTT32A00BCAP0	T32A ch0 timer B capture 0		
✓	✓	✓	88	INTT32A00BCAP1	T32A ch0 timer B capture 1		
✓	✓	✓	89	INTT32A01AC	T32A ch1 timer A/C match, Overflow, and underflow		
✓	✓	✓	90	INTT32A01ACCAP0	T32A ch1 timer A/C capture 0		
✓	✓	✓	91	INTT32A01ACCAP1	T32A ch1 timer A/C capture 1		
✓	✓	✓	92	INTT32A01B	T32A ch1 timer B match, overflow, and underflow		
✓	✓	✓	93	INTT32A01BCAP0	T32A ch1 timer B capture 0		
✓	✓	✓	94	INTT32A01BCAP1	T32A ch1 timer B capture 1		
✓	✓	✓	95	INTT32A02AC	T32A ch2 timer A/C match, overflow, and underflow		
✓	✓	✓	96	INTT32A02ACCAP0	T32A ch2 timer A/C capture 0		
✓	✓	✓	97	INTT32A02ACCAP1	T32A ch2 timer A/C capture 1		
✓	✓	✓	98	INTT32A02B	T32A ch2 timer B match, overflow, and underflow		
✓	✓	✓	99	INTT32A02BCAP0	T32A ch2 timer B capture 0		
✓	✓	✓	100	INTT32A02BCAP1	T32A ch2 timer B capture 1		
✓	✓	✓	101	INTT32A03AC	T32A ch3 timer A/C match, overflow, and underflow		
✓	✓	✓	102	INTT32A03ACCAP0	T32A ch3 timer A/C capture 0		
✓	✓	✓	103	INTT32A03ACCAP1	T32A ch3 timer A/C capture 1		
✓	✓	✓	104	INTT32A03B	T32A ch3 timer B match, overflow, and underflow		
✓	✓	✓	105	INTT32A03BCAP0	T32A ch3 timer B capture 0		
✓	✓	✓	106	INTT32A03BCAP1	T32A ch3 timer B capture 1		
✓	✓	✓	107	INTT32A04AC	T32A ch4 timer A/C match, overflow, and underflow		
✓	✓	✓	108	INTT32A04ACCAP0	T32A ch4 timer A/C capture 0		
✓	✓	✓	109	INTT32A04ACCAP1	T32A ch4 timer A/C capture 1		
✓	✓	✓	110	INTT32A04B	T32A ch4 timer B match, overflow, and underflow		
✓	✓	✓	111	INTT32A04BCAP0	T32A ch4 timer B capture 0		
✓	✓	✓	112	INTT32A04BCAP1	T32A ch4 timer B capture 1		
✓	✓	✓	113	INTT32A05AC	T32A ch5 timer A/C match, overflow, and underflow		
✓	✓	✓	114	INTT32A05ACCAP0	T32A ch5 timer A/C capture 0		
✓	✓	✓	115	INTT32A05ACCAP1	T32A ch5 timer A/C capture 1		
✓	✓	✓	116	INTT32A05B	T32A ch5 timer B match, overflow, and underflow		
✓	✓	✓	117	INTT32A05BCAP0	T32A ch5 timer B capture 0		

M4MN	M4MM	M4ML	Interrupt No	Interrupt Factor	Interrupt Request	Interrupt Control Register	Interrupt Monitor Register
✓	✓	✓	118	INTT32A05BCAP1	T32A ch5 timer B capture 1		
✓	✓	✓	119	INTPARI0	RAM Parity interrupt 0		
✓	✓	✓	120	INTPARI1	RAM Parity interrupt 1		
✓	✓	✓	121	INTDMAATC	DMAC transfer completion interrupt (ch0 to 31)	***[IBIMC000]*** to ***[IBIMC031]*** (Note2)	***[IMNFLG3]*** <INT096FLG> to <INT127FLG> (Note2)
✓	✓	✓	122	INTDMAAERR	DMAC transfer error	***[IBIMC032]***	***[IMNFLG4]*** <INT128FLG>
✓	✓	✓	123	INTFLCRDY	Code FLASH Ready interrupt		
✓	✓	✓	124	INTFLDRDY	Data FLASH Ready interrupt		

Note1: ✓:Available, -: N/A

Note2: Please refer to "4.4.1. Joint interruption".

7. Revision History

Table 7.1 Revision History

Revision	Date	Description
1.0	2020-12-03	New Release

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