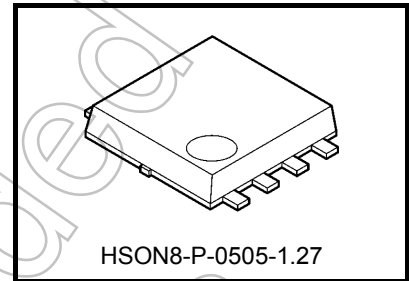


TB7106F

Buck DC-DC Converter IC

The TB7106F is a single-chip buck DC-DC converter IC that utilizing a chopper circuit. The TB7106F adopts bootstrap system and contains high-speed and low-on-resistance N-channel MOSFETs for the high side main switch to achieve high efficiency.

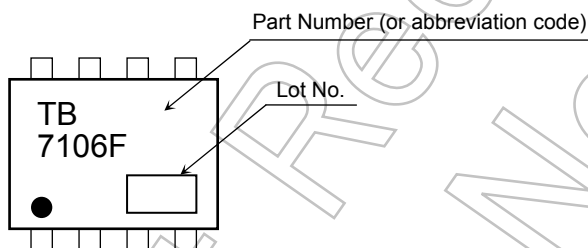


Weight: 0.068 g (typ.)

Features

- Enables up to 3 A of load current (I_{OUT}) with a minimum of external components.
- High efficiency ($\eta = 88\%$ typ.) (@V_{IN} = 12 V, V_{OUT} = 3.3 V and I_{OUT} = 1A)
- Operating voltage range: V_{IN} = 4.5 to 20 V
- Low ON-resistance: R_{DS (ON)} = 0.18 Ω (high-side) typical (@V_{IN} = 12 V, T_j = 25°C)
- Oscillation frequency: f_{OSC} = 380 kHz (typ.)
- Reference voltage: V_{FB} = 0.8 V $\pm 2.25\%$ (@ T_j = 25 °C)
- Because of an external phase compensation element, the optimal phase compensation according to the output filter capacitor can be realized.
- Allows the use of a small surface-mount ceramic capacitor as an output filter capacitor.
- Housed in a small surface-mount package (SOP Advance) with low thermal resistance.
- Soft-start time adjustable by an external capacitor

Part Marking



The dot (•) on the top surface indicates pin 1.

*: The lot number consists of three digits. The first digit represents the last digit of the year of manufacture, and the following two digits indicates the week of manufacture between 01 and either 52 or 53.



Manufacturing week code
(The first week of the year is 01; the last week is 52 or 53.)
Manufacturing year code (last digit of the year of manufacture)

This product has a MOS structure and is sensitive to electrostatic discharge. Handle with care.

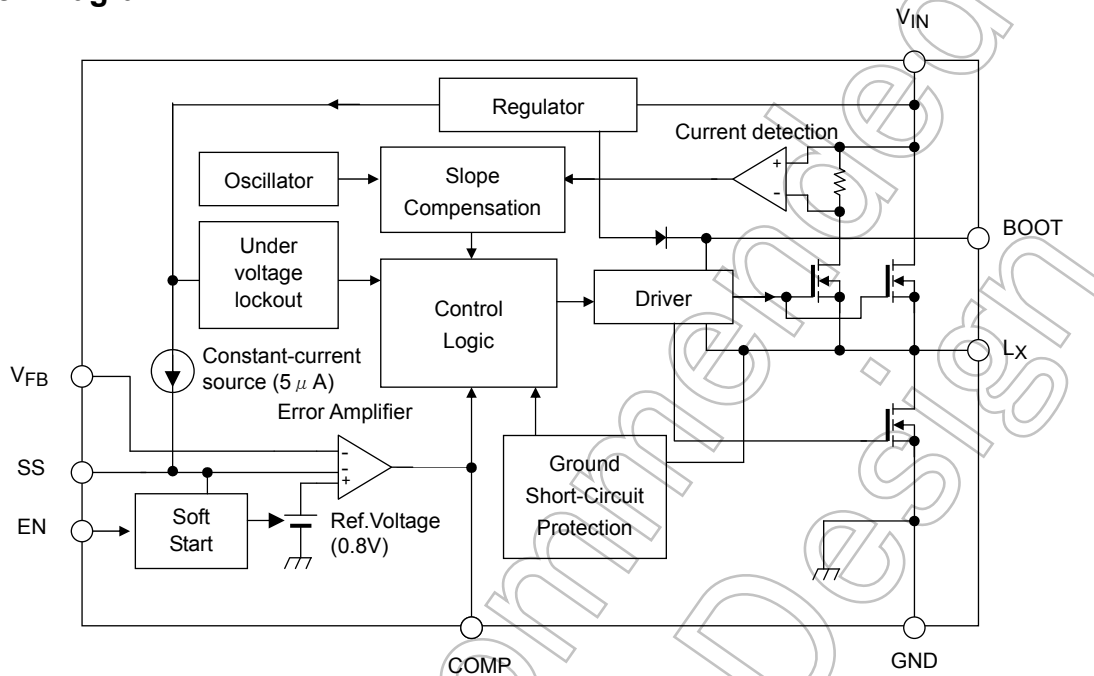
The product(s) in this document (“Product”) contain functions intended to protect the Product from temporary small overloads such as minor short-term overcurrent, or overheating. The protective functions do not necessarily protect Product under all circumstances. When incorporating Product into your system, please design the system to avoid such overloads upon the Product, and to shut down or otherwise relieve the Product of such overload conditions immediately upon occurrence. For details, please refer to the notes appearing below in this document and other documents referenced in this document.

Start of commercial production
2010-07

Ordering Information

Part Number	Shipping
TB7106F (TE12L, Q)	Embossed tape (3000 units per reel)

Block Diagram



Pin Description

Pin No.	Symbol	Description
1	BOOT	Bootstrap pin This pin is connected to Bootstrap capacitor. A 0.1μF bootstrap capacitor is required between BOOT pin and L _x pin.
2	V _{IN}	Input pin This pin is placed in the standby state if V _{EN} ="L". Standby current is 60 μA (@V _{IN} =12V) or less.
3	L _x	Switch pin This pin is connected to high-side N-channel MOSFET.
4	GND	Ground pin
5	V _{FB}	Feedback pin This input is fed into an internal error amplifier with a reference voltage of 0.8 V (typ.).
6	COMP	Phase compensation pin Pin for connecting an error amplifier phase compensation resistor and capacitor.
7	EN	Enable pin When V _{EN} ≥ 1.8 V (@ V _{IN} = 12 V), the internal circuitry is allowed to operate and thus enable the switching operation of the output section. When V _{EN} ≤ 0.5 V (@ V _{IN} = 12 V), the internal circuitry is disabled, putting the TB7106F in Standby mode. This pin has an internal pull-up current of 15 μA(typ.).
8	SS	Soft-start pin When the SS input is left open, the soft-start time is 1 ms (typ.). The soft-start time can be adjusted with an external capacitor. The external capacitor is charged from a 5μA (typ.) constant-current source, and the reference voltage of the error amplifier is regulated between 0 V and 0.8 V. The external capacitor is discharged when V _{EN} ="L" and in case of undervoltage lockout or thermal shutdown.

Absolute Maximum Ratings (Ta = 25°C)

Characteristics	Symbol	Rating	Unit
Input pin voltage	V _{IN}	-0.3~25	V
Bootstrap pin voltage	V _{BOOT}	-0.3~28	V
Bootstrap pin - Switch pin voltage	V _{BOOT} - V _{LX}	-0.3~6	V
Switch pin voltage (Note1)	V _{LX}	-0.3~25	V
Feedback pin voltage	V _{FB}	-0.3~6	V
Enable pin voltage	V _{EN}	-0.3~25	V
Soft-start pin voltage	V _{SS}	-0.3~6	V
Error amplifier phase compensation pin voltage	V _{COMP}	-0.3~6	V
Switch pin current	I _{LX}	-3.6	A
Power dissipation (Note 2)	P _D	2.2	W
Operating junction temperature	T _{jopr}	-40~125	°C
Junction temperature (Note 3)	T _j	150	°C
Storage temperature	T _{stg}	-55~150	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

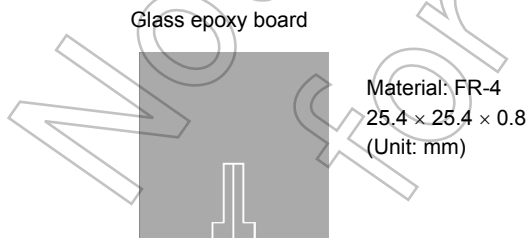
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc)

Note 1: The switch pin voltage (V_{LX}) doesn't include the peak voltage generated by TB7106F's switching.

Thermal Resistance Characteristics

Characteristics	Symbol	Max	Unit
Thermal resistance, junction to ambient	R _{th(j-a)}	44.6(Note2)	°C/W
Thermal resistance, junction to case (T _c =25°C)	R _{th(j-c)}	4.17	°C/W

Note 2:



Single-pulse measurement: pulse width t=10(s)

Note 3: The TB7106F may go into thermal shutdown at the rated maximum junction temperature. Thermal design is required to ensure that the rated maximum operating junction temperature, T_{jopr}, will not be exceeded.

Electrical Characteristics (T_j = 25°C, V_{IN} = 4.5 to 20 V, unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit	
Operating input voltage	V _{IN(OPR)}	—	4.5	—	20	V	
Input current	I _{IN}	V _{IN} = 12V, V _{EN} = 5V, V _{F_{FB}} = 2 V	—	1.8	2.5	mA	
Output voltage range	V _{OUT(OPR)}	V _{EN} = V _{IN}	0.8	—	V _{IN} - 2	V	
Standby current	I _{IN(STBY)}	V _{IN} = 12 V, V _{EN} = 0 V V _{F_{FB}} = 0.8 V	—	—	60	μA	
High-side switch leakage current	I _{LEAK(H)}	V _{IN} = 12 V, V _{EN} = 0 V V _{F_{FB}} = 0.8 V, V _{LX} = 0 V	—	—	10	μA	
EN threshold voltage	V _{IH(EN)}	V _{IN} = 12 V	1.8	—	—	V	
	V _{IL(EN)}	V _{IN} = 12V	—	—	0.5		
EN input current	I _{IH(EN)}	V _{IN} = 12V, V _{EN} = 5 V	-5	—	5	μA	
	I _{IL(EN)}	V _{IN} = 12V, V _{EN} = 0 V	—	-15	—		
V _{F_{FB}} input voltage	V _{F_{FB}}	V _{IN} = 12 V, V _{EN} = 5 V	0.782	0.8	0.818	V	
V _{F_{FB}} input current	I _{F_{FB}}	V _{IN} = 12 V, V _{EN} = 5 V V _{F_{FB}} = 2V	-1	—	1	μA	
Error amplifier phase compensation input current	I _{COMP(H)}	V _{IN} = 12 V, V _{EN} = 5 V V _{F_{FB}} = 0.7V, V _{COMP} = 0.5 V	—	-18	—	μA	
	I _{COMP(L)}	V _{IN} = 12 V, V _{EN} = 5 V V _{F_{FB}} = 0.9V, V _{COMP} = 0.5 V	—	18	—		
High-side switch on-state resistance	R _{DS(ON)(H)}	V _{IN} = 12V, V _{EN} = 5V I _{LX} = -1A	—	0.18	—	Ω	
Low-side switch on-state resistance	R _{DS(ON)(L)}	V _{IN} = 12 V, V _{EN} = 5 V I _{LX} = 100m A	—	1.5	—	Ω	
Oscillation frequency	f _{OSC}	V _{IN} = 12V, V _{EN} = 5V	300	380	460	kHz	
Internal soft-start time	t _{SS}	V _{IN} = 12 V, V _{EN} = 5V, I _{OUT} = 0A Measured between 0% and 90% points at V _{OUT}	0.5	1	2	ms	
External soft-start charge current	I _{SS}	V _{IN} = 12 V, V _{EN} = 5 V	-3	-5	-8	μA	
High-side switch duty cycle	D _{max}	V _{IN} = 12 V, V _{EN} = 5 V	—	88	—	%	
Thermal shutdown (TSD)	Detection temperature	T _{SD}	V _{IN} = 12 V, V _{EN} = 5 V	—	160	—	°C
	Hysteresis	ΔT _{SD}	V _{IN} = 12 V, V _{EN} = 5 V	—	15	—	
Undervoltage lockout (UVLO)	Detection voltage	V _{UV}	V _{EN} = V _{IN}	2.9	3.2	3.5	V
	Recovery voltage	V _{UVR}	V _{EN} = V _{IN}	3.2	3.5	3.8	
	Hysteresis	ΔV _{UV}	V _{EN} = V _{IN}	—	0.3	—	
L _X current limit	I _{LIM}	V _{IN} = 12V, V _{EN} = 5V V _{OUT} = 2 V	3.4	4.5	—	A	

Note on Electrical Characteristics

The test condition $T_j = 25^\circ\text{C}$ means a state where any drifts in electrical characteristics incurred by an increase in the chip's junction temperature can be ignored during pulse testing.

Application Circuit Example

Figure1 shows a typical application circuit using a low-ESR electrolytic or ceramic capacitor for C_{OUT} .

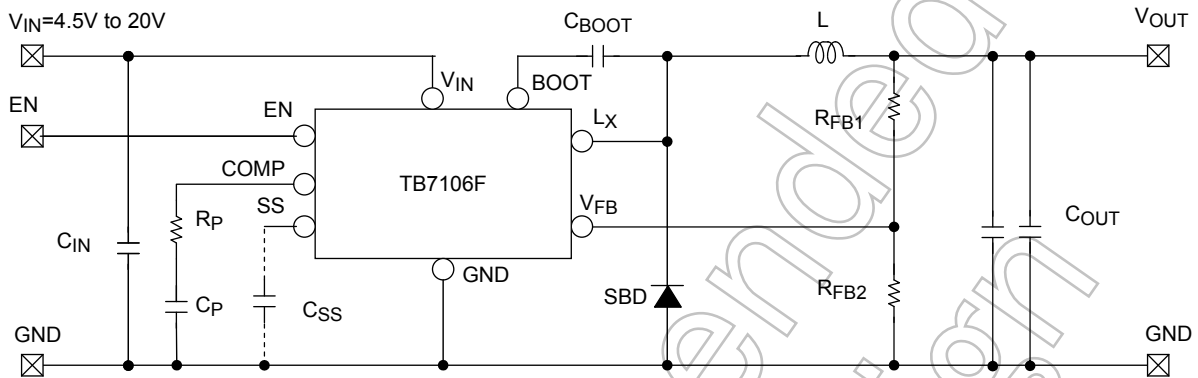


Figure 1 TB7106F Application Circuit Example

Component values (reference value@ $V_{IN} = 12\text{ V}$, $V_{OUT} = 3.3\text{ V}$, $T_a = 25^\circ\text{C}$)

C_{IN} : Input filter capacitor = $10\ \mu\text{F}$

(ceramic capacitor: GRM31CR71E106K manufactured by Murata Manufacturing Co., Ltd.)

C_{OUT} : Output filter capacitor = $22\ \mu\text{F} \times 2$

(ceramic capacitor: GRM31CB31C226ME15L manufactured by Murata Manufacturing Co., Ltd.)

R_{FB1} : Output voltage setting resistor = $7.5\ \text{k}\Omega$

R_{FB2} : Output voltage setting resistor = $2.4\ \text{k}\Omega$

C_p : Phase compensation capacitance

R_p : Phase compensation resistance

L : Inductor = $10\ \mu\text{H}$ (SLF10165T-100M3R83PF manufactured by TDK-EPC Corporation or DG8040C-1267AY-100M manufactured by TOKO, INC)

SBD : Schottky barrier diode CRS30I30A (manufactured by Toshiba Co., Ltd.)

C_{BOOT} : Bootstrap capacitor = $0.1\ \mu\text{F}$ (GRM188R71H104J manufactured by Murata Manufacturing Co., Ltd.)

C_{SS} is a capacitor for adjusting the soft-start time.

Examples of Component Values (For Reference Only)

Output Voltage Setting V_{OUT}	Inductance L	Input Capacitance C_{IN}	Output Capacitance C_{OUT}	Feedback Resistor R_{FB1}	Feedback Resistor R_{FB2}	Phase Compensation Capacitance C_p	Phase Compensation Resistance R_p
1.2 V	$6.8\ \mu\text{H}$	$10\ \mu\text{F}$	$44\ \mu\text{F}$	$7.5\ \text{k}\Omega$	$15\ \text{k}\Omega$	4700pF	$10\ \text{k}\Omega$
1.51 V	$6.8\ \mu\text{H}$	$10\ \mu\text{F}$	$44\ \mu\text{F}$	$16\ \text{k}\Omega$	$18\ \text{k}\Omega$	4700pF	$12\ \text{k}\Omega$
1.8 V	$6.8\ \mu\text{H}$	$10\ \mu\text{F}$	$44\ \mu\text{F}$	$15\ \text{k}\Omega$	$12\ \text{k}\Omega$	2200pF	$15\ \text{k}\Omega$
2.5 V	$10\ \mu\text{H}$	$10\ \mu\text{F}$	$44\ \mu\text{F}$	$5.1\ \text{k}\Omega$	$2.4\ \text{k}\Omega$	2200pF	$22\ \text{k}\Omega$
3.3 V	$10\ \mu\text{H}$	$10\ \mu\text{F}$	$44\ \mu\text{F}$	$7.5\ \text{k}\Omega$	$2.4\ \text{k}\Omega$	2200pF	$27\ \text{k}\Omega$
5.0V	$10\ \mu\text{H}$	$10\ \mu\text{F}$	$44\ \mu\text{F}$	$27\ \text{k}\Omega$	$5.1\ \text{k}\Omega$	2200pF	$33\ \text{k}\Omega$

Component values need to be adjusted, depending on the TB7106F's I/O conditions and the board layout.

Application Notes

Inductor Selection

The inductance required for inductor L can be calculated as follows:

$$L = \frac{V_{IN} - V_{OUT}}{f_{OSC} \cdot \Delta I_L} \cdot \frac{V_{OUT}}{V_{IN}} \dots\dots\dots(1)$$

V_{IN}: Input voltage (V)
 V_{OUT}: Output voltage (V)
 f_{OSC}: Oscillation frequency = 380 kHz (typ.)
 ΔI_L: Inductor ripple current (A)

*: Generally, ΔI_L should be set to approximately 30% of the maximum output current. Since the maximum output current of the TB7106F is 3.0 A, ΔI_L should be 0.9 A or so. The inductor should have a current rating greater than the peak output current of 3.5 A. If the inductor current rating is exceeded, the inductor becomes saturated, leading to an unstable DC-DC converter operation.

When V_{IN} = 12 V and V_{OUT} = 3.3 V, the required inductance can be calculated as follows. Be sure to select an appropriate inductor, taking the input voltage range into account.

$$\begin{aligned} L &= \frac{V_{IN} - V_{OUT}}{f_{OSC} \cdot \Delta I_L} \cdot \frac{V_{OUT}}{V_{IN}} \\ &= \frac{12 \text{ V} - 3.3 \text{ V}}{380 \text{ kHz} \cdot 0.9 \text{ A}} \cdot \frac{3.3 \text{ V}}{12 \text{ V}} \\ &= 7.0 \mu\text{H} \end{aligned}$$

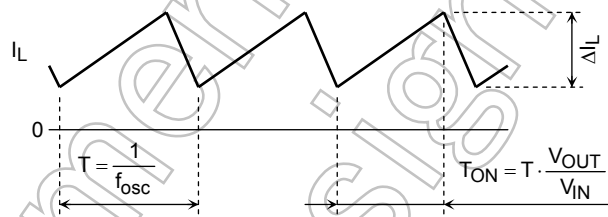


Figure 2 Inductor Current Waveform

Setting the Output Voltage

A resistive voltage divider is connected as shown in Figure 3 to set the output voltage; it is given by Equation 2 based on the reference voltage of the error amplifier (0.8 V typ.), which is connected to the Feedback pin, V_{FB}. R_{FB1} should be up to 30 kΩ or so, because an extremely large-value R_{FB1} incurs a delay due to parasitic capacitance at the V_{FB} pin. It is recommended that resistors with a precision of ±1% or higher be used for R_{FB1} and R_{FB2}.

$$\begin{aligned} V_{OUT} &= V_{FB} \cdot \left(1 + \frac{R_{FB1}}{R_{FB2}} \right) \\ &= 0.8 \text{ V} \cdot \left(1 + \frac{R_{FB1}}{R_{FB2}} \right) \dots\dots\dots(2) \end{aligned}$$

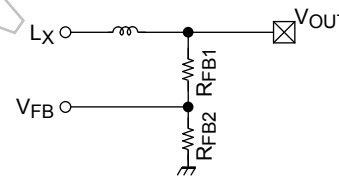


Figure 3 Output Voltage Setting Resistors

Setting the Phase Compensation Circuit

Connect a resistor (R_P) in series with a capacitor (C_P) to COMP pin as a phase compensation. The following calculated value provides an estimation of the constant of phase compensation.

$$\begin{aligned} F_0 &= \frac{1}{2\pi} \cdot \frac{R_{FB2}}{R_{FB1} + R_{FB2}} \cdot G_m(\text{EA}) R_p \cdot \frac{G_m(\text{IS})}{C_{OUT}} \\ F_z &= \frac{1}{2\pi} \cdot \frac{1}{C_p \cdot R_p} \end{aligned}$$

F₀=Frequency in loop gain being 0dB
 : Set approximately to one-tenth of the switching frequency
 F_z=Frequency of pole-zero
 : Set approximately to one-tenth of the F₀
 Design value (reference):
 G_m(EA)=Error Amp G_m : 200(μS)
 G_m(IS)=Current detection circuit G_m : 7(S)

The optimum value of phase compensation may change with the characteristics of C_{OUT} and another.

If it use on the low temperature and the low output voltage conditions, switching waves becomes unstable and the output voltage ripple might increase. At this time, when the value of the output filter capacitor is enlarged, it is likely to be improved. Carry out sufficient evaluation on an actual operating condition.

Output Filter Capacitor Selection

Use a low-ESR electrolytic or ceramic capacitor as the output filter capacitor. Since a capacitor is generally sensitive to temperature, choose one with excellent temperature characteristics. The large capacitance improves load response characteristics. The capacitance should be set to an optimal value that meets the system’s ripple voltage requirement and transient load response characteristics. Since the ceramic capacitor has a very low ESR value, it helps reduce the output ripple voltage; however, because the ceramic capacitor provides less phase margin, it should be thoroughly evaluated.

Rectifier Selection

A Schottky barrier diode should be externally connected to the TB7106F as a rectifier between the Lx and GND pins. It is recommended that either CRS30I30A, be used as the Schottky barrier diode. If a large voltage overshoot is on the Lx pin, it reduces the voltage to connect a series CR network consisting of a resistor of $R_S = 4.7 \Omega$ and a capacitor of $C_S = 470 \text{ pF}$ with the Schottky barrier diode in parallel. Power loss of the Schottky barrier diode tends to increase due to an increased reverse current caused by the rise in ambient temperature and self-heating due to a supplied current. The rated current should therefore be derated to allow for such conditions in selecting an appropriate diode.

Soft-Start Feature

The TB7106F has a soft-start feature.

If the SS pin is left open, the soft-start time, t_{SS} , for V_{OUT} defaults to 1 ms (typ.) internally.

The soft-start time can be extended by adding an external capacitor (C_{SS}) between the SS and GND pins. The soft-start time can be calculated as follows:

$$t_{SS2} = 0.16 \cdot C_{SS} \dots\dots\dots(3)$$

t_{SS2} : Soft-start time (in seconds) when an external capacitor is connected between SS and GND.
 C_{SS} : Capacitor value (μF)

The soft-start feature is activated when the TB7106F exits the undervoltage lockout (UVLO) state after power-up and when the voltage at the EN pin has changed from logic low to logic high.

Overcurrent Protection (OCP)

The TB7106F has built-in maximum current limiting with pulse skip. When the peak current of Lx pin exceeds $I_{LIM}=4.5\text{A}(\text{typ.}) @V_{IN} = 12\text{V}$, the ON time of the high-side switch(internal) will be limited. Switching frequency will be reduced and output current will be restricted further if output voltage falls and the voltage of VFB pin drops below the overcurrent pulse skip detection voltage V_{LOC} (0.3V typ.) during overcurrent protection . When $V_{IN} \geq 6.5\text{V}$, The TB7106F can operate at $I_{OUT} = 3.0\text{A}(\text{max})$. Meanwhile, use it at $I_{OUT} = 2.5\text{A}(\text{max})$ when $V_{IN} < 6.5\text{V}$.

Undervoltage Lockout (UVLO)

The TB7106F has undervoltage lockout (UVLO) protection circuitry. The TB7106F does not provide output voltage (V_{OUT}) until the input voltage has reached V_{UVR} (3.5 V typ.). UVLO has hysteresis of 0.3 V (typ.). After the switch turns on, if V_{IN} drops below V_{UV} (3.2 V typ.), UVLO shuts off the switch at V_{OUT} .

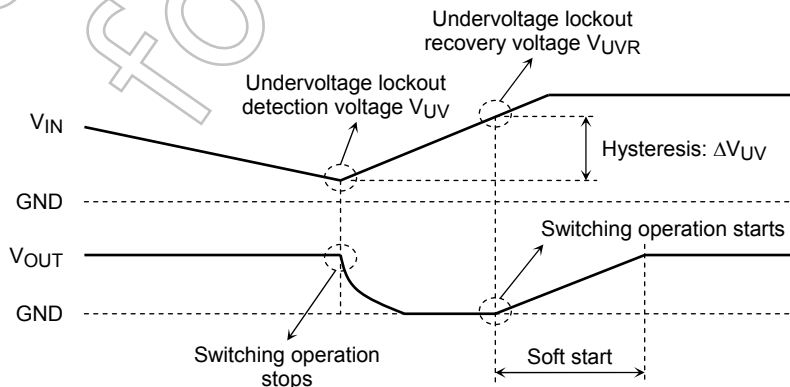


Figure 4 Undervoltage Lockout Operation

Thermal Shutdown (TSD)

The TB7106F provides thermal shutdown. When the junction temperature continues to rise and reaches TSD (160°C typ.), the TB7106F goes into thermal shutdown and shuts off the power supply. TSD has a hysteresis of about 15°C (typ.). The device is enabled again when the junction temperature has dropped by approximately 15°C from the TSD trip point. The device resumes the power supply when the soft-start circuit is activated upon recovery from TSD state.

Thermal shutdown is intended to protect the device against abnormal system conditions. It should be ensured that the TSD circuit will not be activated during normal operation of the system.

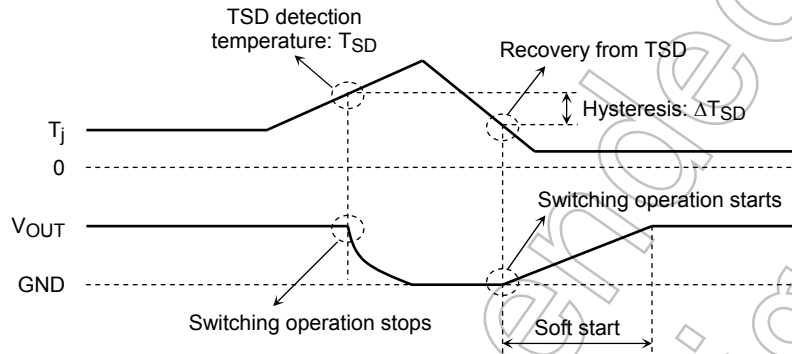


Figure 5 Thermal Shutdown Operation

Area of Safety Operation

The TB7106F limits the output current according to the duty cycle of the high side switch. I_{OUT} in the area of safety operation is a mean value of direct current. Please note that it might cause the decrease in the output voltage and the decrease in the reliability of the product when this product is used on the condition to exceed the area of safety operation (Figure 6).

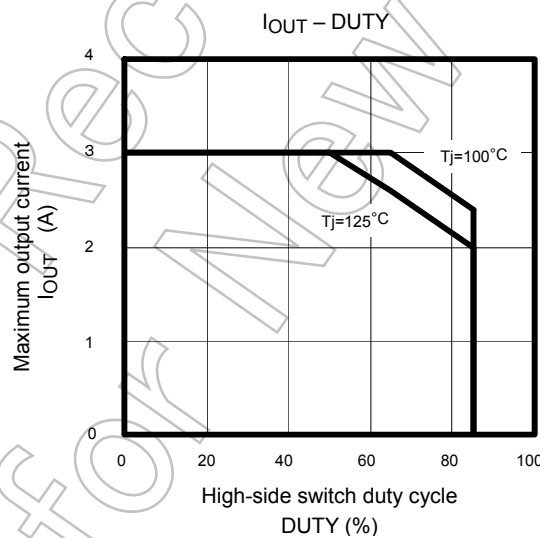


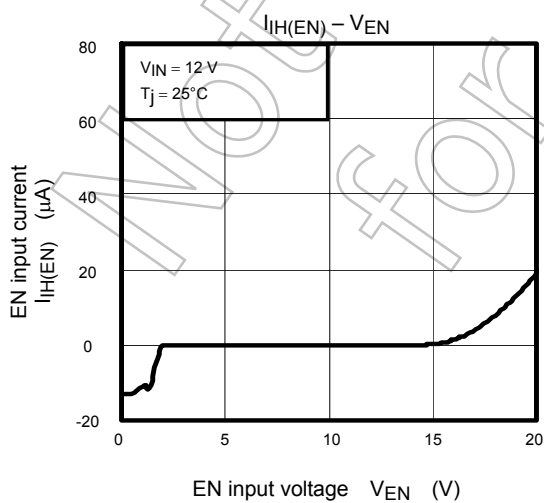
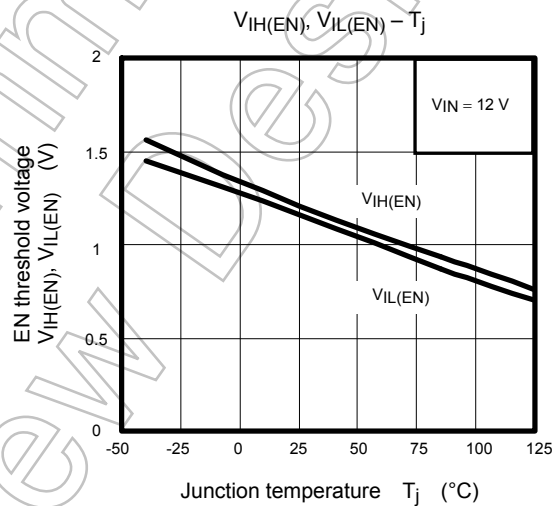
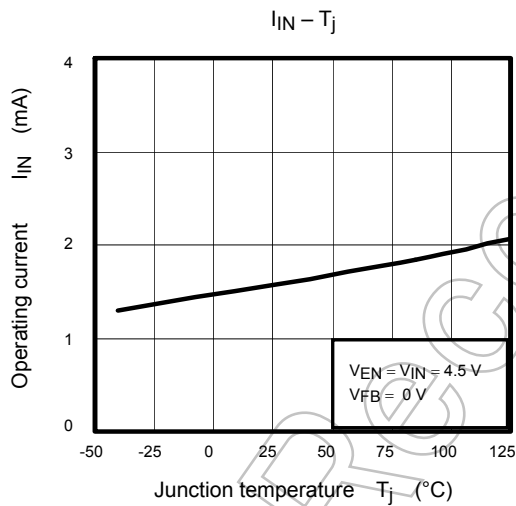
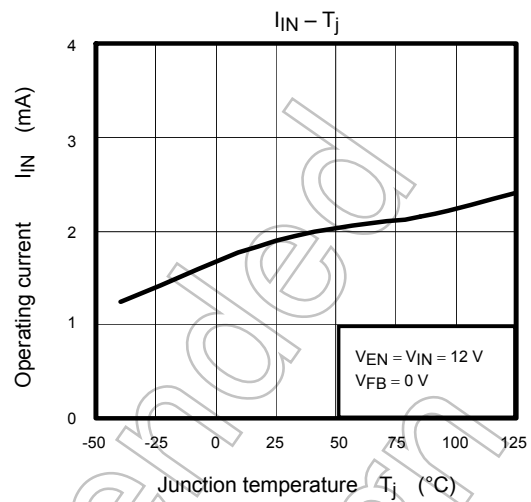
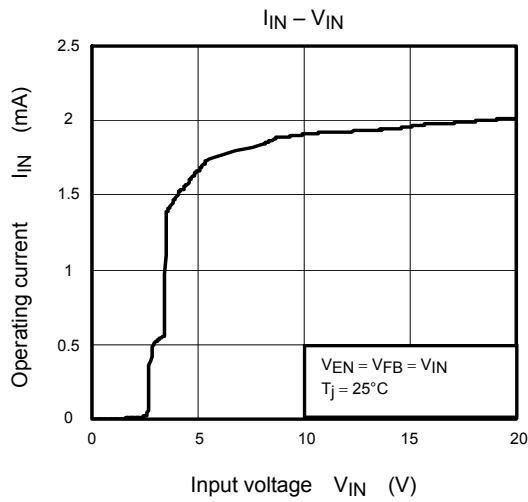
Figure 6 Area of Safety Operation

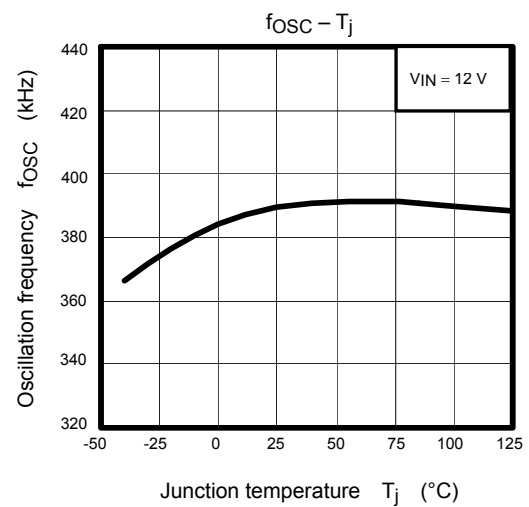
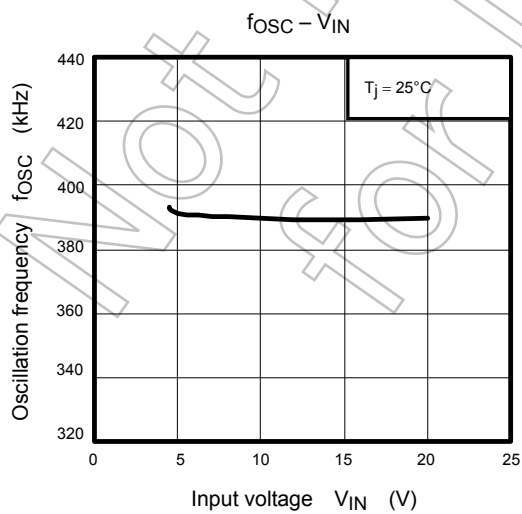
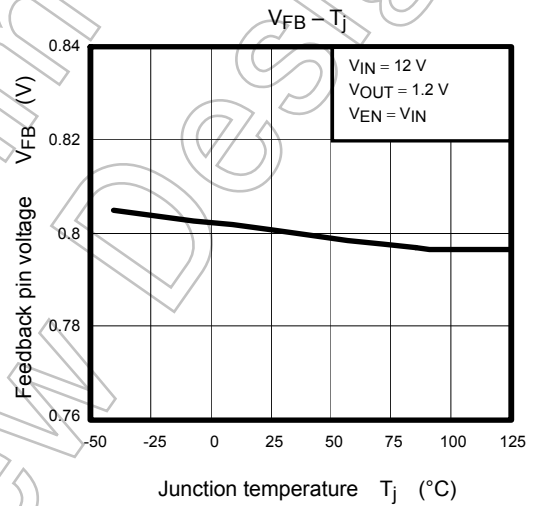
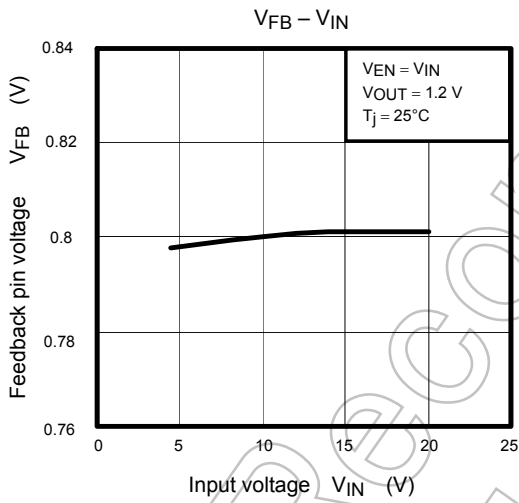
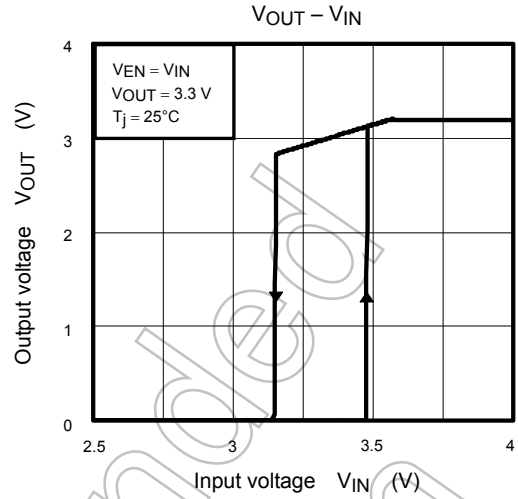
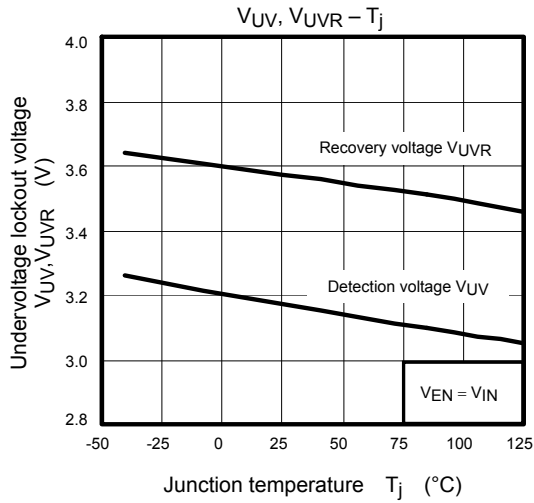
Usage Precautions

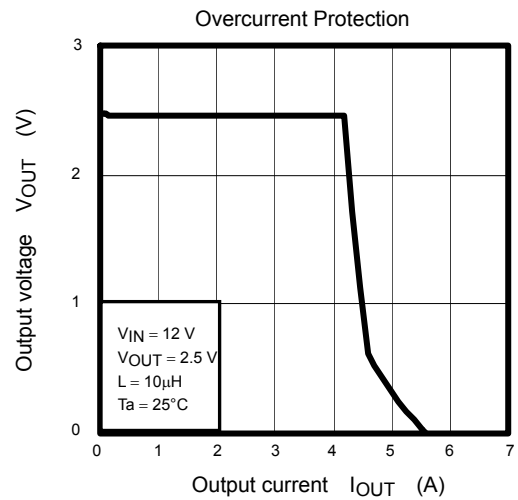
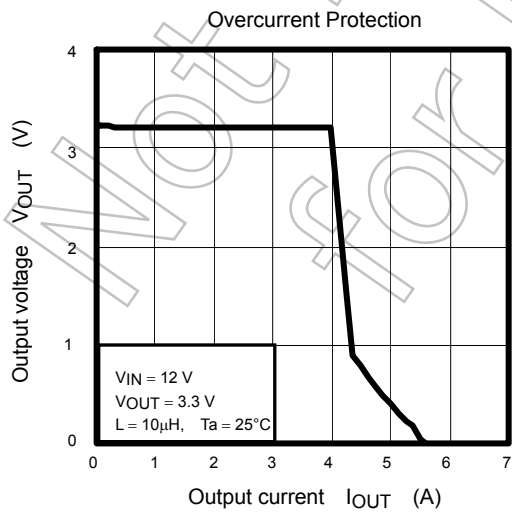
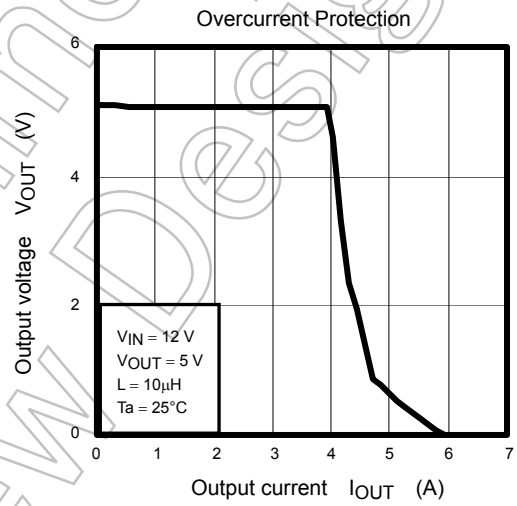
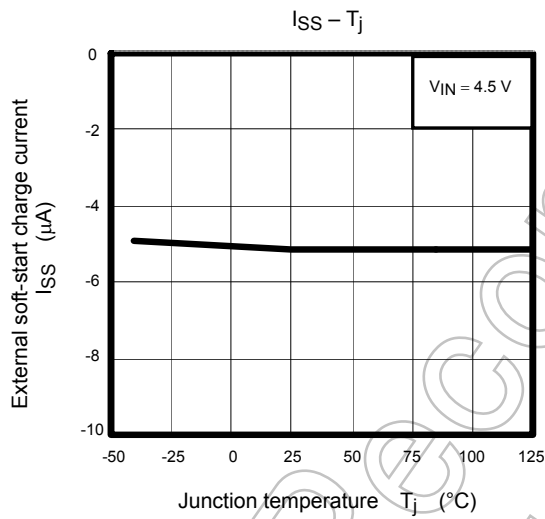
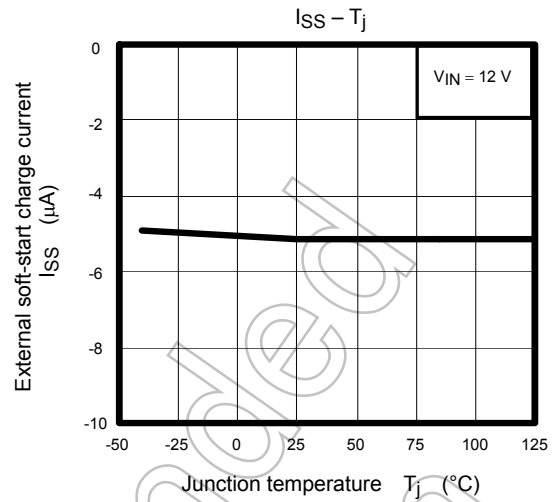
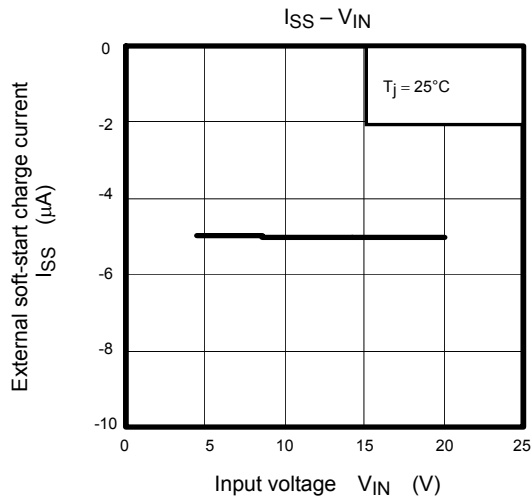
- The input voltage, output voltage, output current and temperature conditions should be considered when selecting capacitors, inductors and resistors. These components should be evaluated on an actual system prototype for best selection.
- Parts of this product in the surrounding are examples of the representative, and the supply might become impossible. Please confirm latest information when using it.
- External components such as capacitors, inductors and resistors should be placed as close to the TB7106F as possible.
- C_{IN} should be connected as close to the GND and V_{IN} pins as possible. Operation might become unstable due to board layout.
- The minimum programmable output voltage is 0.8 V (typ.). If the difference between the input and output voltages is small, the output voltage might not be regulated accurately and fluctuate significantly.
- GND pin is connected with the back of IC chip and serves as the heat radiation pin. Secure the area of a GND pattern as large as possible for greater of heat radiation.
- The overcurrent protection circuits in the Product are designed to temporarily protect Product from minor overcurrent of brief duration. When the overcurrent protective function in the Product activates, immediately cease application of overcurrent to Product. Improper usage of Product, such as application of current to Product exceeding the absolute maximum ratings, could cause the overcurrent protection circuit not to operate properly and/or damage Product permanently even before the protection circuit starts to operate.
- The thermal shutdown circuits in the Product are designed to temporarily protect Product from minor overheating of brief duration. When the overheating protective function in the Product activates, immediately correct the overheating situation. Improper usage of Product, such as the application of heat to Product exceeding the absolute maximum ratings, could cause the overheating protection circuit not to operate properly and/or damage Product permanently even before the protection circuit starts to operate.

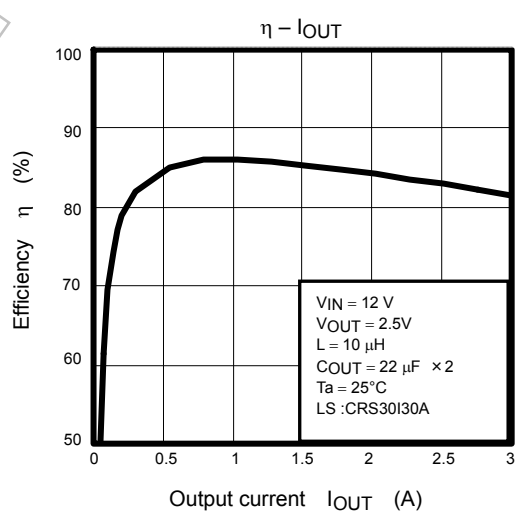
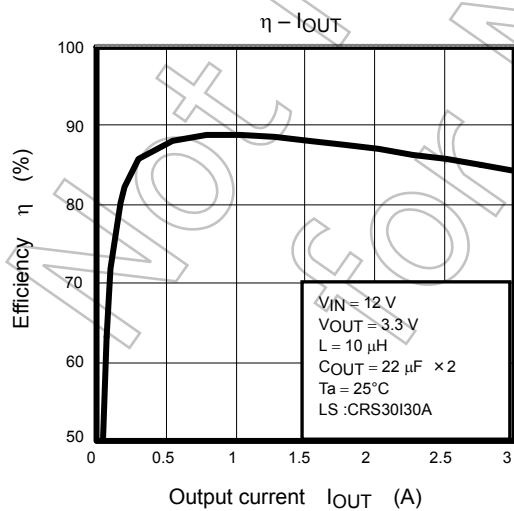
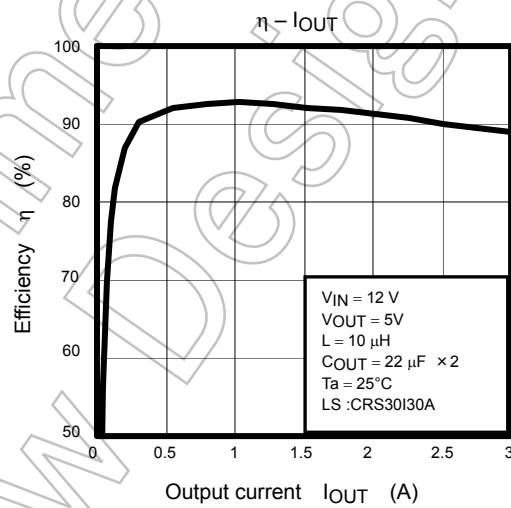
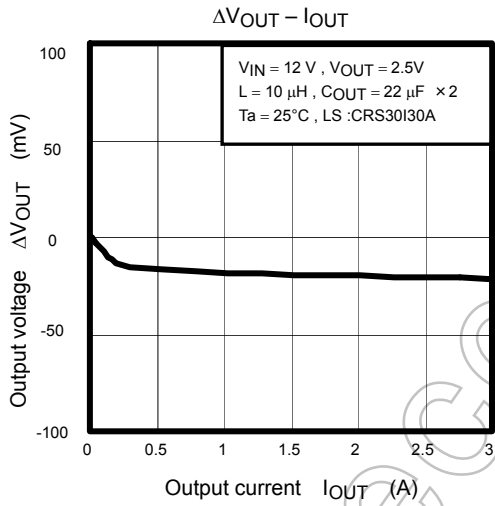
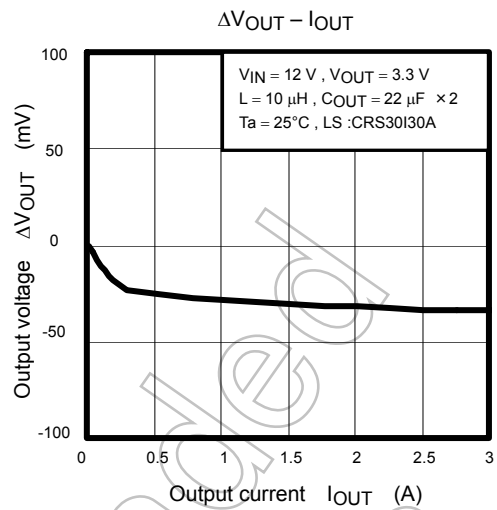
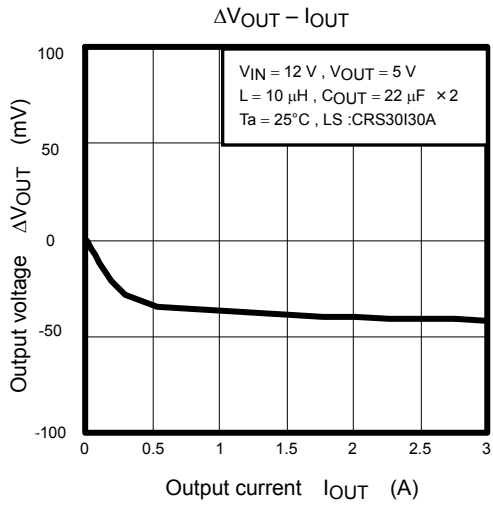
Not Recommended
for New Design

Typical Performance Characteristics

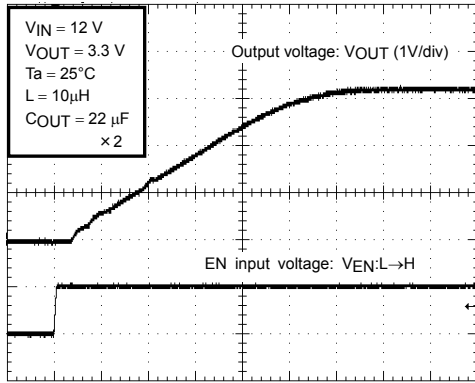






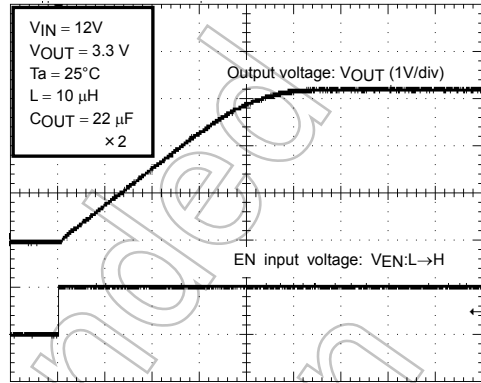


Startup Characteristics
(Internal Soft-Start Time)



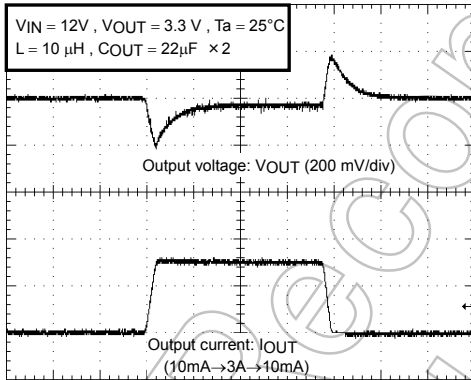
200 $\mu\text{s/div}$

Startup Characteristics
($C_{SS} = 0.1\ \mu\text{F}$)



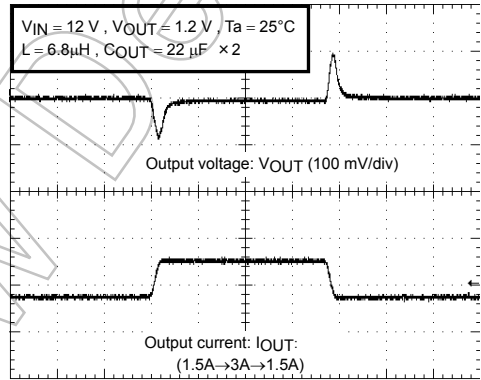
4 ms/div

Load Response Characteristics



200 $\mu\text{s/div}$

Load Response Characteristics



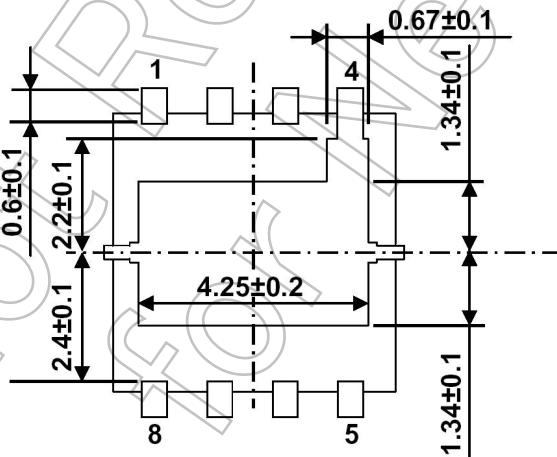
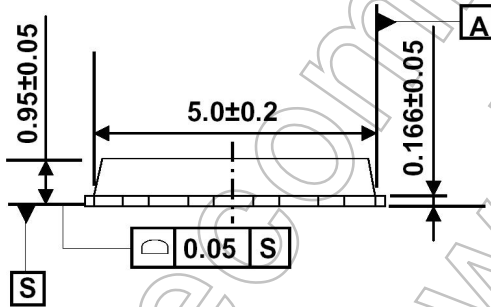
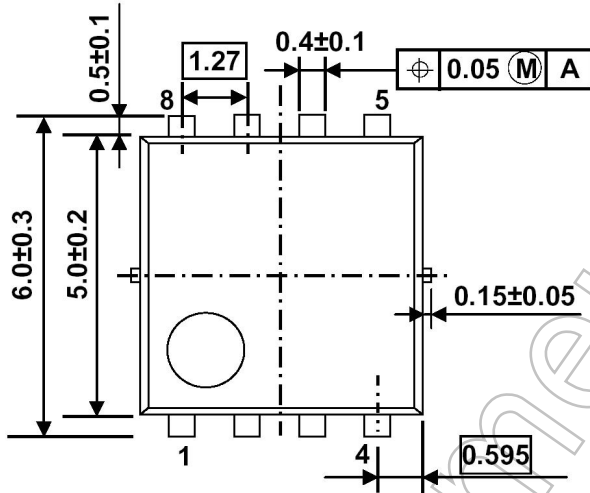
200 $\mu\text{s/div}$

Not for New Design

Package Dimensions

HS0N8-P-0505-1.27

Unit: mm



Weight: 0.068 g (typ.)

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