Toshiba BiCMOS Linear Integrated Circuits — silicon monolithic

TB9083FTG

Automotive GATE-driver for Brushless motor

1. INTRODUCTION

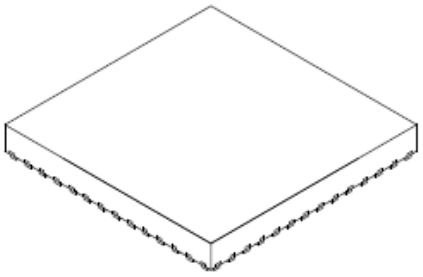
The TB9083FTG is a pre-driver IC for brushless motors in vehicle application.

It features a built-in safety relay pre-driver in addition to the three-phase pre-driver.

It also has a charge pump, a motor current detector circuit, an oscillator circuits and an SPI communication circuit.

It has multiple error detection features. Trigger threshold, response action and other settings are modified via the SPI.

The TB9083FTG is also equipped with ABIST/LBIST for testing and evaluation of the error detection functions.



P-VQFN48-0707-0.50-005

weight: 137.9 mg (typ.)

2. APPLICATIONS

Used mainly on EPS, powered brakes and pumps

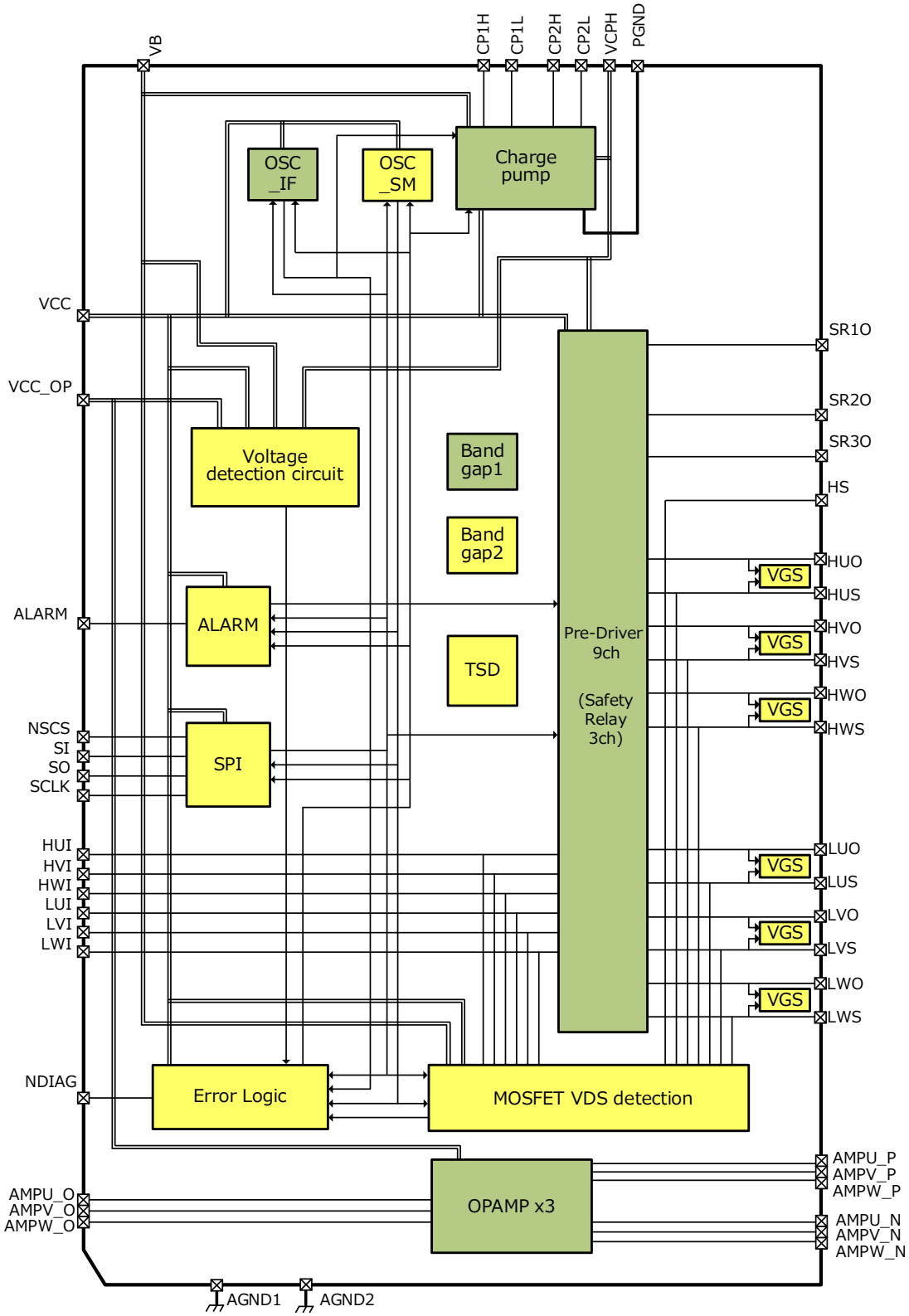
3. FEATURES AND BENEFITS

- Three-phase pre-driver PWM control up to 20 kHz
- Fail-safe relay pre-driver
- Built-in charge pump circuit
- Built-in current detector circuit
- Error detection functionality: undervoltage (VB, VCC, VCC_OP), overvoltage (VCC, VCC_OP, VCPH, external MOSFET VGS), overtemperature, external MOSFET VDS detector
- Built-in ABIST / LBIST
- AEC-Q100 and AEC-Q006 Qualified
- Operating voltage range VB: 4.5 to 28 V, VCC: 3.0 to 5.5 V
- Operating temperature range Ta: -40°C to 150°C, Tj: -40°C to 175°C
- Package P-VQFN48-0707-0.50-005 (Wettable flank, 0.5 mm pitch)
- Functional safety
  - Developed according to ISO 26262 2nd Ed. ASIL-D Capable.
  - Safety manual and safety evaluation report
  - Redundancy and built-in ABIST/LBIST
  - SPI interface with CRC check

The product(s) is/are compatible with RoHS regulations (EU directive 2011 / 65 / EU) as indicated, if any, on the packaging label ("[[G]]/RoHS COMPATIBLE", "[[G]]/RoHS [[Chemical symbol(s) of controlled substance(s)]]", "RoHS COMPATIBLE" or "RoHS COMPATIBLE, [[Chemical symbol(s) of controlled substance(s)]]>MCV").

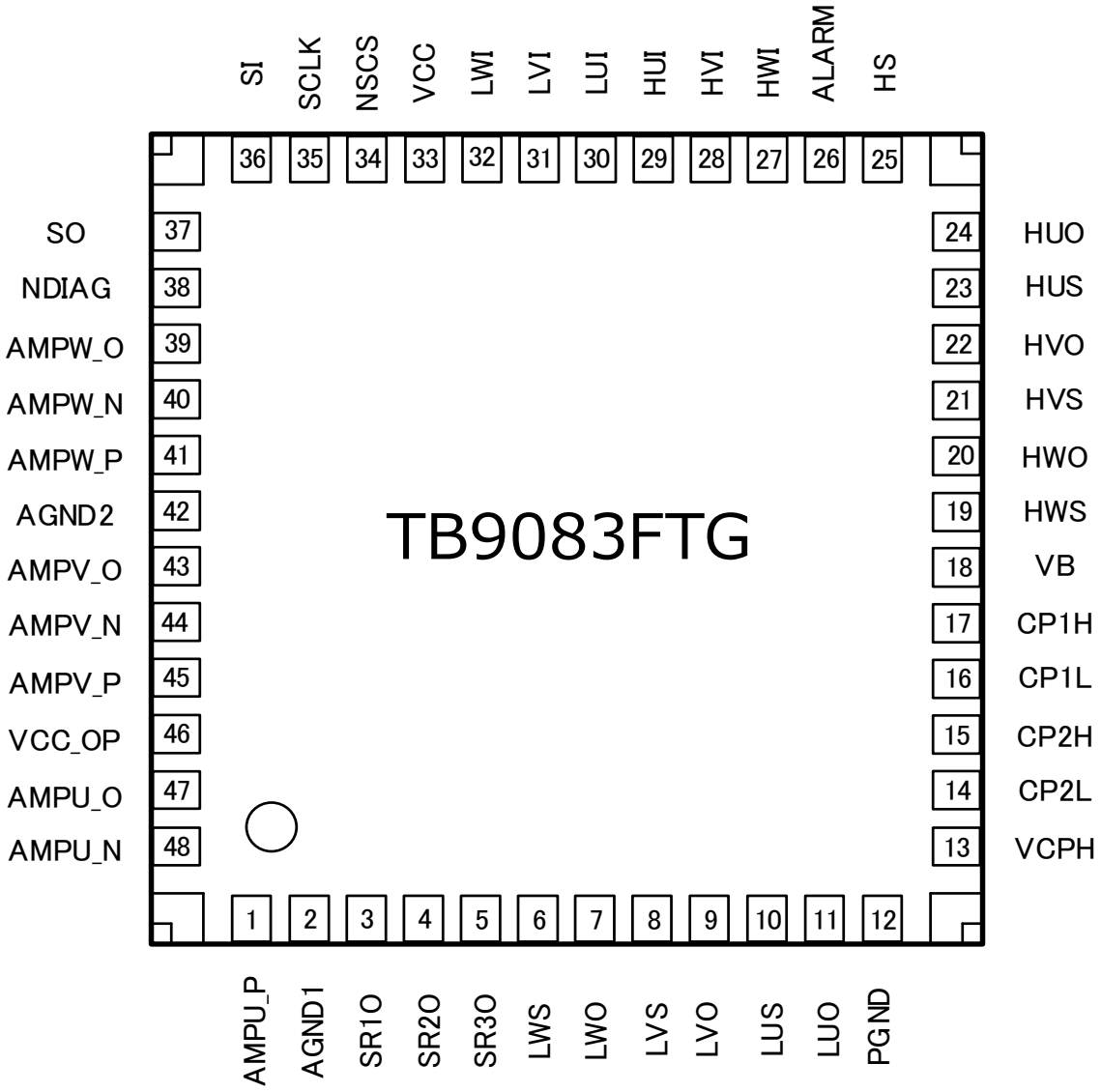
Start of commercial production
2022-11

4. BLOCK DIAGRAM



Note Functional blocks and wiring scheme have been simplified for the purpose of clarity (including individual block diagrams)

5. Terminal layout (top view)



6. Terminals

Pin No	Name	I/O	Description	Pull-up/down resistor	Remark
1	AMPU_P	IN	Current sense amplifier positive input for U phase	–	–
2	AGND1	GND	GND 1 for analog circuits	–	–
3	SR1O	OUT	Safety relay 1 output	–	SPI setting
4	SR2O	OUT	Safety relay 2 output	–	SPI setting
5	SR3O	OUT	Safety relay 3 output	–	SPI setting
6	LWS	IN	Pre-driver reference input for W phase low side (source)	–	–
7	LWO	OUT	Pre-driver output for W phase low side	Pull-down to LWS	–
8	LVS	IN	Pre-driver reference input for V phase low side (source)	–	–
9	LVO	OUT	Pre-driver output for V phase low side	Pull-down to LVS	–
10	LUS	IN	Pre-driver reference input for U phase low side (source)	–	–
11	LUO	OUT	Pre-driver output for U phase low side	Pull-down to LUS	–
12	PGND	GND	Power GND	–	–
13	VCPH	Power supply	Charge pump output voltage	Pull-down to VB	–
14	CP2L	OUT	Charge pump output 2	–	–
15	CP2H	I/O	Charge pump drive output 2	–	–
16	CP1L	OUT	Charge pump output 1	–	–
17	CP1H	I/O	Charge pump drive output 1	–	–
18	VB	Power supply	VB input	–	–
19	HWS	IN	Pre-driver reference input for W phase high side (source)	Pull-up to HS Pull-down to LWS	Pull-up and pull-down resistors can be connected only in the external FET test mode (FET_TEST).
20	HWO	OUT	Pre-driver output for W phase high side	Pull-down to HWS	-
21	HVS	IN	Pre-driver reference input for V phase high side (source)	Pull-up to HS Pull-down to LVS	Pull-up and pull-down resistors can be connected only in the external FET test mode (FET_TEST).
22	HVO	OUT	Pre-driver output for V phase high side	Pull-down to LVS	–
23	HUS	IN	Pre-driver reference input for U phase high side (source)	Pull-up to HS Pull-down to LUS	Pull-up and pull-down resistors can be connected only in the external FET test mode (FET_TEST).
24	HUO	OUT	Pre-driver output for U phase high side	Pull-down to HUS	–
25	HS	IN	VDS sense input for external high side MOSFET	–	–
26	ALARM	IN	Enable input for pre-driver	Pull-down to GND	–
27	HWI	IN	Pre-driver input for W phase high side	Pull-down to GND	–
28	HVI	IN	Pre-driver input for V phase high side	Pull-down to GND	–
29	HUI	IN	Pre-driver input for U phase high side	Pull-down to GND	–
30	LUI	IN	Pre-driver input for U phase low side	Pull-down to GND	–
31	LVI	IN	Pre-driver input for V phase low side	Pull-down to GND	–
32	LWI	IN	Pre-driver input for W phase low side	Pull-down to GND	–
33	VCC	Power supply	5V/3.3V supply input	–	–
34	NSCS	IN	SPI chip select	Pull-up to VCC	–
35	SCLK	IN	SPI clock input	Pull-down to GND	–
36	SI	IN	SPI input	Pull-down to GND	–
37	SO	OUT	SPI output	–	–
38	NDIAG	OUT	Diagnosis output	–	–
39	AMPW_O	OUT	Current sense amplifier output for W phase	–	–
40	AMPW_N	IN	Current sense amplifier negative input for W phase	–	–
41	AMPW_P	IN	Current sense amplifier positive input for W phase	–	–
42	AGND2	GND	GND 2 for analog circuits	–	–
43	AMPV_O	OUT	Current sense amplifier output for V phase	–	–
44	AMPV_N	IN	Current sense amplifier negative input for V phase	–	–
45	AMPV_P	IN	Current sense amplifier positive input for V phase	–	–
46	VCC_OP	Power supply	5V/3.3V supply input for current sense amplifiers	–	–
47	AMPU_O	OUT	Current sense amplifier output for U phase	–	–
48	AMPU_N	IN	Current sense amplifier negative input for U phase	–	–

● Internal signals

Internal Signal	Description	State	
		H	L
(abst_pass)	ABIST normal signal	ABIST normal	ABIST abnormal
(abst_end)	ABIST end signal	ABIST completed	ABIST incomplete
(gate_en_u)	Pre-driver output enabling signal for U Phase	Enable	Disable
(gate_en_v)	Pre-driver output enabling signal for V Phase	Enable	Disable
(gate_en_w)	Pre-driver output enabling signal for W Phase	Enable	Disable
(gate_en_r)	Pre-driver output enabling signal for safety relay	Enable	Disable
(gate_off_u)	Pre-driver off signal other than ALARM factor for U Phase.	–	–
(gate_off_v)	Pre-driver off signal other than ALARM factor for V Phase.	–	–
(gate_off_w)	Pre-driver off signal other than ALARM factor for W Phase.	–	–
(gate_off_r)	Relay off signal other than ALARM factor.	–	–
(cp_en)	Charge pump enable signal	Enable	Disable
(cp_off)	Charge pump off signal	–	–
(vbl)	VB under voltage detection signal	Detection	Release
(vcphh)	VCPH overvoltage detection signal	Detection	Release
(vcl1)	VCC undervoltage detection signal 1	Detection	Release
(vcl2)	VCC undervoltage detection signal 2	Detection	Release
(por_x)	Internal reset signal	Reset release	Reset
(vccopl)	VCC_OP undervoltage detection signal	Detection	Release
(vccoph)	VCC_OP overvoltage detection signal	Detection	Release
(vch)	VCC overvoltage detection signal	Detection	Release
(tsddet)	Thermal shutdown detection signal	Detection	Release
(clk4m_if)	4MHz clock (oscillation for IF)	–	–
(clk4m_sm)	4MHz clock (oscillation for SM)	–	–
(vdsuho)	External MOSFET Vds detection signal for U phase low side	Detection	Release
(vdsvho)	External MOSFET Vds detection signal for V phase low side	Detection	Release
(vdswho)	External MOSFET Vds detection signal for W phase low side	Detection	Release
(vdsulo)	External MOSFET Vds detection signal for U phase high side	Detection	Release
(vdsvlo)	External MOSFET Vds detection signal for V phase high side	Detection	Release
(vdswlo)	External MOSFET Vds detection signal for W phase high side	Detection	Release

Power/ground terminals

Symbol	Pin Name	Description
Vb	VB	Battery power supply input
Vcc	VCC	5V/3.3V supply input
Vccop	VCC_OP	5V/3.3V supply input for current sense amplifier
Vcph	VCPH	Charge pump voltage (high side)
AGND	AGND1,AGND2	GND for analog circuits
PGND	PGND	Power GND

7. FUNCTIONS AND FEATURES

7.1. Charge pump circuit

If Vcph for the pre-driver charge pump that drives the external MOSFET reaches Vb + 14 V (Typ.), the charge pump will be shut down by the internal circuit controller.

The switching circuit (CP_SW) on the Vb side of the charge pump can switch the transistor off and shut off the supply from Vb to Vcph. When CP_SW switches the transistor off, the charge pump stops and the VCPH terminal output voltage becomes Vb. CP_SW also switches the transistor off when the VCC voltage falls below the VCC undervoltage detection threshold. It is also possible to make CP_SW switch the transistor off via the SPI. Meanwhile, the CP_CL current limiter circuit monitors current on the VB to VCPH supply line to prevent excess current.

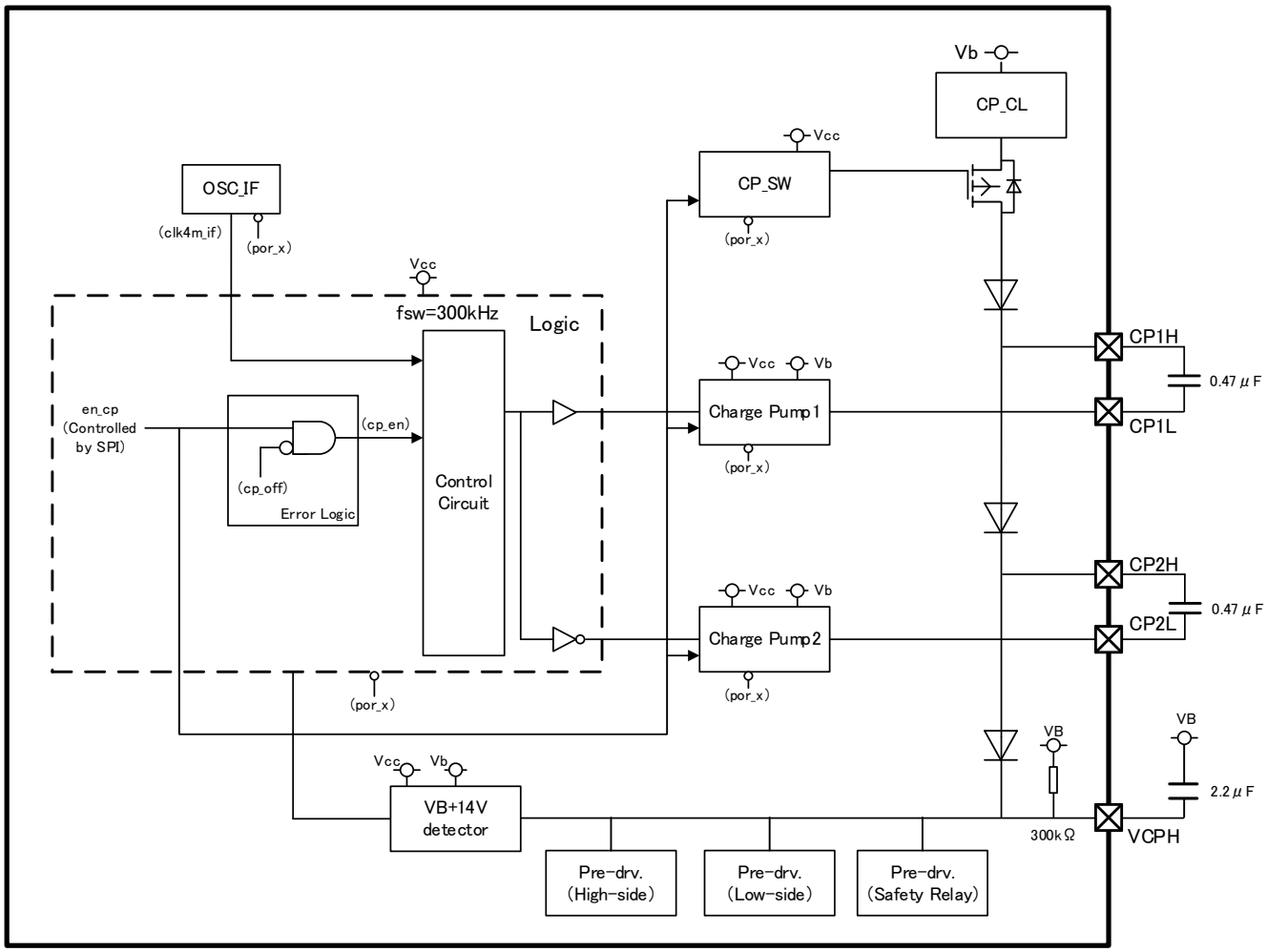


Fig. 7.1-a Block diagram for charge pump circuit

7.2. Pre-driver circuit

The pre-driver circuit consists of pre-drivers for high side, low side and power/motor safety relay drives.

High side and low side pre-drivers have separate input and output terminals and are controlled by signal at the input terminals.

The safety relay pre-driver is controlled by the CP_RLY_CTRL register. It has a built-in 500 Ω resistor and backflow prevention diode for reverse connection (see Figure 7.2-c). When a pull-down resistor is connected to the motor relay, there may be a voltage differential with the gate voltage. There is no restriction on external series resistance if safety relay outputs SR1O, SR2O and/or SR3O are incorporated into the power supply relay.

A resistor for maintaining the HUS, HVS and HWS terminals at the median voltage is used only when performing an initial diagnosis as described in Section 7.8.

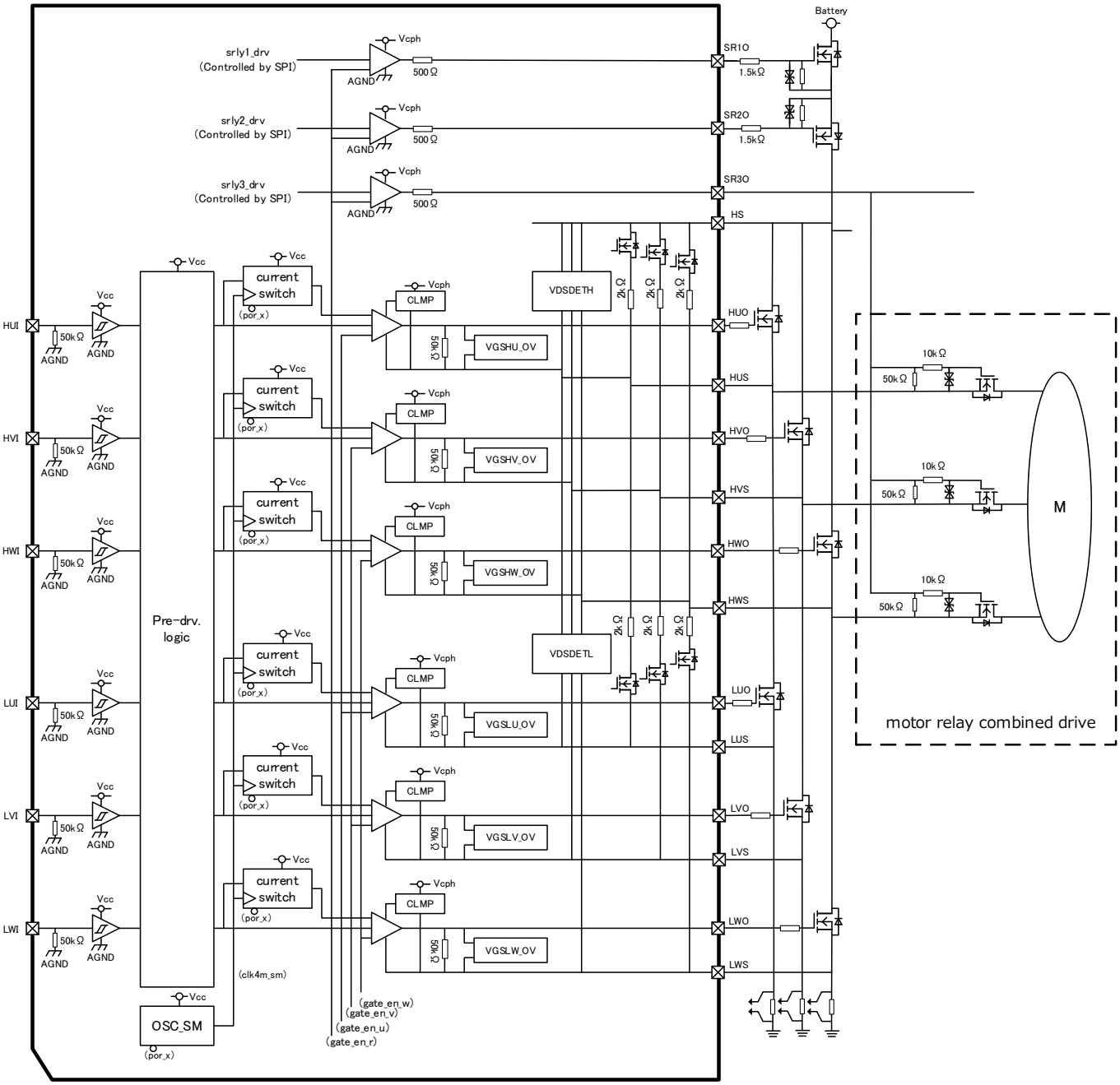


Fig. 7.2-a Block diagram for pre-driver circuit (motor relay combined drive)

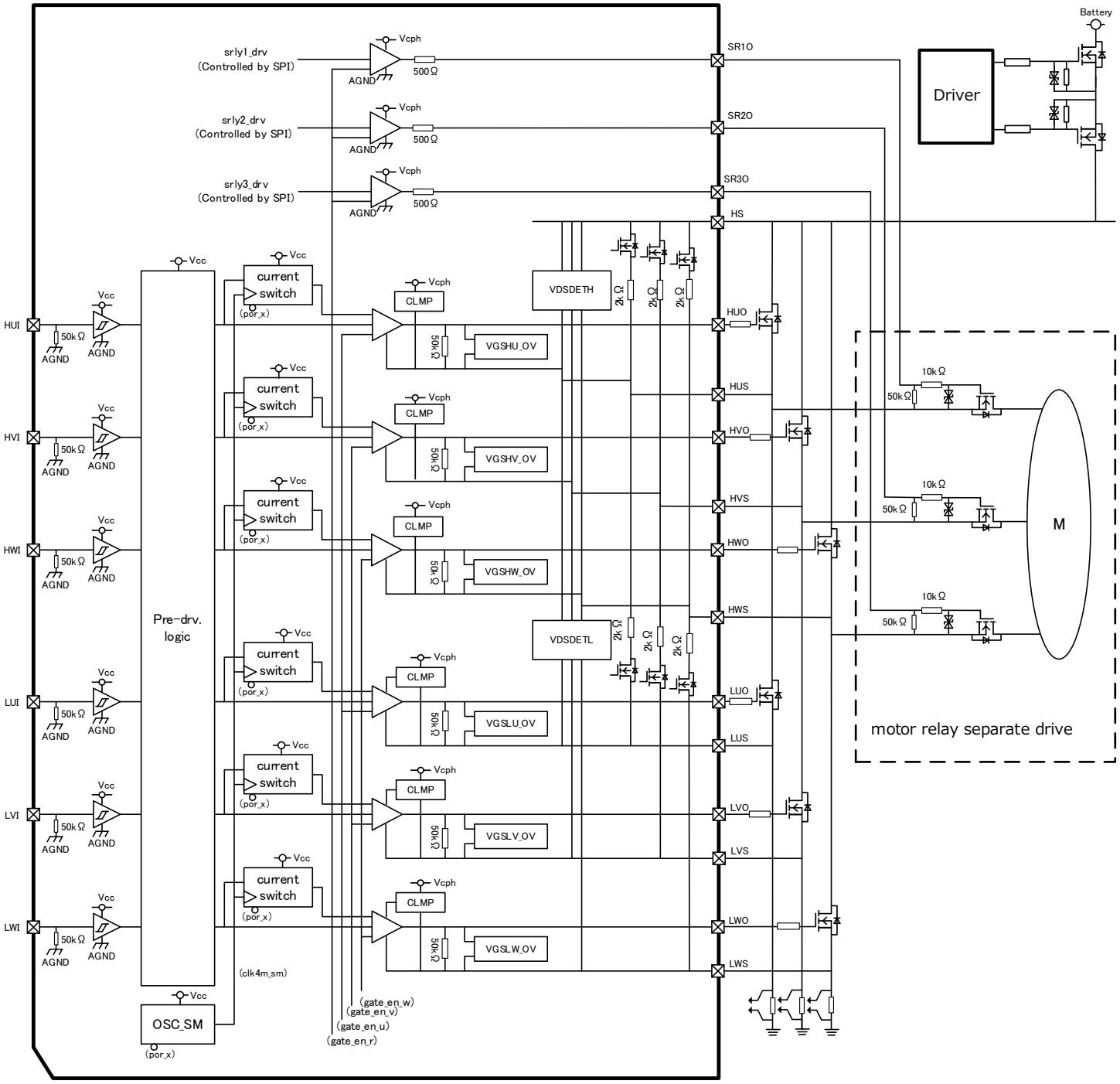


Fig. 7.2-b Block diagram for pre-driver circuit (motor relay separate drive)

Safety relay (power/motor relay) driver

The safety relay driver controls the power or motor relay. The safety relay pre-driver circuit is controlled via the CP_RLY_CTRL register. It has a built-in 500 Ω resistor and backflow prevention diode for reverse connection (see Figure 7.2-c).

Table 7.2-a shows the truth table. Refer to Section 7.6 for details of internal signals (gate_en_r) listed in the truth table.

Table 7.2-a I/O truth table for safety relay driver

・ Power/motor relay driver 1 (SR1O)

Internal Signal (gate_en_r)	Input (SPI) Register srly1_drv	Output SR1O	Remark
"L"	*	"L"	—
"H"	"0"	"L"	—
	"1"	"H"	—

・Power/motor relay driver 2 (SR2O)

Internal Signal (gate_en_r)	Input (SPI) Register srly2_drv	Output SR2O	Remark
"L"	*	"L"	—
"H"	"0"	"L"	—
	"1"	"H"	—

・Power/motor relay driver 3 (SR3O)

Internal Signal (gate_en_r)	Input (SPI) Register srly3_drv	Output SR3O	Remark
"L"	*	"L"	—
"H"	"0"	"L"	—
	"1"	"H"	—

*:Don't care

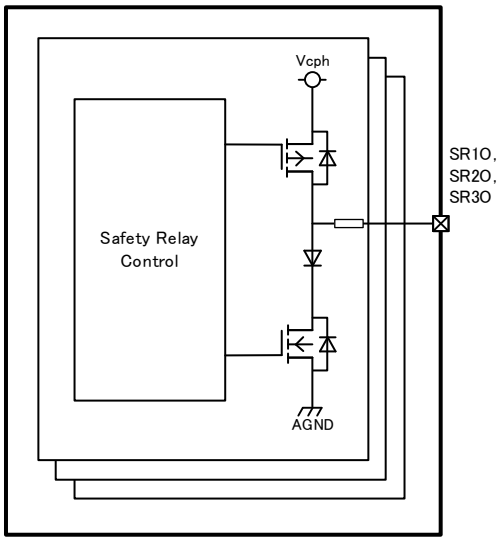


Fig. 7.2-c Block diagram for safety relay circuit

High side and low side drivers

The high side driver drives the MOSFET on the high side, while the low side driver drives the MOSFET on the low side. The high and low side drives both have three built-in channels. Input signal (HUI/HVI/HWI, LUI/LVI/LWI) is converted to output signal (HUO/HVO/HWO, LUO/LVO/LWO) by the control block.

➢ Current limiter

Depending on the t_ilim setting in the T_ILIM register, the high-side and / or low-side driver can limit the current(Io_lmth/ Io_lmtl) after a certain period from the on / off drive transition point. A register value of t_ilim="11" denotes no current limiting (the preset constant current); t_ilim = "00" to "10" applies current limiting for the specified period.

➢ Inhibited input

Table 7.2-b shows the truth table, using U phase as an example. The action for HUI=LUI="H" when the pre-driver is enabled (gate_en_u="H") can be selected via the PL_CTRL register. Input prohibit mode is engaged when the plu_dis bit is "L," and the output is HUO=LUO="L." At this time, pl_op can be used to specify whether the status register is set to "H." When pl_op is "H," err_pl_u is set to "H." When pl_op is "L," err_pl_u is not set to "H." The DIAG terminal follows the status register. When plu_dis is "H," the prohibited input detector itself is disabled and HUO=LUO="H" output is possible. Refer to Section 7.6 for details of internal signals listed in the truth table (gate_en_u, gate_en_v, gate_en_w).

Table 7.2-b I/O truth table (high side and low side drivers)

・MOSFET driver 1 (U phase)

Internal Signal	Input		Register		Output		status	Remark
(gate_en_u)	HUI	LUI	plu_dis	pl_op	HUO	LUO	err_pl_u	
"L"	"L"	*	*	*	"L"	"L"	—	—
	*	"L"	*	*			—	—
	"H"	"H"	"L"	"L"			—	Inhibit input mode without status
			"L"	"H"			"set"	Inhibit input mode with status
			"H"	*			—	Inhibit input mode disabled (U phase)
"H"	"L"	"L"	*	*	"L"	"L"	—	—
	"L"	"H"	*	*	"L"	"H"	—	—
	"H"	"L"	*	*	"H"	"L"	—	—
	"H"	"H"	"L"	"L"	"L"	"L"	—	Inhibit input mode without status
			"L"	"H"	"L"	"L"	"set"	Inhibit input mode with status
			"H"	*	"H"	"H"	—	Inhibit input mode disabled (U phase)

・MOSFET driver 2 (V phase)

Internal Signal	Input		Register		Output		status	Remark
(gate_en_v)	HVI	LVI	plv_dis	pl_op	HVO	LVO	err_pl_v	
"L"	"L"	*	*	*	"L"	"L"	—	—
	*	"L"	*	*			—	—
	"H"	"H"	"L"	"L"			—	Inhibit input mode without status
			"L"	"H"			"set"	Inhibit input mode with status
			"H"	*			—	Inhibit input mode disabled (V phase)
"H"	"L"	"L"	*	*	"L"	"L"	—	—
	"L"	"H"	*	*	"L"	"H"	—	—
	"H"	"L"	*	*	"H"	"L"	—	—
	"H"	"H"	"L"	"L"	"L"	"L"	—	Inhibit input mode without status
			"L"	"H"	"L"	"L"	"set"	Inhibit input mode with status
			"H"	*	"H"	"H"	—	Inhibit input mode disabled (V phase)

・MOSFET driver 3 (W phase)

Internal Signal	Input		Register		Output		status	Remark
(gate_en_w)	HWI	LWI	plw_dis	pl_op	HWO	LWO	err_pl_w	
"L"	"L"	*	*	*	"L"	"L"	—	—
	*	"L"	*	*			—	—
	"H"	"H"	"L"	"L"			—	Inhibit input mode without status
			"L"	"H"			"set"	Inhibit input mode with status
			"H"	*			—	Inhibit input mode disabled (W phase)
"H"	"L"	"L"	*	*	"L"	"L"	—	—
	"L"	"H"	*	*	"L"	"H"	—	—
	"H"	"L"	*	*	"H"	"L"	—	—
	"H"	"H"	"L"	"L"	"L"	"L"	—	Inhibit input mode without status
			"L"	"H"	"L"	"L"	"set"	Inhibit input mode with status
			"H"	*	"H"	"H"	—	Inhibit input mode disabled (W phase)

*:Don’t care

Note: DIAG terminals are linked to status. Use the err_pl_*_cl bit to clear the status.

7.3. Current detector circuit

7.3.1. Circuit structure

The current detector circuit has three motor current detector amps and a reference voltage generator amp (see Figures 7.3-a and 7.3-b). The motor current detector amps can amplify the difference voltage attributable to current in the shunt resistor connected to the motor drive. The reference voltage generator amp serves as a reference voltage generator buffer amp. The external composition of the current detector can be single or triple shunt.

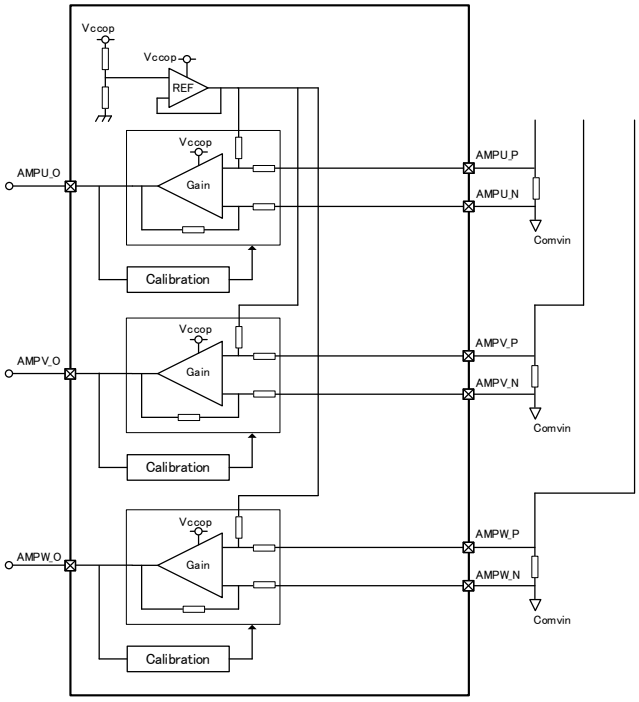


Fig. 7.3-a Block diagram for motor current detector circuit (triple shunt)

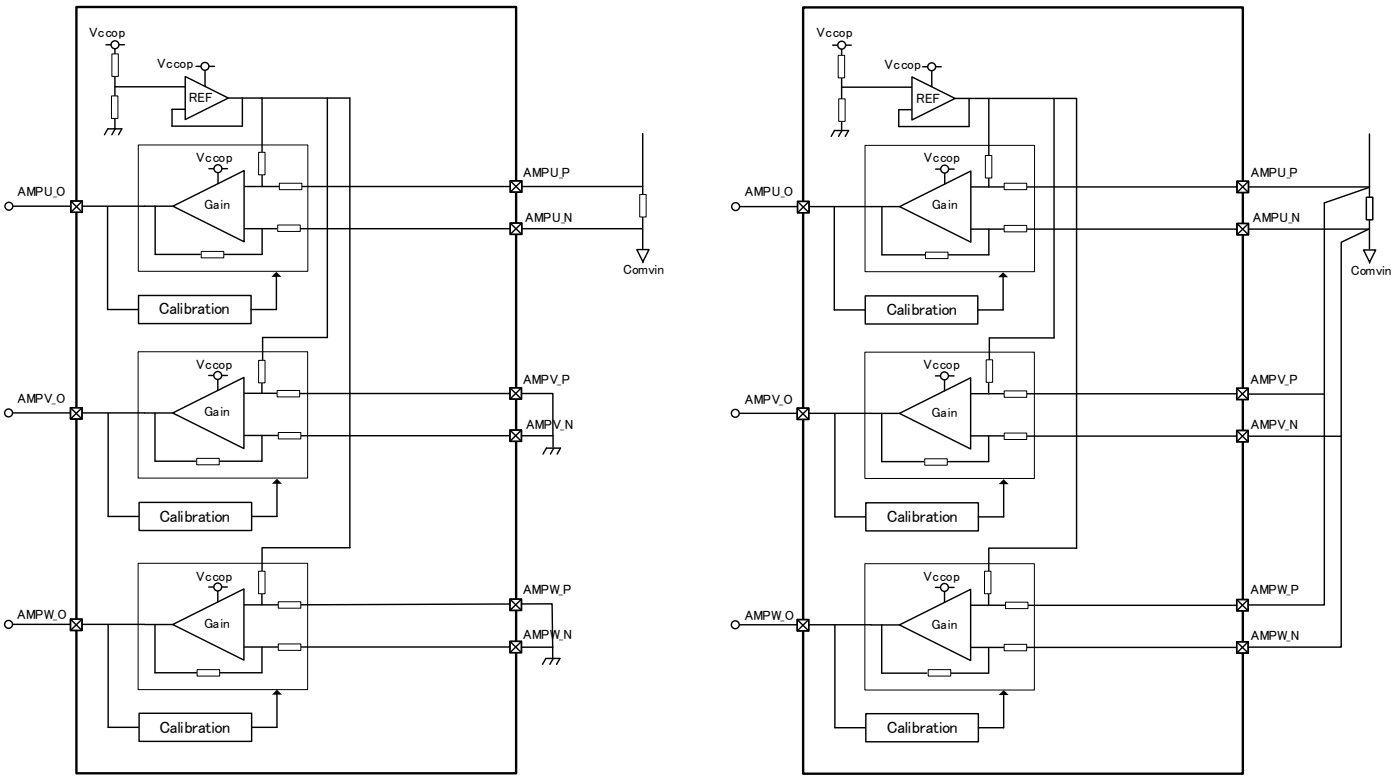


Fig. 7.3-b Block diagram for motor current detector circuit (single shunt)

7.3.2. Offset calibration

A cal_amp_* (where * denotes u, v or w) value of "1" in the AMP_CTRL register is used to perform offset calibration of the current detection amp. To ensure accurate calibration, the input difference voltage must be 0 V (equivalent potential). Figure 7.3-c shows the block diagram. Cal_amp_* initiates the offset calibration procedure and updates the AMP_STAT register cal_en to "H." For the duration of the procedure, GAIN_SEL is fixed at 5 h (equivalent to 30 x). The offset calibration value is

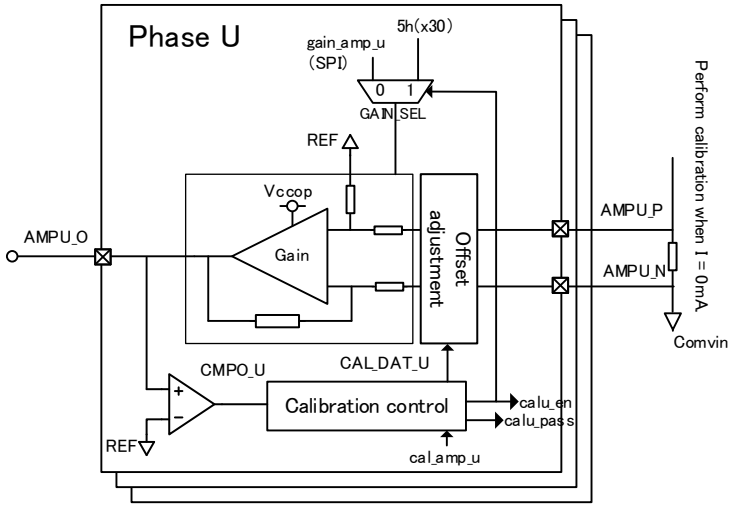


Fig. 7.3-c Block diagram for offset calibration

determined by varying CAL_DAT_* and monitoring amp output against REF. When calibration is complete, cal_en changes to "L" and the calibration result is evaluated and then forwarded to cal*_pass. If cal*_pass is "H" the calibration result is retained as the adjustment value; if cal*_pass is "L" the result is discarded and the default (reset) value is restored.

Where multiple bits have been set simultaneously in cal_amp_* in the AMP_CTRL register, offset calibrations are performed simultaneously for the corresponding phases. When cal_en in the AMP_STAT register changes to "L" and calibration is

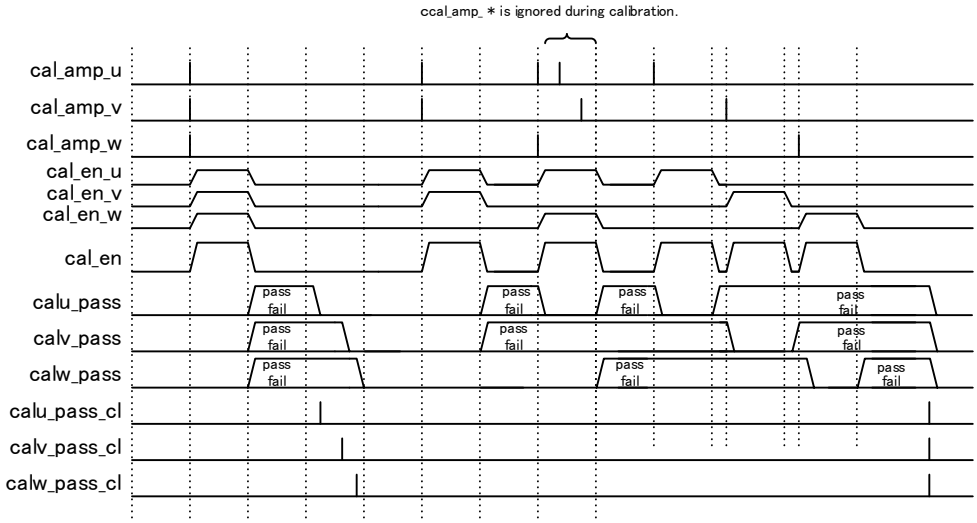


Fig. 7.3-d Offset calibration

complete, cal*_pass is registered. The status can be cleared at any time by writing "1" to the cal*_pass_cl bit in the AMP_STAT_CLR register. Note that cal*_pass automatically updates to "L" when calibration for the corresponding phase begins. During calibration, cal_en is "H" and cal_amp_* settings will be ignored.

7.4. Oscillator circuits

The TB9083FTG has two internal oscillator circuits: OSC_IF is used by the charge pump, and OSC_SM is used by the system clock, monitoring and SPI communication. Both oscillators have built-in CR and oscillate at 4 MHz (typ.). The oscillator circuits start up when the internal signal por_x is cancelled. The reference voltage source used for the two oscillators are independent of each other(BG1,BG2).

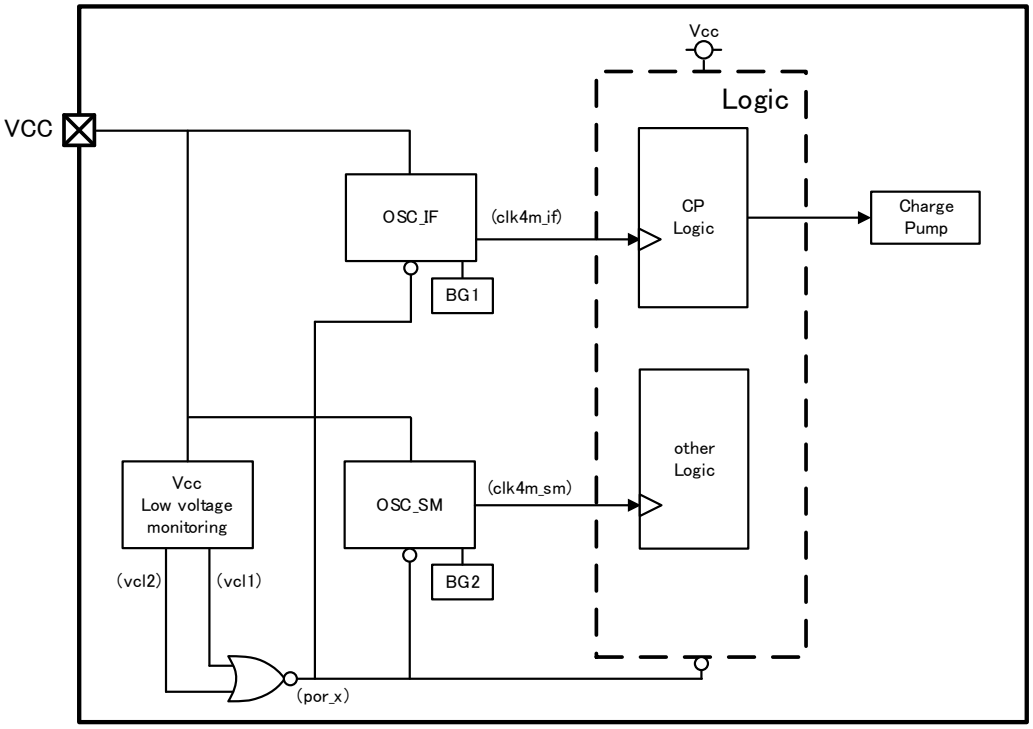


Fig. 7.4-a Oscillator block diagram

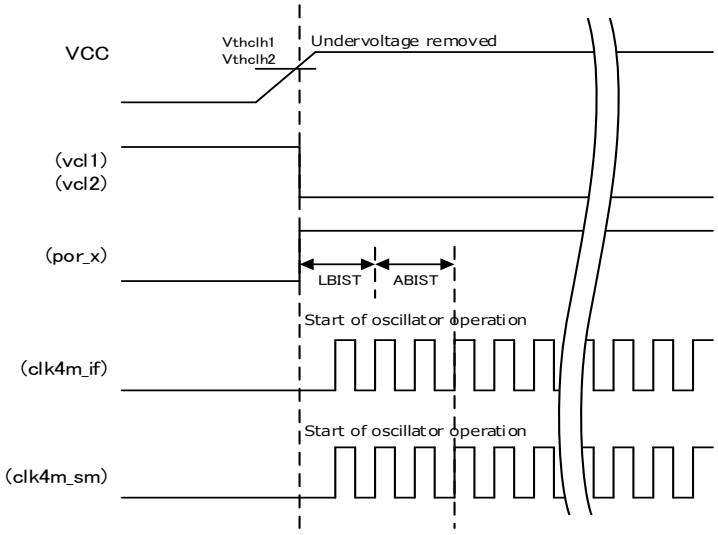


Fig. 7.4-b Oscillator circuit timing chart

7.5. Error detection circuits

The TB9083FTG has error detection circuits for undervoltage (VB, VCC, VCC_OP), overvoltage (VCPH, VCC, VCC_OP, external MOSFET VGS), overtemperature, external MOSFET VDS and abnormal frequency. For operational descriptions refer to Section 7.5.1 onwards. When an error is detected and the pre-driver circuit has been switched off, external MOSFET VDS detection is disabled. Once the error has been rectified and the pre-driver circuit is operational, the external MOSFET VDS detection is re-enabled.

Table 7.5-a Monitoring functions

Monitoring features	Reg. setting	Bit setting	Operation in detection (Note4,5,6,7)	Initial state	BIST (Note8)	Status Reg. (Note2)	Status Clear (Note1)	NDIAG (Note3)
VCC undervoltage1 VCC undervoltage 2	–	–	All(9ch) pre-drivers: OFF, Charge pump: OFF, Oscillator: OFF	–	–	–	–	"L"
VB undervoltage	uvb_op	"000"	All(9ch) pre-drivers: OFF	–	A	uvb	uvb_cl	"L"
		"001"	All(9ch) pre-drivers: OFF	X			–	"L"
		"010"	All(9ch) pre-drivers: OFF	–			–	"H"
		"011"	Motor (6ch) pre-driver: OFF	–			uvb_cl	"L"
		"100"	Motor (6ch) pre-driver: OFF	–			–	"L"
		"101"	Motor (6ch) pre-driver: OFF	–			–	"H"
VCPH overvoltage	ocph_op	"000"	Detection disabled	X	A	–	–	"H"
		"001"	Continued operation	–		ocph	ocph_cl	"L"
		"010"	All(9ch) pre-drivers: OFF	–				
		"011"	Motor (6ch) pre-driver: OFF	–				
		"100"	All(9ch) pre-drivers: OFF, Charge pump: OFF	–				
		"101"	All(9ch) pre-drivers: OFF, Charge pump: OFF	–				
VCC overvoltage	ovc_op	"000"	Detection disabled	–	A	–	–	"H"
		"001"	Continued operation	–		ovcc	ovcc_cl	"L"
		"010"	All(9ch) pre-drivers: OFF	X				
		"011"	Motor (6ch) pre-driver: OFF	–				
		"100"	All(9ch) pre-drivers: OFF, Charge pump: OFF	–				
		"101"	All(9ch) pre-drivers: OFF (hold), Charge pump: OFF (hold)	–				
VCC_OP undervoltage	uvccop_op	"000"	Detection disabled	X	A	–	–	"H"
		"001"	Continued operation	–		uvccop	uvccop_cl	"L"
		"010"	All(9ch) pre-drivers: OFF	–				
		"011"	Motor (6ch) pre-driver: OFF	–				
		"100"	All(9ch) pre-drivers: OFF, Charge pump: OFF	–				
		"101"	All(9ch) pre-drivers: "L"(hold), Charge pump: OFF (hold)	–				
VCC_OP overvoltage	ovccop_op	"000"	Detection disabled	X	A	–	–	"H"
		"001"	Continued operation	–		ovccop	ovvccop_cl	"L"
		"010"	All(9ch) pre-drivers: OFF	–				
		"011"	Motor (6ch) pre-driver: OFF	–				
		"100"	All(9ch) pre-drivers: OFF, Charge pump: OFF	–				
		"101"	All(9ch) pre-drivers: "L"(hold),	–				

Monitoring features	Reg. setting	Bit setting	Operation in detection (Note4,5,6,7)	Initial state	BIST (Note8)	Status Reg. (Note2)	Status Clear (Note1)	NDIAG (Note3)
			Charge pump: OFF (hold)					
Over temperature	tsd_op	"000"	Detection disabled	–	A	–	–	"H"
		"001"	Continued operation	–		tsd	tsd_cl	"L"
		"010"	All(9ch) pre-drivers: OFF	X				
		"011"	Motor (6ch) pre-driver: OFF	–				
		"100"	All(9ch) pre-drivers: OFF Charge pump: OFF	–				
		"101"	All(9ch) pre-drivers: OFF (hold) Charge pump: OFF (hold)	–				
ALARM	alr_op	"0"	All(9ch) pre-drivers: OFF	X	–	alm_det	–	"L"
		"1"	Motor (6ch) pre-driver: OFF	–				
External MOSFET Vds (high side)	vdsh_op	"0000"	Detection disabled	–	–	–	–	"H"
		"0001"	Continued operation	–		vds_uh vds_vh vds_wh	vds_uh_cl vds_vh_cl vds_wh_cl	"L"
		"0010"	Detected phase pre-driver: OFF	–				
		"0011"	Detected phase pre-driver: OFF(hold)	–				
		"0100"	All(9ch) pre-drivers: OFF	–				
		"0101"	All(9ch) pre-drivers: OFF(hold)	–				
		"0110"	Motor (6ch) pre-driver: OFF	–				
		"0111"	Motor (6ch) pre-driver: OFF(hold)	X				
		"1000"	All(9ch) pre-drivers: OFF, Charge pump: OFF	–				
		"1001"	All(9ch) pre-drivers: OFF(hold), Charge pump: OFF (hold)	–				
External MOSFET Vds (low side)	vdsl_op	"0000"	Detection disabled	–	–	–	–	"H"
		"0001"	Continued operation	–		vds_ul vds_vl vds_wl	vds_ul_cl vds_vl_cl vds_wl_cl	"L"
		"0010"	Detected phase pre-driver: OFF	–				
		"0011"	Detected phase pre-driver: OFF(hold)	–				
		"0100"	All(9ch) pre-drivers: OFF	–				
		"0101"	All(9ch) pre-drivers: OFF(hold)	–				
		"0110"	Motor (6ch) pre-driver: OFF					
		"0111"	Motor (6ch) pre-driver:OFF(hold)	X				
		"1000"	All(9ch) pre-drivers: OFF, Charge pump: OFF	–				
		"1001"	All(9ch) pre-drivers: OFF(hold), Charge pump: OFF (hold)	–				
external MOSFET Vgs overvoltage	vgs_op	"000"	Detection disabled	–	A	–	–	"H"
		"001"	Continued operation	–		vgs_uh vgs_ul vgs_vh vgs_vl vgs_wh vgs_wl	vgs_uh_cl vgs_ul_cl vgs_vh_cl vgs_vl_cl vgs_wh_cl vgs_wl_cl	"L"
		"010"	All(9ch) pre-drivers: OFF	–				
		"011"	Motor (6ch) pre-driver: OFF	–				
		"100"	All(9ch) pre-drivers: OFF, Charge pump: OFF	–				
		"101"	All(9ch) pre-drivers: OFF(hold), Charge pump: OFF (hold)	X				

Monitoring features	Reg. setting	Bit setting	Operation in detection (Note4,5,6,7)	Initial state	BIST (Note8)	Status Reg. (Note2)	Status Clear (Note1)	NDIAG (Note3)
Abnormalities in frequency (Note 9)	ferr_op	"000"	Detection disabled	○	L	–	–	"H"
		"001"	Continued operation	–		err_of err_uf	err_of_cl err_uf_cl	"L"
		"010"	All(9ch) pre-drivers: OFF	–				
		"011"	Motor (6ch) pre-driver: OFF	–				
		"100"	All(9ch) pre-drivers: OFF, Charge pump: OFF	–				
		"101"	All(9ch) pre-drivers: OFF(hold), Charge pump: OFF (hold)	–				
Pre-driver Inhibition input	pl_op	"0"	Detected phase pre-driver: OFF	○	–	–	–	"H"
		"1"	Detected phase pre-driver: OFF	–		err_pl_u err_pl_v err_pl_w	err_pl_u_cl err_pl_v_cl err_pl_w_cl	"L"
SPI communication error	–	–	Detection disabled	–	–	err_spi	err_spi_cl	"L"
QA calculation	qat_op	"001"	Continued operation	○	L	err_qac	err_qac_cl	"L"
		"010"	All(9ch) pre-drivers: OFF(hold)	–				
		"011"	Motor (6ch) pre-driver: OFF	–				
		"100"	All(9ch) pre-drivers: OFF(hold), Charge pump: OFF (hold)	–				

Note1 In settings modes where the status clear bit is shown in the Status Clear column, once a status bit has been set by the error detection function, it will be retained until cleared by writing "1" to the corresponding status clear bit. A retained status register cannot be cleared while the error detection circuit is still showing an error. In operation modes that do not have a status clear bit in the Status Clear column, the status bit is cleared when error detection is resolved.

Note2 A dash in the Status Reg column indicates that no value is set in the status register for that operating mode.

Note3 "H" in the NDIAG column means that the NDIAG terminal does not change to "L" when an error is detected. "L" in the NDIAG column means that the NDIAG terminal will be the same as the status register (with the exception of VCC undervoltage detection). NDIAG output is "L" while the status register is retained, but reverts to "H" when all status registers are cleared. In operating modes where the status register is not retained, NDIAG reverts to "H" when error detection is cleared, irrespective of whether the status register has been cleared.

Note4 "(Retained)" in the Response to Detection column means that the response is dictated by the retained status register. To revert to the standard response, the status register needs to be cleared. Where "(Retained)" does not appear, this means that the normal response will be restored once error detection is cleared, without needing to clear the status register.

Note5 The value ****_op in the settings register for a monitoring function can be modified at any time; however, ****_op has no effect on actual operations while the corresponding status register is indicating that an error has been detected.

Note6 "Charge pump off" means the CP_SW is off and the CP driver stopped.

Note7 “All (9ch) pre-drivers:OFF”, the pre-driver is driven to “L” so that the external FET including the safety relay is turned off. "Motor (6ch) pre-drivers:OFF" drives the pre-driver to "L" so that the external FET except the safety relay is turned off. “Detected phase pre-driver : OFF”, the pre-driver is driven to “L” to turn off the high-side and low-side FET of the phase where the abnormality is detected.

Note8 A = ABIST, L = LBIST

Note9 If the OSC_SM clock is lost, the detection response can still be executed but NDIAG will not change to "L."

7.5.1. VCC undervoltage detection 1 and 2

This circuit has two built-in comparators for detecting low VCC voltage; an "H" value from either of the comparators indicates undervoltage. The band gap voltages used as the baseline reference by the comparators are generated by band gap circuits BG1 and BG2.

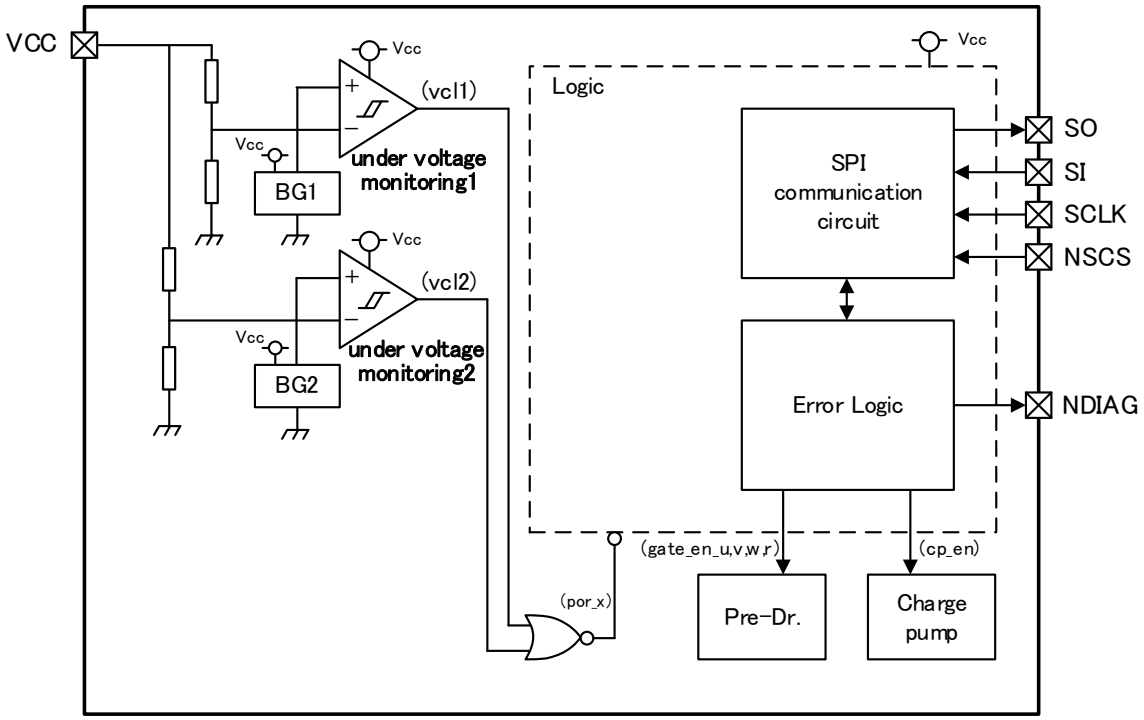


Fig. 7.5.1-a Block diagram for VCC undervoltage detector

➢ ① VCC voltage drops

VCC voltage drops below the undervoltage Vthcll1/Vthcll2.

➢ ② VCC undervoltage detected

After the response time Tcl, VCC undervoltage signal (vcl1), (vcl2) "H" denotes undervoltage detection, (por_x) changes to "L" and NDIAG output is "L." The motor drive (6 ch) pre-driver, safety relay (3 ch) pre-driver, charge pump and oscillator circuits all switch off and remain off until the undervoltage is cancelled.

➢ ③ VCC voltage restored (undervoltage cancelled)

When VCC voltage is greater than Vthclh1/Vthclh2, VCC undervoltage signal (vcl1), (vcl2) changes to "L" and undervoltage is cancelled.

➢ ④ Normal operation resumes

If a BIST diagnosis of OK is returned after LBIST/ABIST execution, normal operation resumes. The charge pump circuit starts operating and the pre-driver circuits are re-enabled. If an NG diagnosis is returned, the charge pump and pre-driver circuits will not operate. NDIAG output is "H" for an OK diagnosis and "L" for a NG diagnosis. (See Section 7.7 for details.)

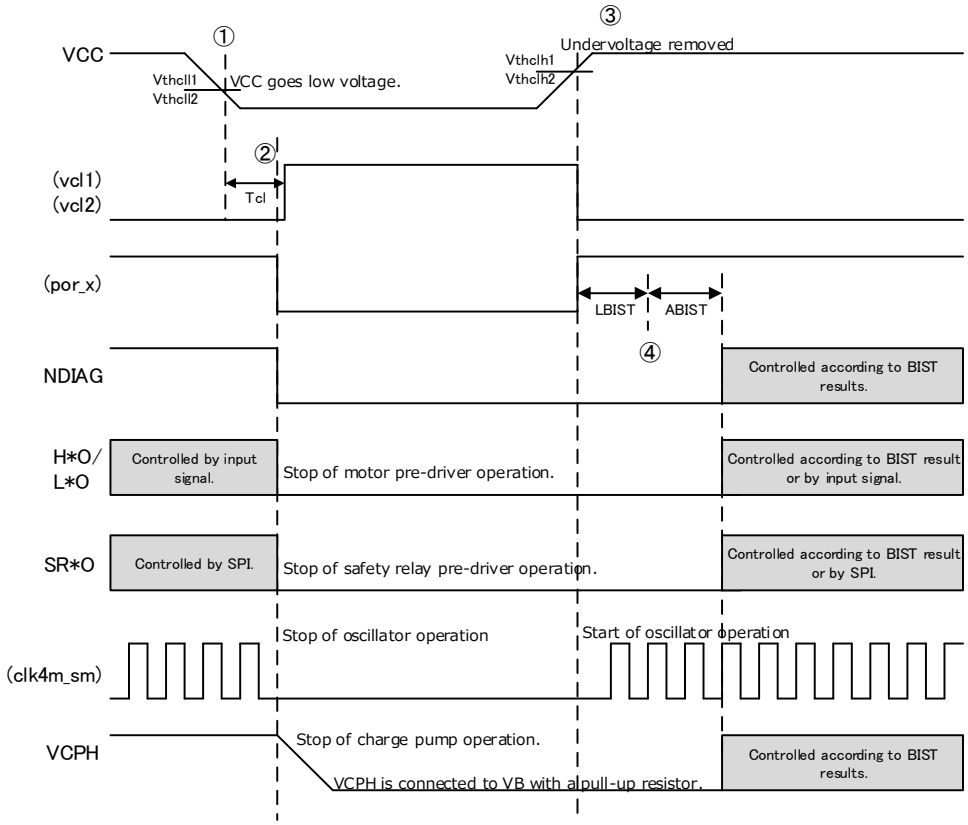


Fig. 7.5.1-b Timing chart for VCC undervoltage detection

Note: If the Vcc voltage falls further below the undervoltage threshold, standby mode will be engaged, whereby all functions other than Vcc undervoltage detection are switched off.

7.5.2. VB undervoltage detection

This circuit comprises a comparator and a filter for detecting VB undervoltage; filter output of "H" indicates undervoltage. The band gap voltage used as the baseline reference by the comparator is generated by the band gap circuit BG2.

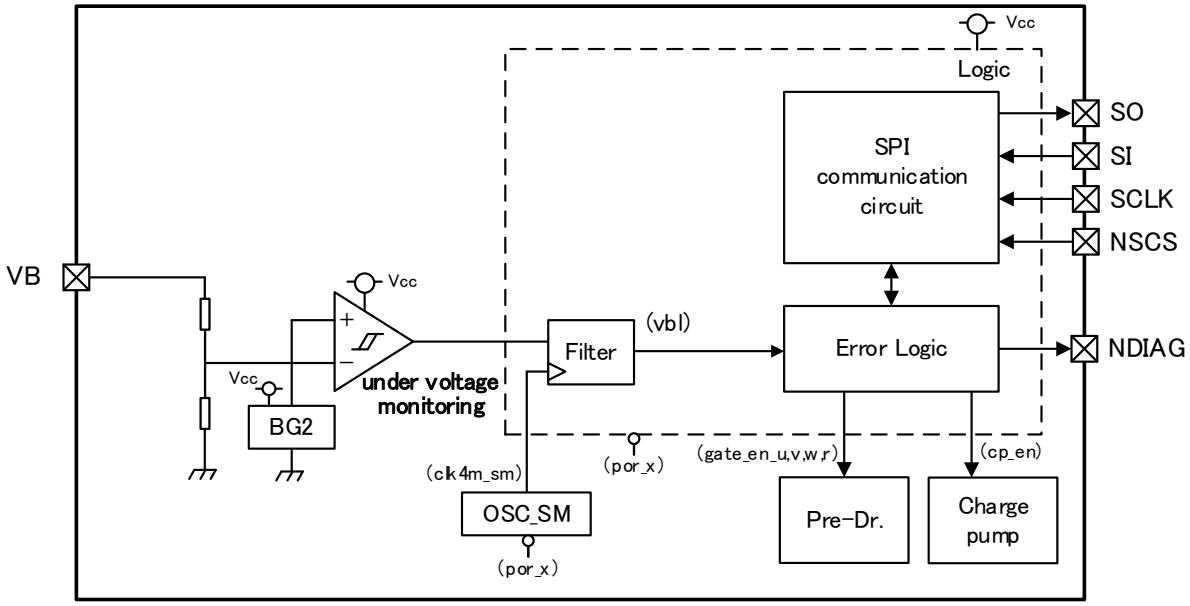


Fig. 7.5.2-a Block diagram for VB undervoltage detection

➢ ① VB voltage drops

VB voltage drops below the undervoltage threshold Vthbll. Vb L detection comparator outputs H.

➢ ② VB undervoltage detected

After the detection filter time Tbl has elapsed, VB undervoltage signal (vbl) "H" indicating undervoltage is generated, and all (9 ch) pre-driver circuits including safety relay switch off, as well as the motor drive (6 ch) pre-driver circuit. Note that the oscillator and charge pump circuits do not switch off. Pre-driver circuits remain off until undervoltage is cancelled.

At this point one of six operating modes can be selected via the SPI.

If the mode is changed during VB undervoltage, settings will not be enabled until the undervoltage is cancelled and the uvb register is cleared.

➢ ③ VB voltage restored (undervoltage cancelled)

Once the VB voltage exceeds Vthblh, the VB undervoltage signal (vbl) changes to "L," undervoltage is cancelled and normal operation resumes.

If NDIAG output is "L," clear the uvb register via the SPI to change it back to "H."

During an undervoltage, uvb register cannot be cleared and NDIAG output is "L."

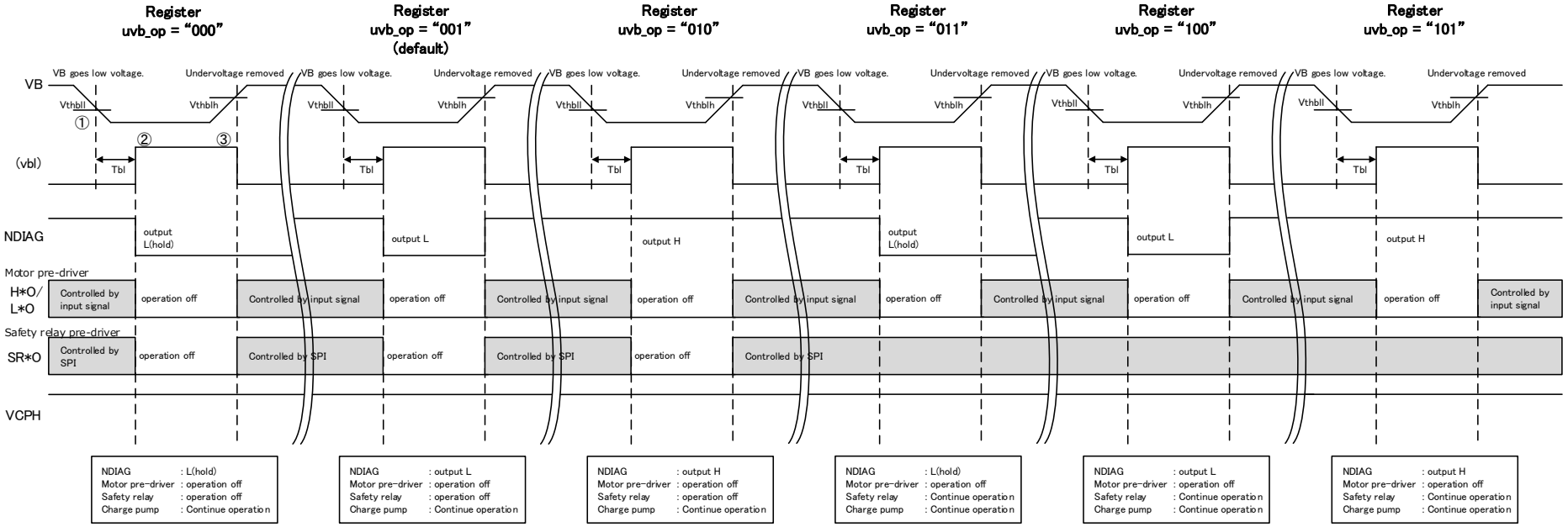


Fig. 7.5.2-b Timing chart for VB undervoltage detection

7.5.3. VCPH overvoltage detection

This circuit comprises a comparator and a filter; filter output of "H" indicates overvoltage. The band gap voltage used as the baseline reference by the comparator is generated by the band gap circuit BG2.

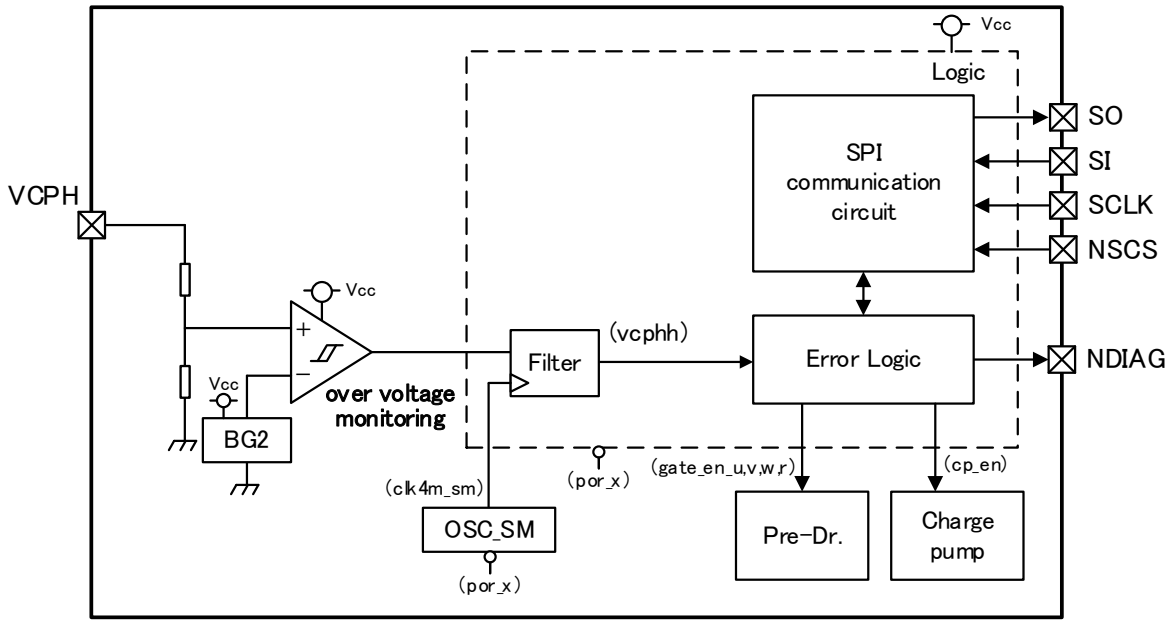


Fig. 7.5.3-a Block diagram for VCPH overvoltage

➢ ① VCPH voltage rises

VCPH voltage exceeds the overvoltage threshold Vthcphh. VCPH H detection comparator outputs "H."

➢ ② VCPH overvoltage detected

After the filter time Tcphh has elapsed, VCPH overvoltage signal (vcphh) "H" indicating overvoltage is generated and NDIAG output is "L," except where the register ocph_op is "000," in which case NDIAG output remains at "H" and all circuits continue to operate as normal.

At this point one of six operating modes can be selected via the SPI.

If the mode is changed during VCPH overvoltage, settings will not be enabled until the overvoltage is cancelled and the ocph register is cleared.

➢ ③ VCPH voltage restored (overvoltage cancelled)

Once the VCPH voltage drops below Vthcphhl, the VCPH overvoltage signal (vcphh) changes to "L" and the overvoltage is cancelled.

When register ocph_op is "101," the charge pump and pre-drivers remain off after the overvoltage is cancelled and NDIAG remains at "L."

When register ocph_op is "001", "010", "011" or "100," the charge pump and pre-drivers operate normally but the status register is retained and NDIAG remains at "L."

When register ocph is cleared via SPI, NDIAG changes to "H."

During an overvoltage, register ocph cannot be cleared and NDIAG output is "L."

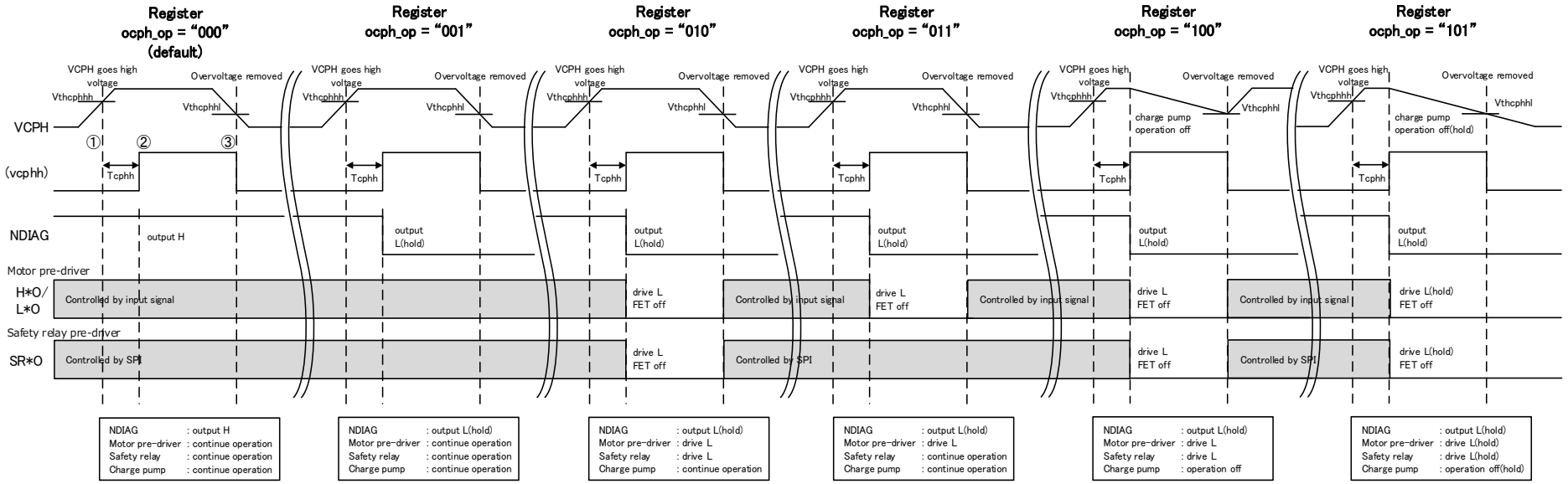


Fig. 7.5.3-b Timing chart for VCPH overvoltage

7.5.4. VCC overvoltage detection

This circuit comprises a comparator and a filter; filter output of "H" indicates overvoltage. The band gap voltage used as the baseline reference by the comparator is generated by the band gap circuit BG2.

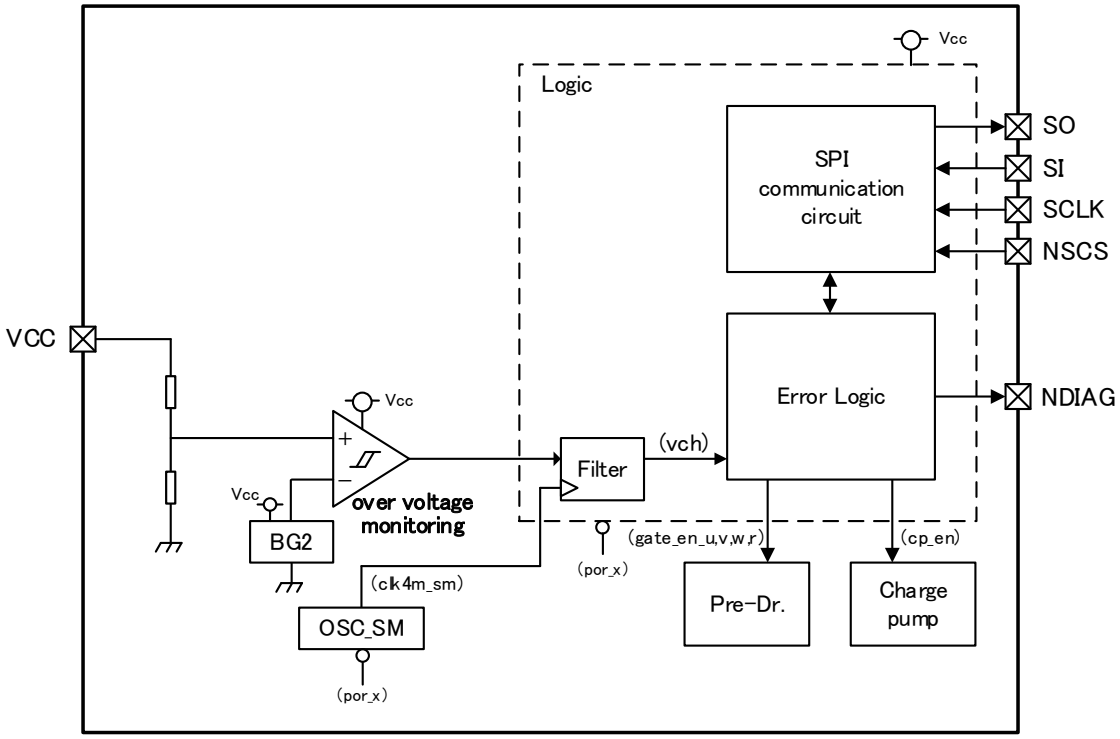


Fig. 7.5.4-a Block diagram for VCC overvoltage detection

➢ ① VCC voltage rises

VCC voltage exceeds the overvoltage threshold Vthchh. VCC H detection comparator outputs "H."

➢ ② VCC overvoltage detected

After the filter time Tch has elapsed, VCC overvoltage signal (vch) "H" indicating overvoltage is generated and NDIAG output is "L," except where the register ovc_op is "000," in which case NDIAG output remains at "H" and all circuits continue to operate as normal.

At this point one of six operating modes can be selected via the SPI.

If the mode is changed during VCC overvoltage, settings will not be enabled until the overvoltage is cancelled and the ovc register is cleared.

➢ ③ VCC voltage restored (overvoltage cancelled)

Once the VCC voltage drops below Vthchl, the VCC overvoltage signal (vch) changes to "L" and the overvoltage is cancelled.

When register ovc_op is "101," the charge pump and pre-drivers remain off after the overvoltage is cancelled and NDIAG remains at "L."

When register ovc_op is "001", "010", "011" or "100," the charge pump and pre-drivers operate normally but the status register is retained and NDIAG remains at "L."

When register ovc is cleared via the SPI, NDIAG changes to "H."

During an overvoltage, register ovc cannot be cleared and NDIAG output is "L."

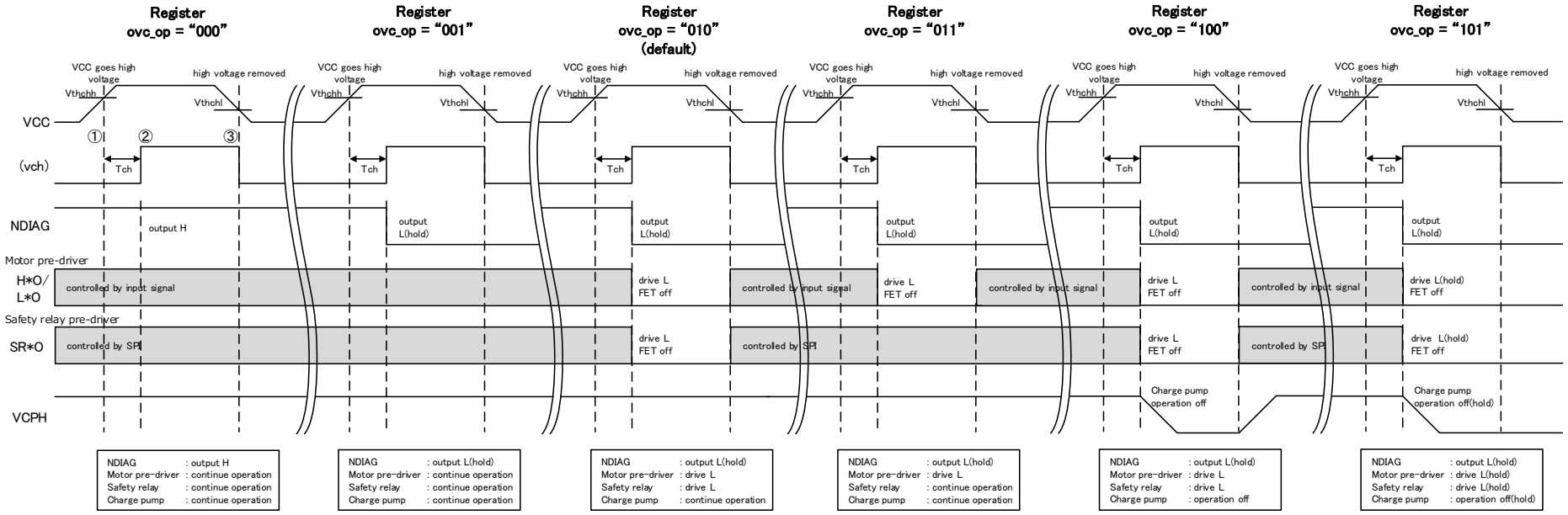


Fig. 7.5.4-b Timing chart for VCC overvoltage detection

7.5.5. VCC_OP undervoltage detection

This circuit comprises a comparator and a filter; filter output of "H" indicates undervoltage. The band gap voltage used as the baseline reference by the comparator is generated by the band gap circuit BG2.

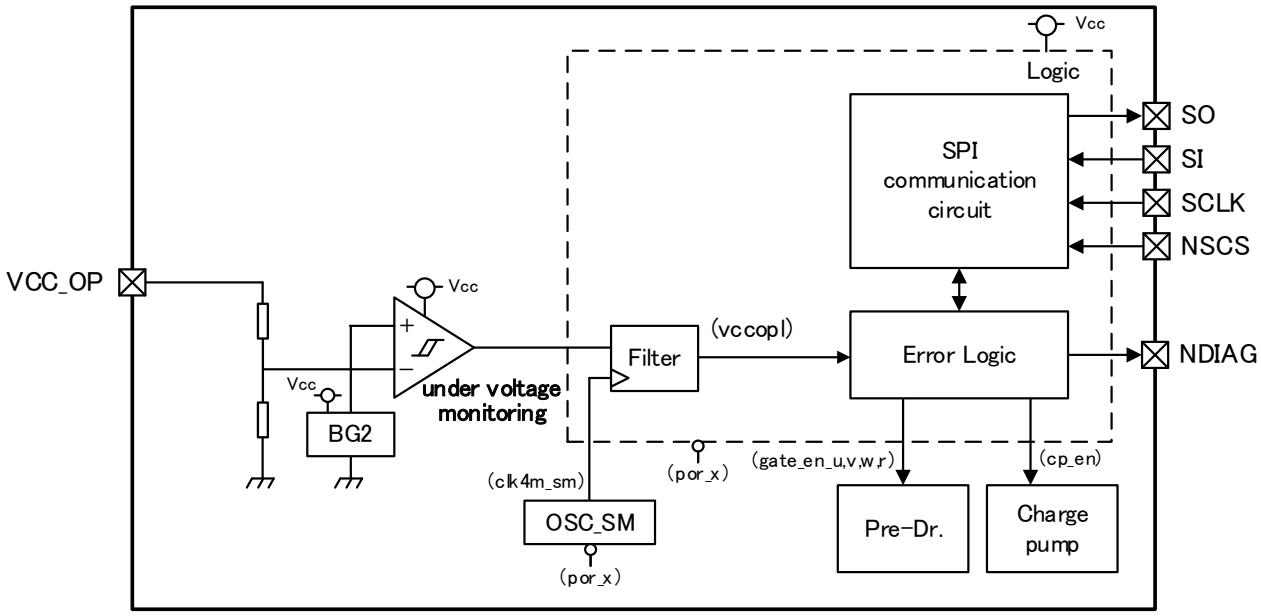


Fig. 7.5.5-a Block diagram for VCC_OP undervoltage detection

➢ ① VCC_OP voltage drops

VCC_OP voltage drops below the undervoltage threshold Vthccopll. VCC_OP L detection comparator outputs "H."

➢ ② VCC_OP undervoltage detected

After the detection filter time Tccopl has elapsed, VCC_OP undervoltage signal (vccopl) "H" indicating undervoltage is generated and NDIAG becomes "L," except where the register uvccop_op is "000," in which case NDIAG output remains at "H" and all circuits continue to operate as normal.

At this point one of six operating modes can be selected via the SPI.

If the mode is changed during VCC_OP undervoltage, settings will not be enabled until the undervoltage is cancelled and the uvccop_op register is cleared.

➢ ③ VCC_OP voltage restored (undervoltage cancelled)

Once the VCC_OP voltage rises above Vthccoplh, the VCC_OP undervoltage signal (vccopl) changes to "L" and the undervoltage is cancelled.

When register uvccop_op is "101," the charge pump and pre-drivers remain off after the overvoltage is cancelled and NDIAG remains at "L."

When register uvccop_op is "001", "010", "011" or "100," the charge pump and pre-drivers operate normally but the status register is retained and NDIAG remains at "L."

When register uvccop is cleared via the SPI, NDIAG changes to "H."

During an overvoltage, register uvccop cannot be cleared and NDIAG output is "L."

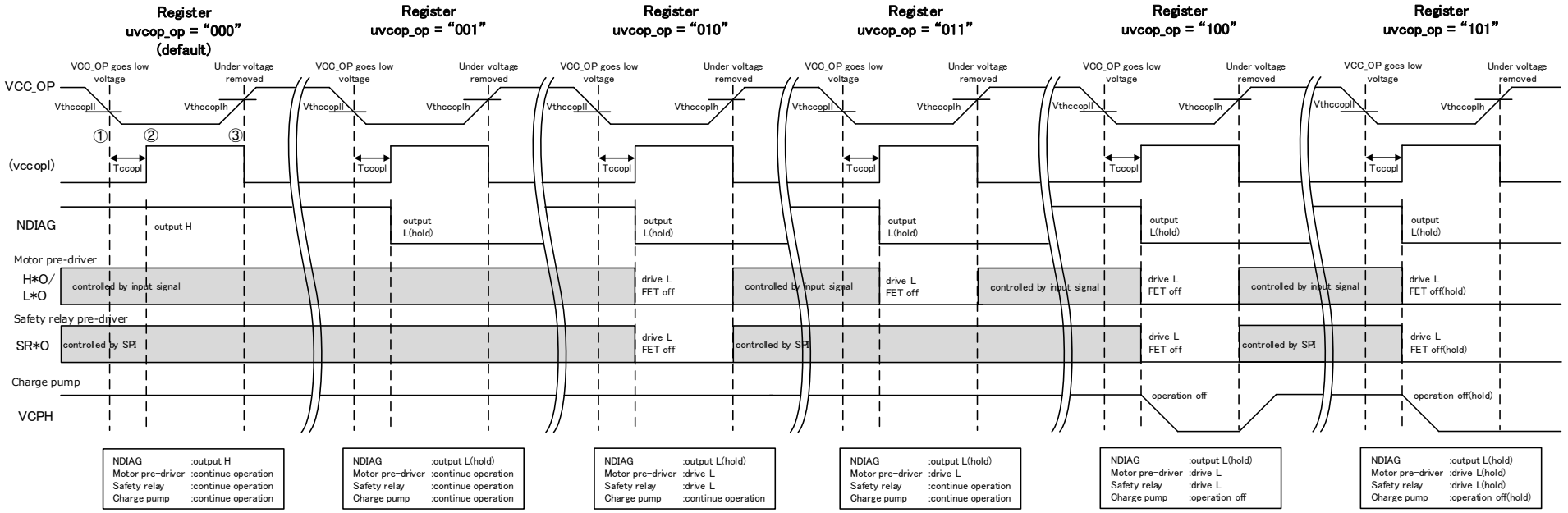


Fig. 7.5.5-b Timing chart for VCC_OP undervoltage detection

7.5.6. VCC_OP overvoltage detection

This circuit comprises a comparator and a filter; filter output of "H" indicates overvoltage. The band gap voltage used as the baseline reference by the comparator is generated by the band gap circuit BG2.

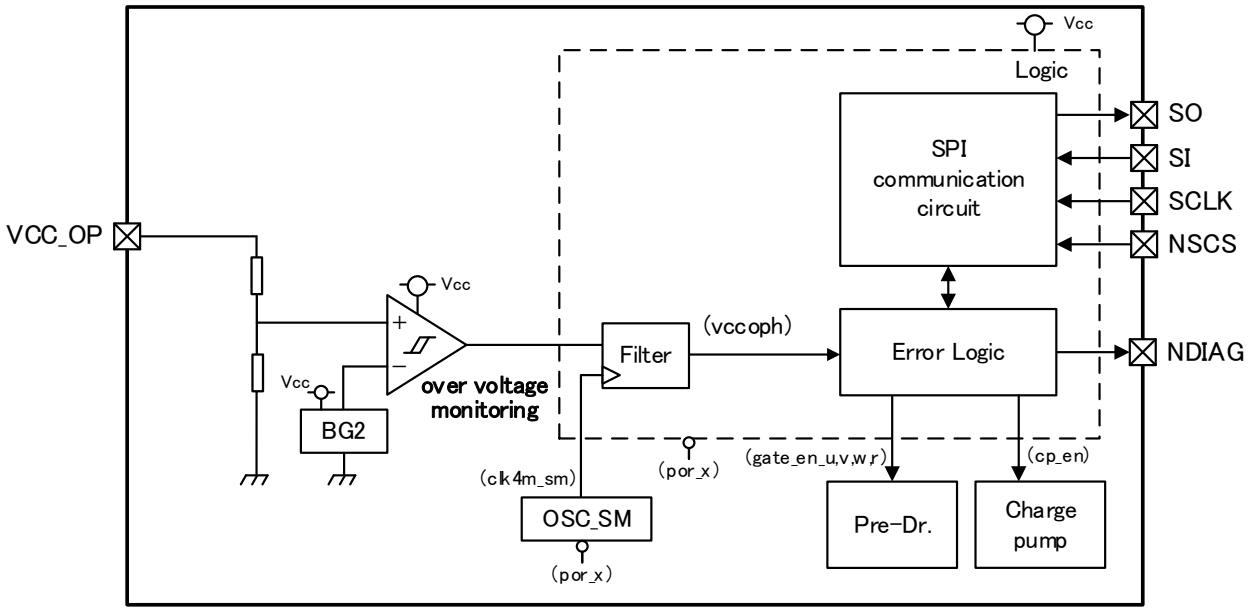


Fig. 7.5.6-a Block diagram for VCC_OP overvoltage detection

➢ ① VCC_OP voltage rises

VCC_OP voltage exceeds the overvoltage threshold Vthccophh. VCC_OP H detection comparator outputs "H."

➢ ② VCC_OP overvoltage detected

After the filter time Tccoph has elapsed, VCC_OP overvoltage signal (vccoph) "H" indicating overvoltage is generated and NDIAG output is "L," except where the register ovcop_op is "000," in which case NDIAG output remains at "H" and all circuits continue to operate as normal.

At this point one of six operating modes can be selected via the SPI.

If the mode is changed during VCC_OP overvoltage, settings will not be enabled until the overvoltage is cancelled and the ovccop register is cleared.

➢ ③ VCC_OP voltage restored (overvoltage cancelled)

Once the VCC_OP voltage drops below Vthccophl, the VCC_OP overvoltage signal (vccoph) changes to "L" and the overvoltage is cancelled.

When register ovcop_op is "101," the charge pump and pre-drivers remain off after the overvoltage is cancelled and NDIAG remains at "L."

When register ovcop_op is "001", "010", "011" or "100," the charge pump and pre-drivers operate normally but the status register is retained and NDIAG remains at "L."

When register ovccop is cleared via the SPI, NDIAG changes to "H."

During an overvoltage, register ovccop cannot be cleared and NDIAG output is "L."

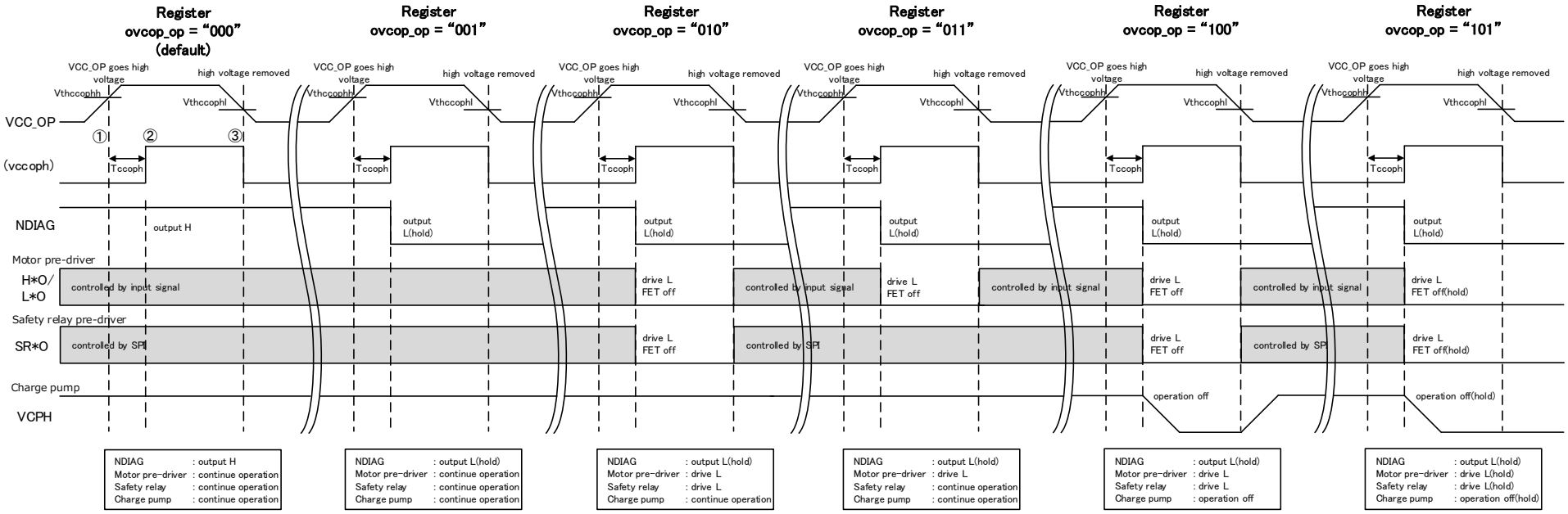


Fig. 7.5.6-b Timing chart for VCC_OP overvoltage detection

7.5.7. Overtemperature detection

The built-in overtemperature detector comprises a detection comparator and a filter; filter output of "H" indicates overtemperature. The band gap voltage used as the baseline reference by the comparator is generated by the band gap circuit BG2.

A chip temperature higher than Tsdh is deemed by the overtemperature detection comparator to be an overtemperature. When the internal temperature falls below Tsdl, the overtemperature is cancelled. At this point one of six operating modes can be selected via the SPI.

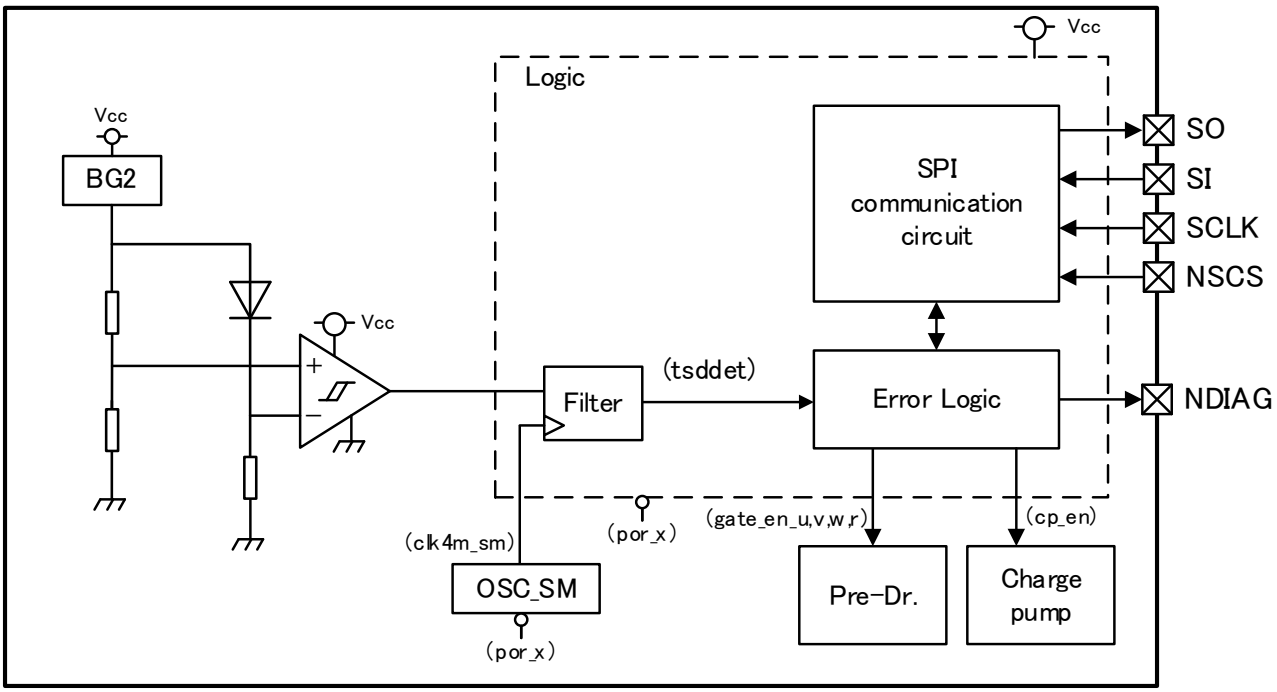


Fig. 7.5.7-a Overtemperature detection block diagram

➢ ①② Overtemperature detected

If the temperature exceeds Tsdh then, after the detection filter time Ttsd has elapsed, the overtemperature detected signal (tsddet) "H" is generated to indicate an overtemperature, and NDIAG changes to "L" except where register tsd_op is "000," in which case NDIAG remains at "H" and all circuits operate as normal.

At this point one of six operating modes can be selected via the SPI.

If the mode is changed during an overtemperature, settings will not be enabled until the overtemperature is cancelled and the tsd register is cleared.

➢ ③ Overtemperature cancelled

Once the temperature drops below Tsdl the overtemperature detected signal (tsddet) changes to "L" and the overtemperature is cancelled.

When register tsd_op is "101," the charge pump and pre-drivers remain off after the overtemperature is cancelled and NDIAG remains at "L."

When register tsd_op is "001", "010", "011" or "100," the charge pump and pre-drivers operate normally but the status register is retained and NDIAG remains at "L."

If register tsd is cleared via the SPI, NDIAG changes to "H."

During an overtemperature, register tsd cannot be cleared and NDIAG output is "L."

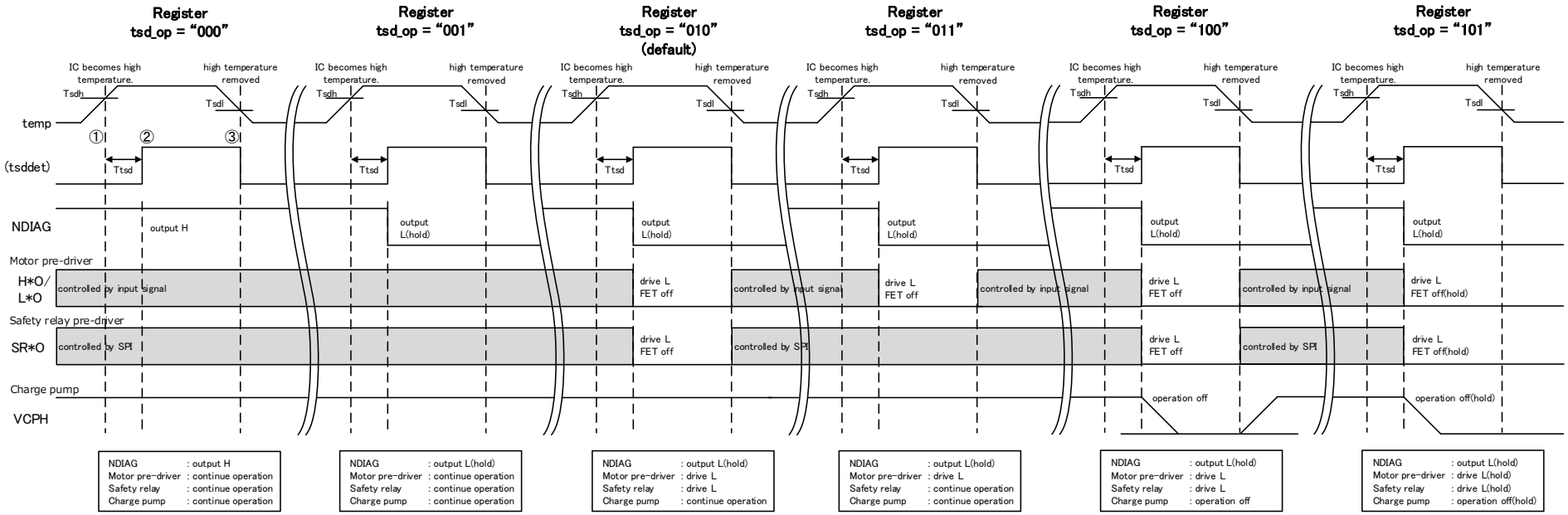


Fig. 7.5.7-b Timing chart for overtemperature detection

7.5.8. External MOSFET VDS detection

The external MOSFET drain and source terminals are monitored. The response to abnormal VDS is specified via the FET_OPSEL register (see Table 7.5-a for details). Similarly, the threshold voltage (value 12) and detection period (value 4) can be modified via the HS_VDS_SEL and LS_VDS_SEL registers. The HUS, HVS and HWS terminals are equipped with internal pull-up and pull-down resistors, though these are normally off (refer to Section 7.8 for details). In a phase where a fault has been detected and pre-drivers are disabled, VDS detection is switched off; consequently, other VDS factors will not be latched. VDS detection can be disabled on individual channels via the FET_DET_SEL register.

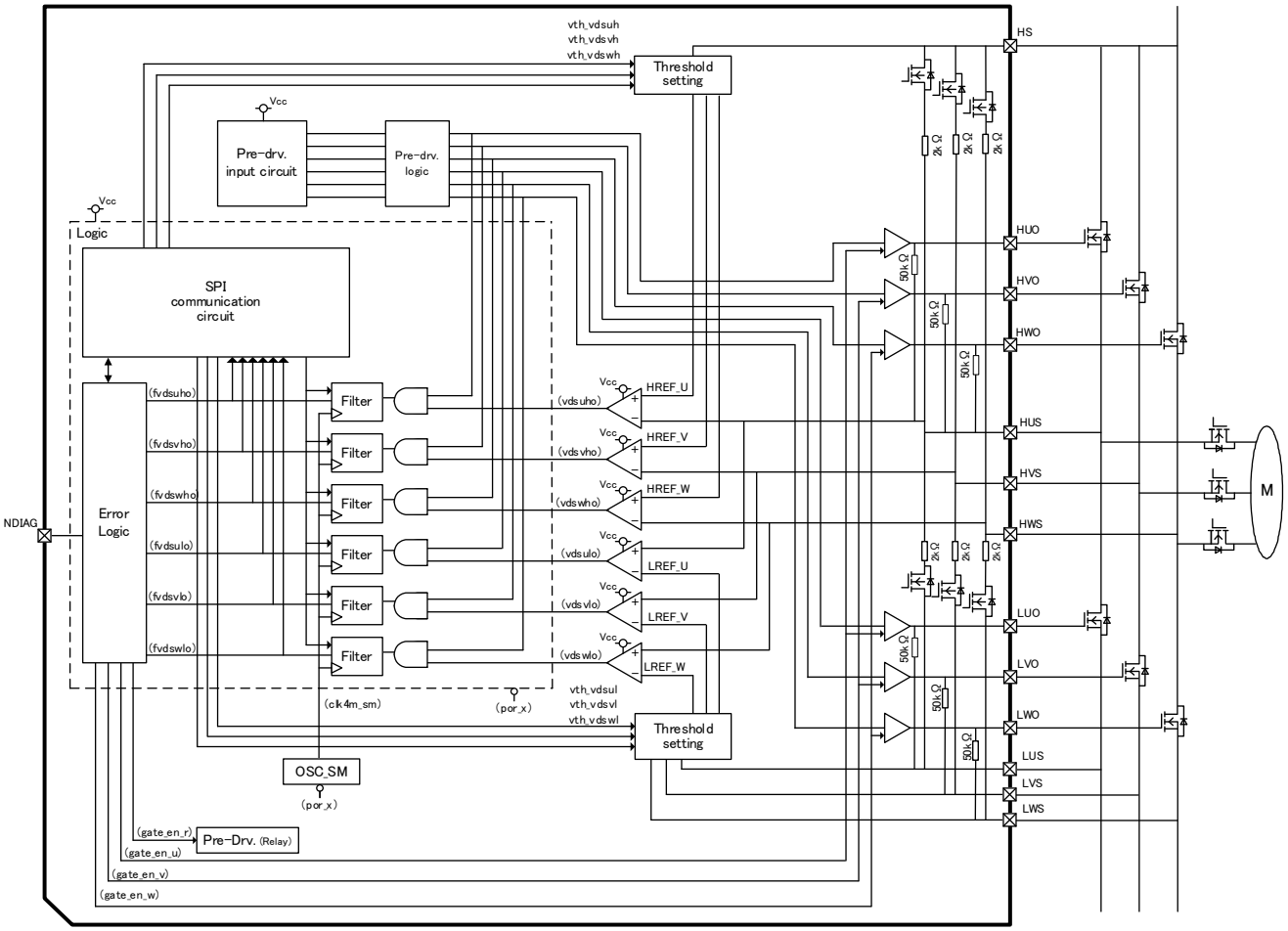


Fig. 7.5.8-a Block diagram for external MOSFET VDS detection

Table 7.5.8-a VDS detection scenarios

Comparator output comparison	Comparator Output	Input Signal	Description
V_{HUS}-V_{LUS} > $V_{thvdsul}$	(vdsulo) = "H"	LUI = "H"	VDS fault for low side U phase MOSFET
V_{HVS}-V_{LVS} > $V_{thvdsvl}$	(vdsvlo) = "H"	LVI = "H"	VDS fault for low side V phase MOSFET
V_{HWS}-V_{LWS} > $V_{thvdswl}$	(vdswlo) = "H"	LWI = "H"	VDS fault for low side W phase MOSFET
V_{HS}-V_{HUS} > $V_{thvdsuh}$	(vdsuho) = "H"	HUI = "H"	VDS fault for high side U phase MOSFET
V_{HS}-V_{HVS} > $V_{thvdsvh}$	(vdsvho) = "H"	HVI = "H"	VDS fault for high side V phase MOSFET
V_{HS}-V_{HWS} > $V_{thvdswh}$	(vdswho) = "H"	HWI = "H"	VDS fault for high side W phase MOSFET

Note

• The high side threshold voltage for detection is defined by the voltage across HS-H*S at the IC terminal. This value should take into account the high side MOSFET drain-source voltage.

• The low side threshold voltage for detection is defined by the voltage across H*S-L*S at the IC terminal. This value should take into account the low side MOSFET drain-source voltage.

• Asterisks (*)denote U, V and W.

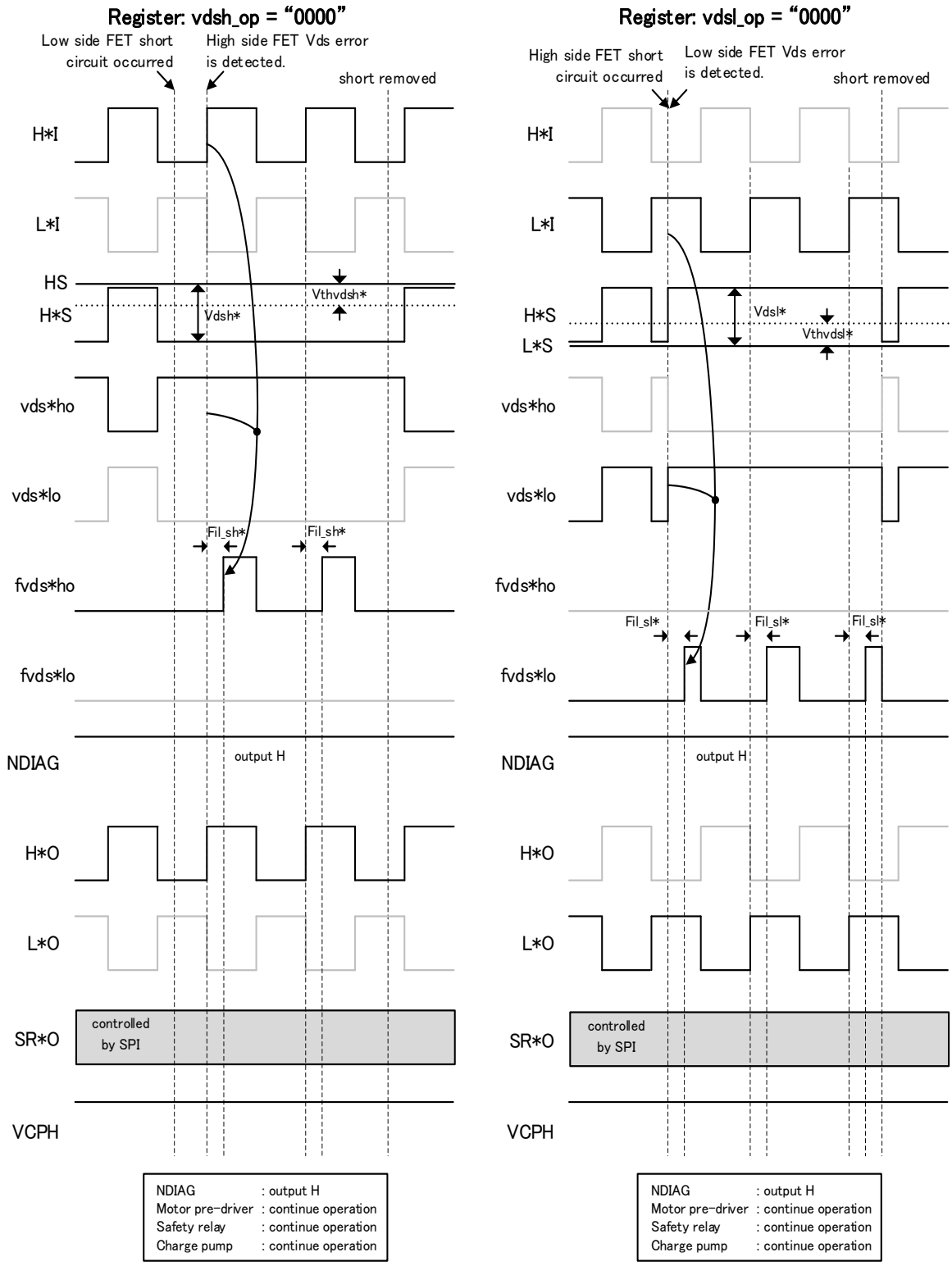


Fig. 7.5.8-b Timing chart for short-circuit detection (register vdsl_op = vdsh_op "0000")

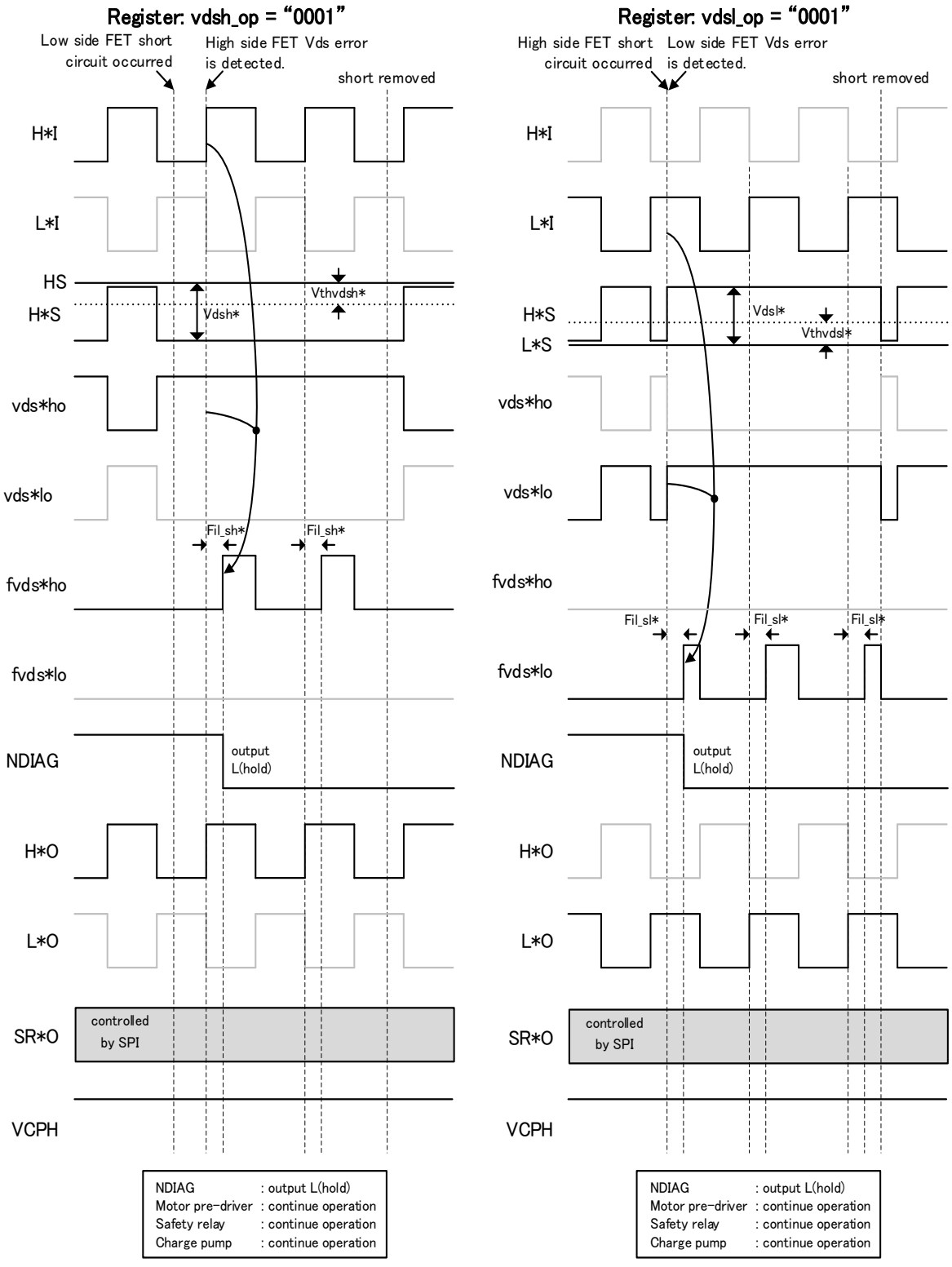


Fig. 7.5.8-c Timing chart for short-circuit detection (register vdsl_op = vdsh_op "0001")

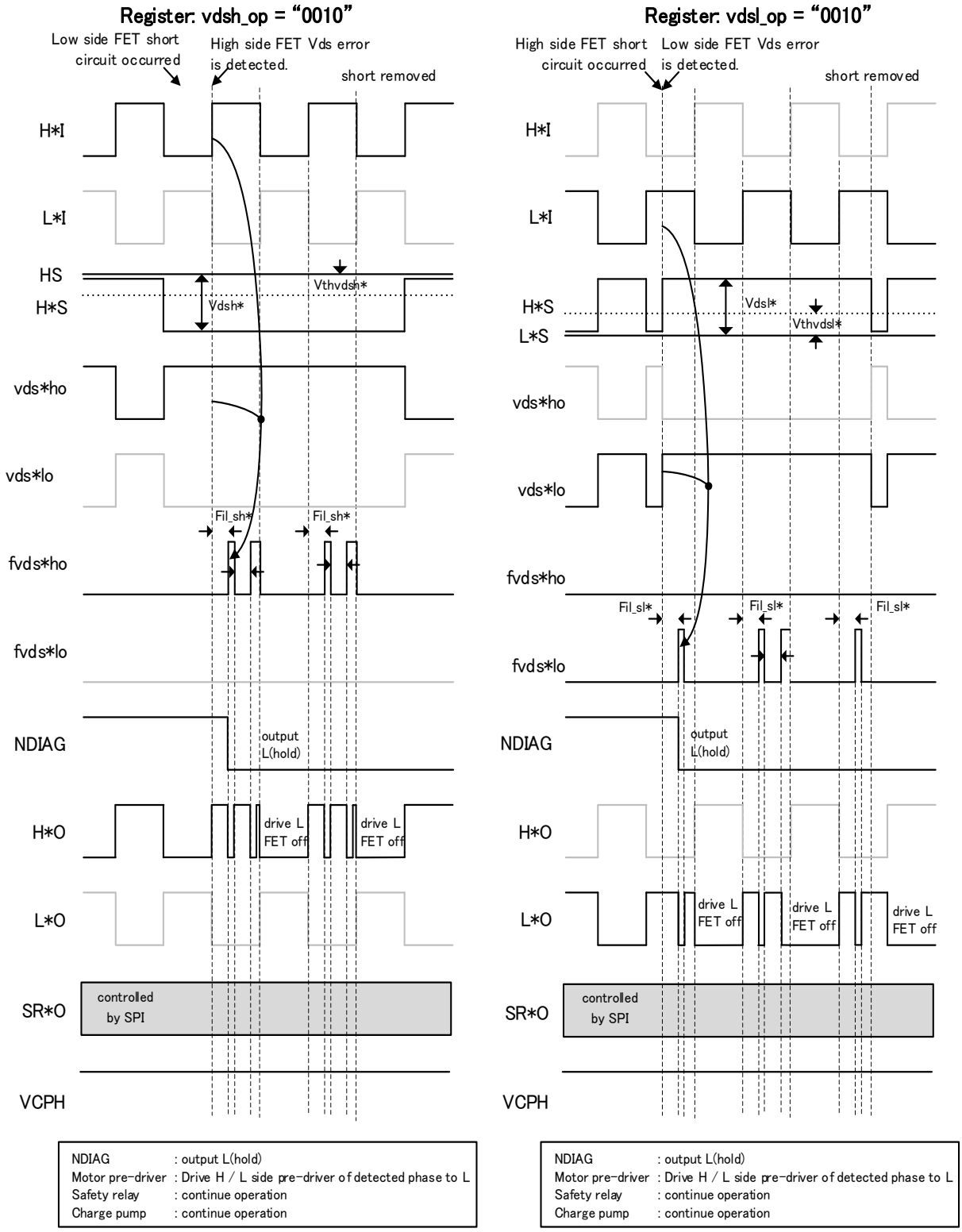


Fig. 7.5.8-d Timing chart for short-circuit detection (register vdsl_op = vdsh_op "0010")

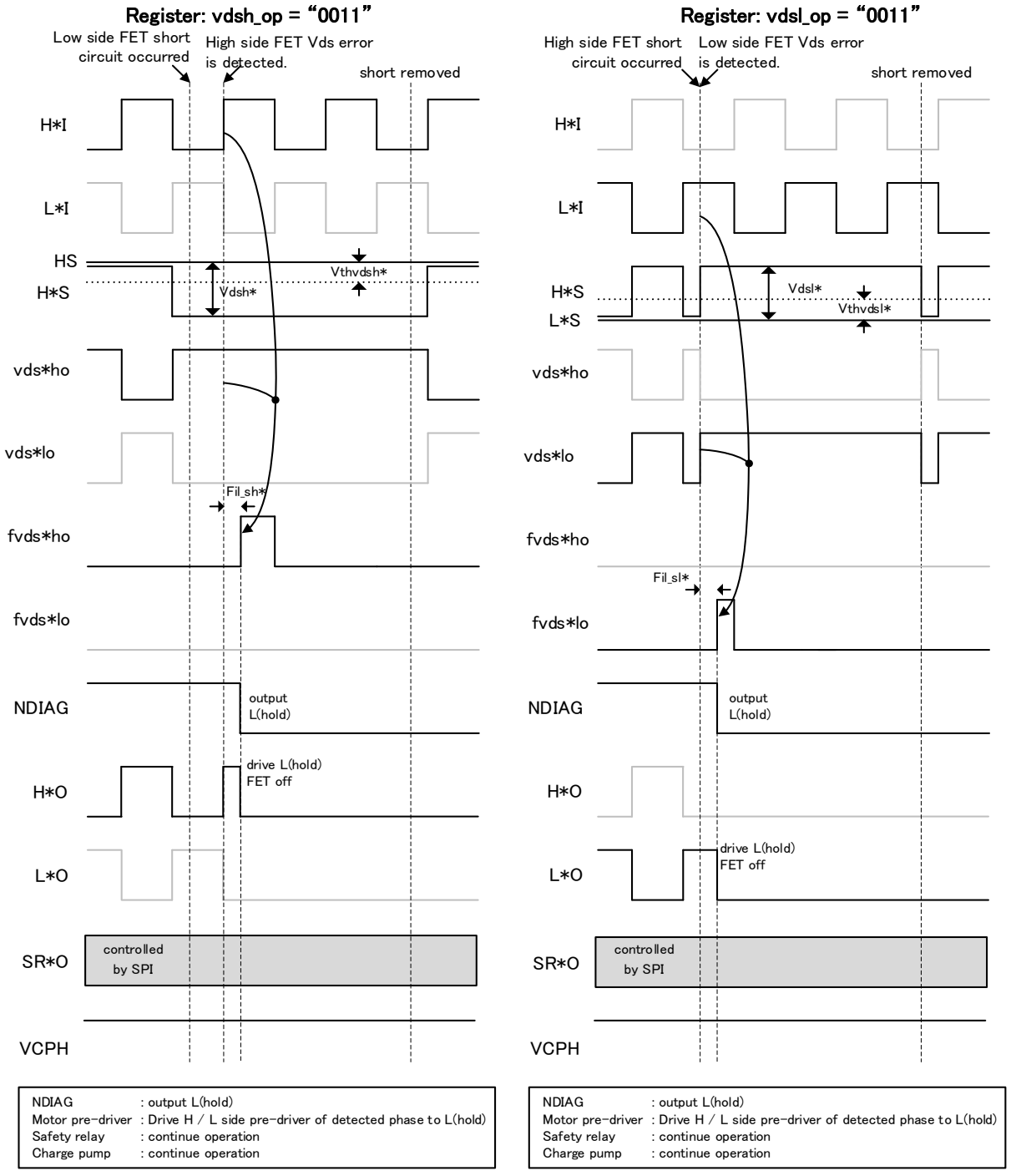


Fig. 7.5.8-e Timing chart for short-circuit detection (register vdsl_op = vdsh_op “0011”)

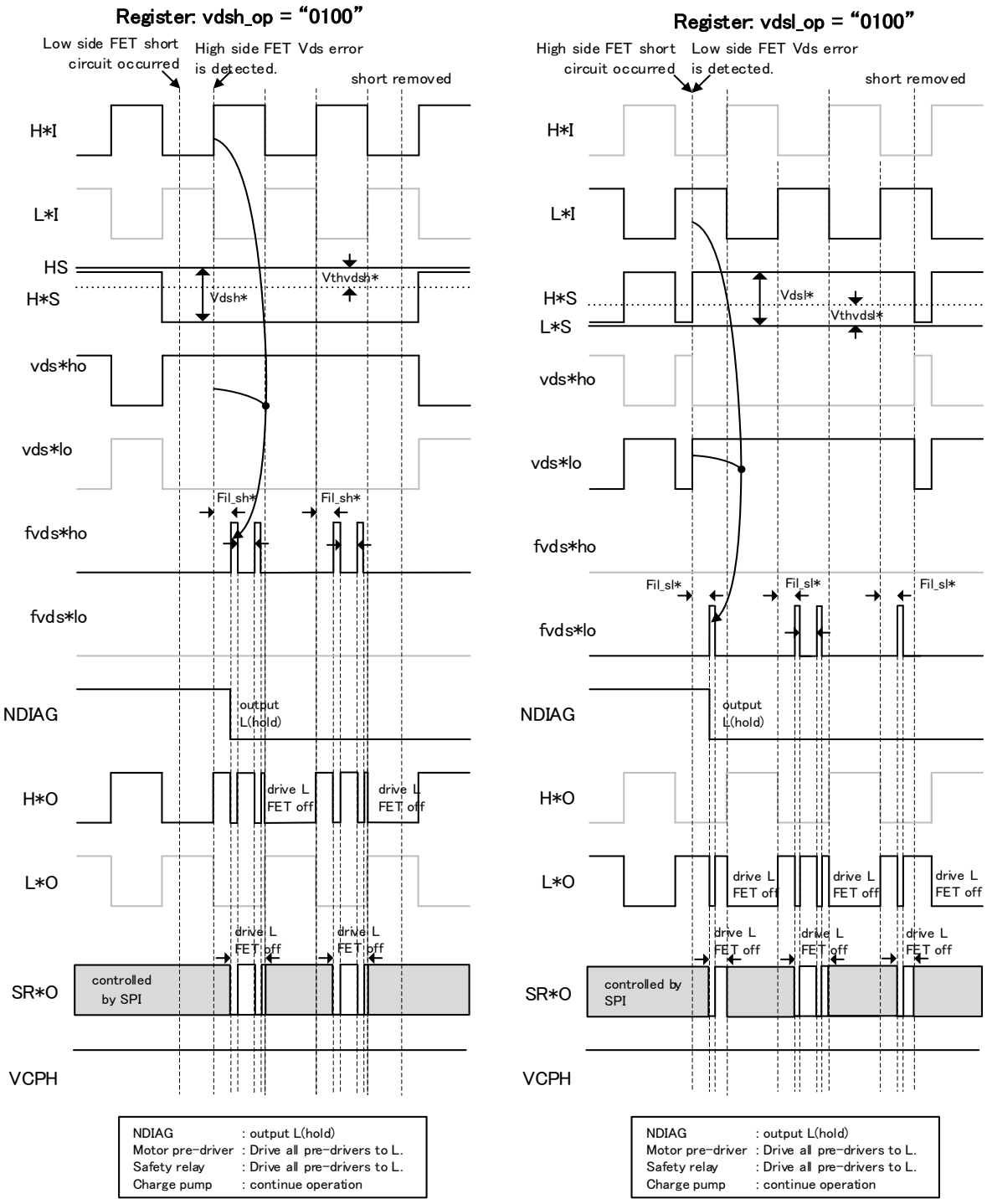


Fig. 7.5.8-f Timing chart for short-circuit detection (register vdsl_op = vdsh_op “0100”)

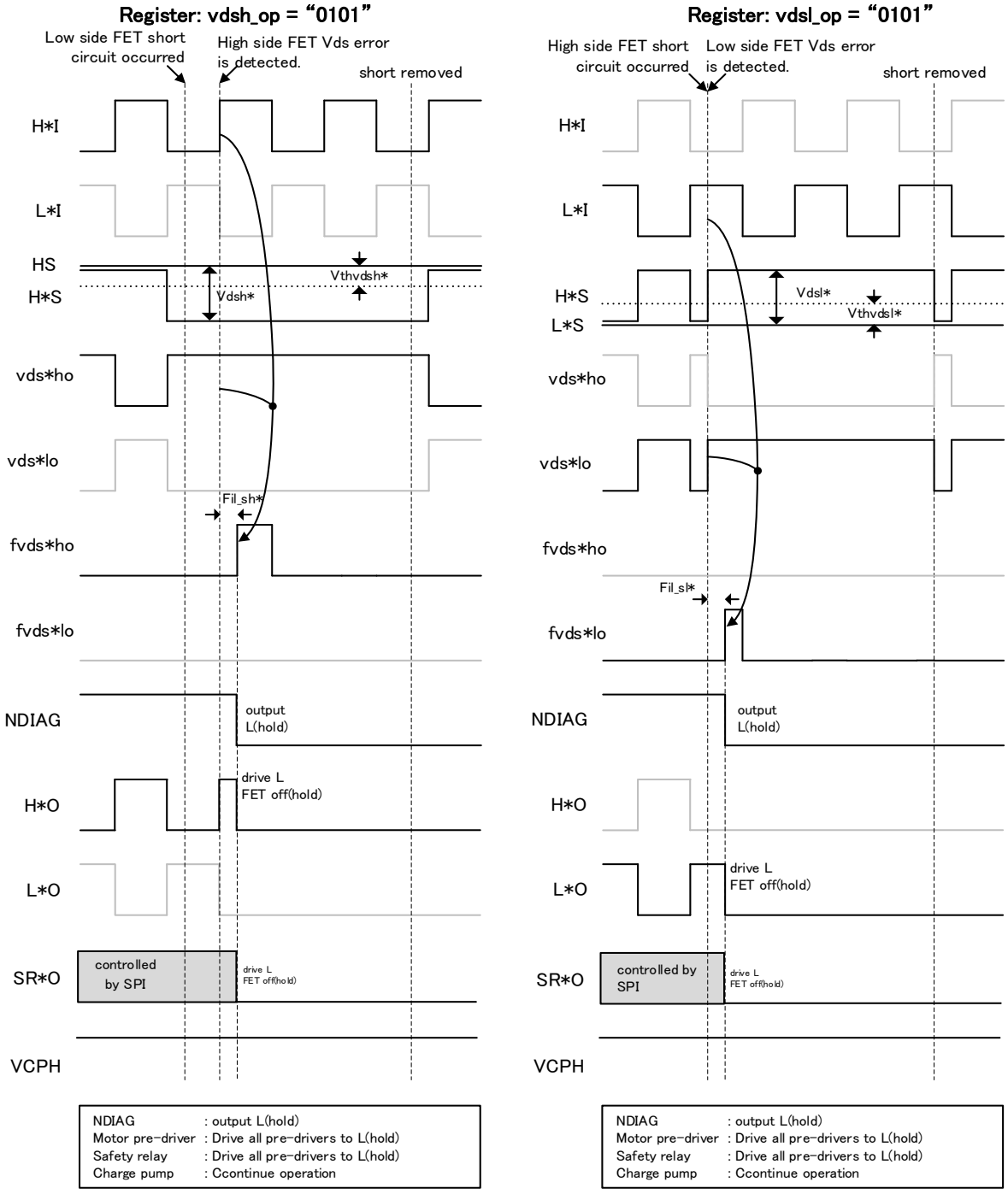


Fig. 7.5.8-g Timing chart for short-circuit detection (register vdsl_op = vdsh_op “0101”)

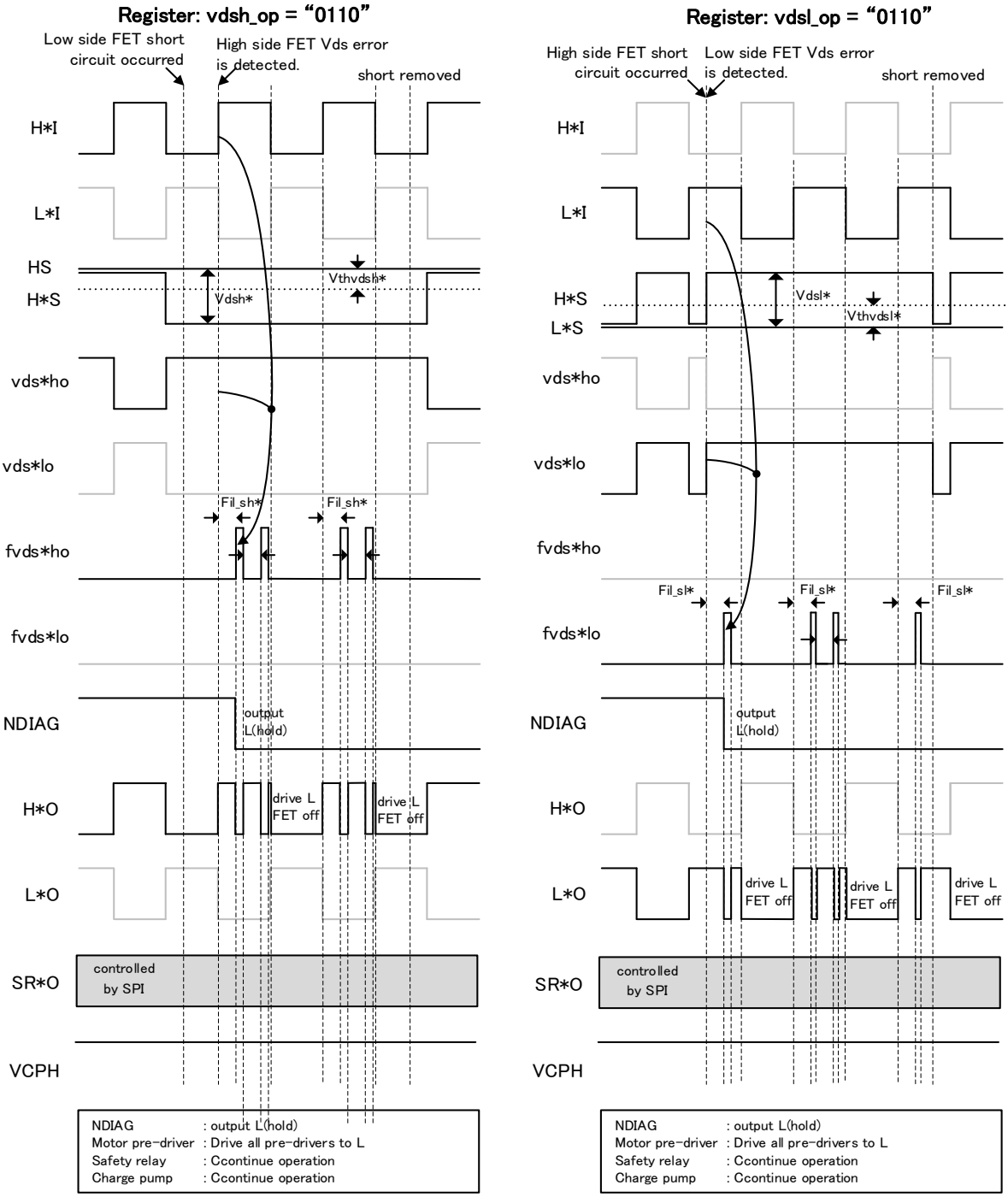


Fig. 7.5.8-h Timing chart for short-circuit detection (register vdsl_op = vdsh_op “0110”)

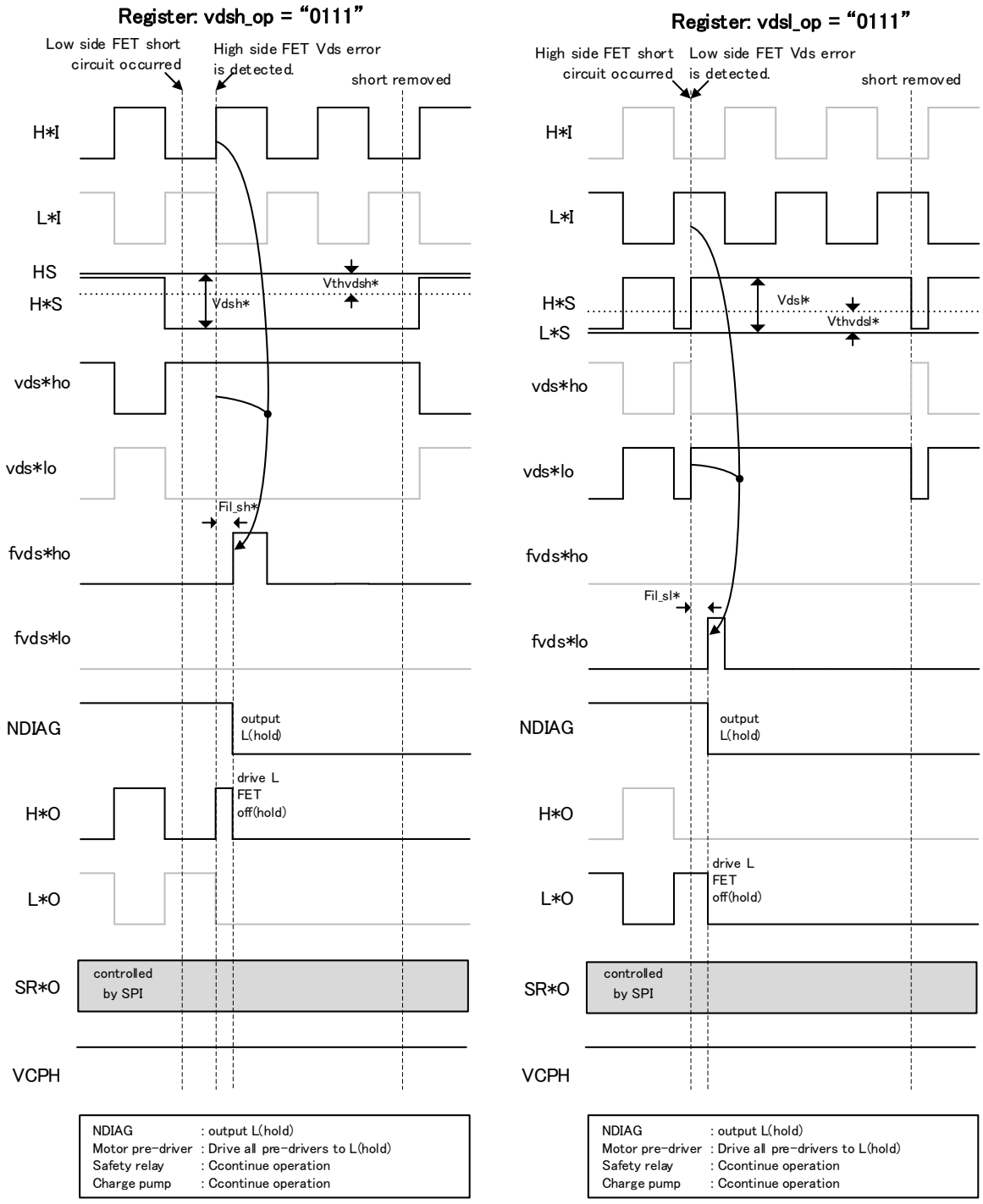


Fig. 7.5.8-i Timing chart for short-circuit detection (register vdsl_op = vdsh_op "0111")

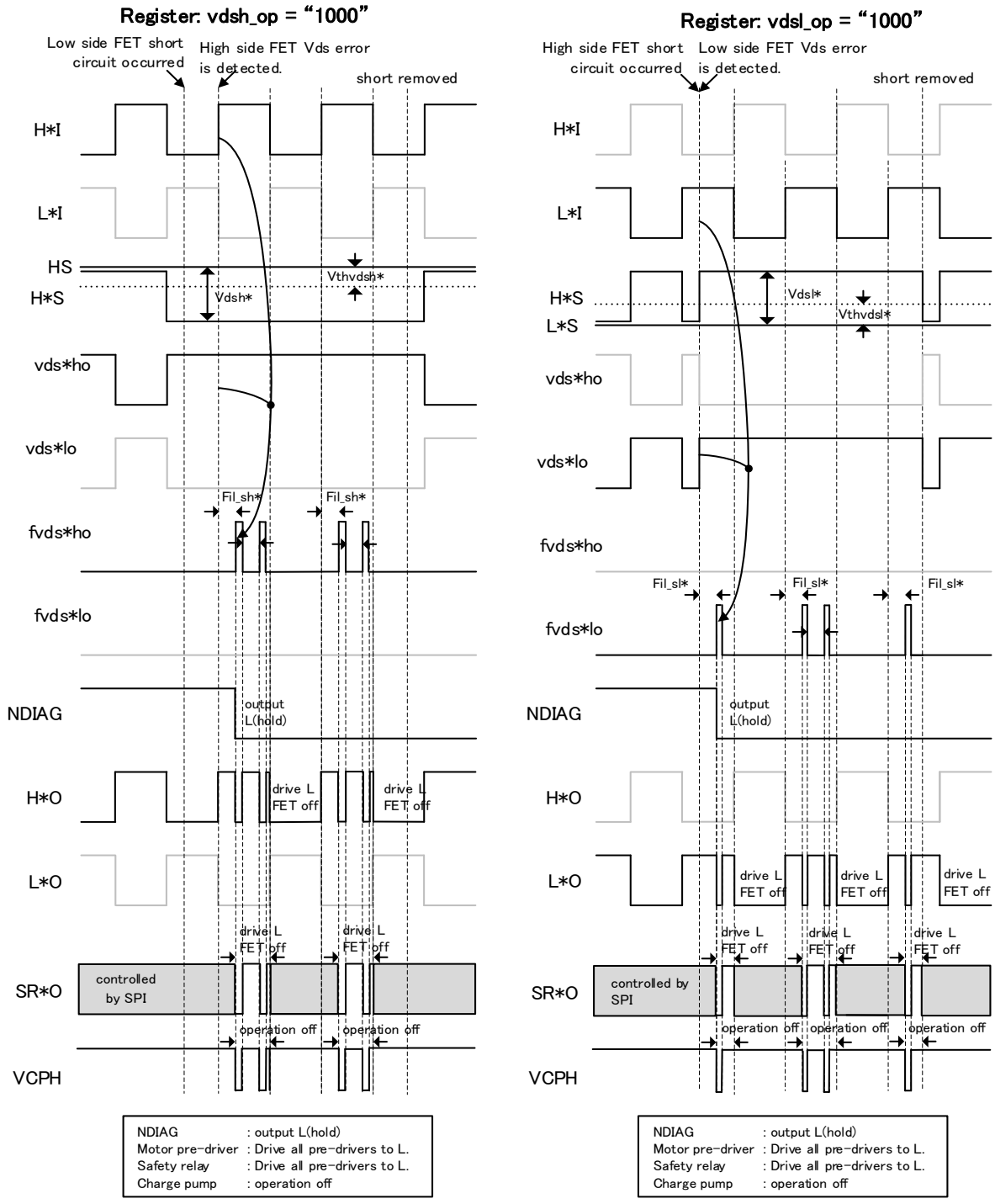


Fig. 7.5.8-j Timing chart for short-circuit detection (register vdsl_op = vdsh_op “1000”)

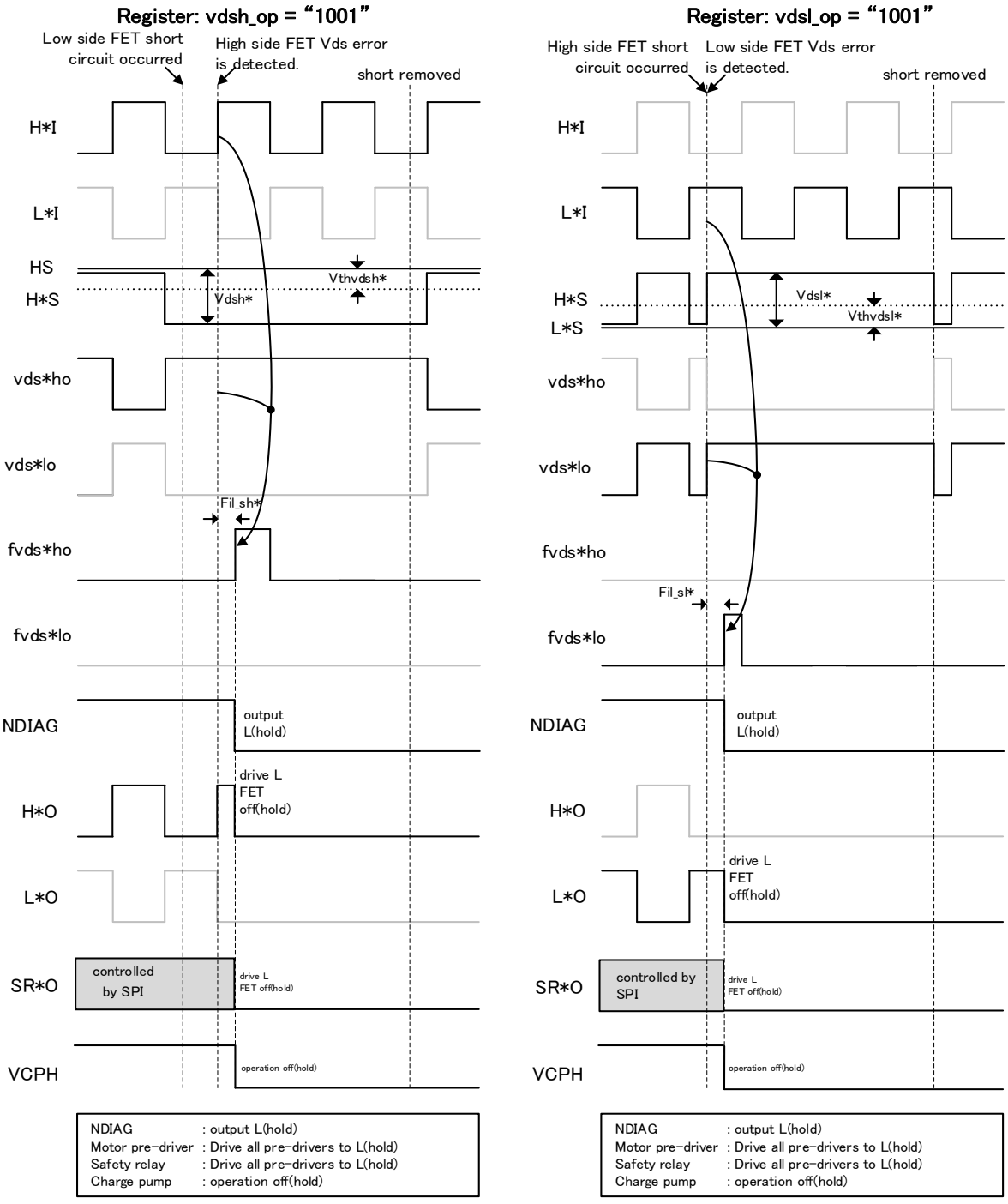


Fig. 7.5.8-k Timing chart for short-circuit detection (register vdsl_op = vdsh_op “1001”)

7.5.9. External MOSFET VGS overvoltage detection

The external MOSFET gate and source terminals are monitored for VGS in excess of the specified threshold. VGS overvoltage detection is applied to each external MOSFET separately.

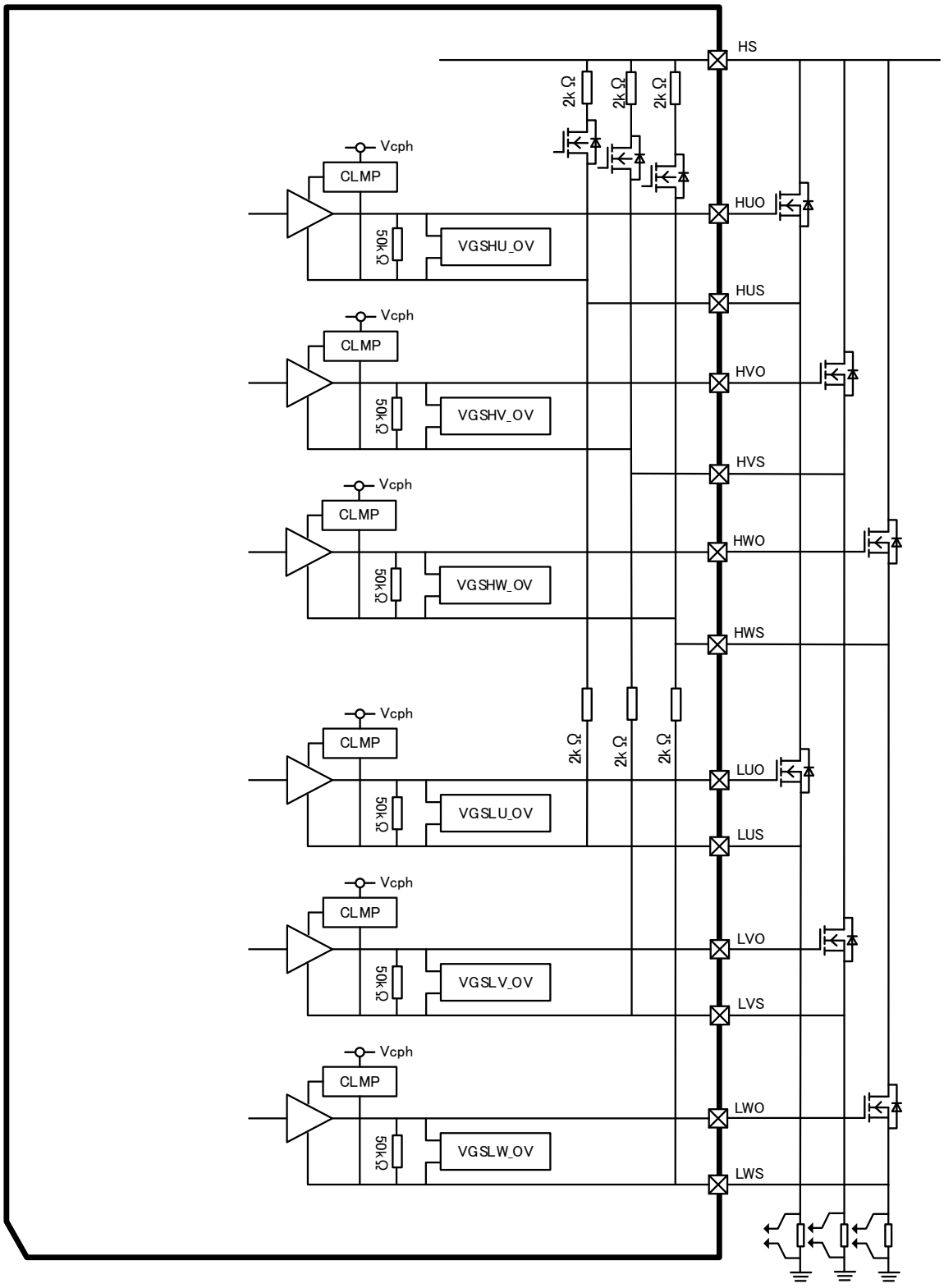


Fig. 7.5.9-a Block diagram for VGS overvoltage detection

The response to VGS overvoltage is specified via the FET_OPSEL register. Power cannot be cut from pre-drivers on individual channels; however, switching the charge pump off will shut off the power to the pre-drivers. Overvoltage threshold values can be specified for individual channels using different reference voltages to VBG1 and VBG2. Up to six VGS overvoltage detection events can be viewed in the STAT2 register. The FET_DET_SEL register is used to enable/disable VGS overvoltage detection on each channel.

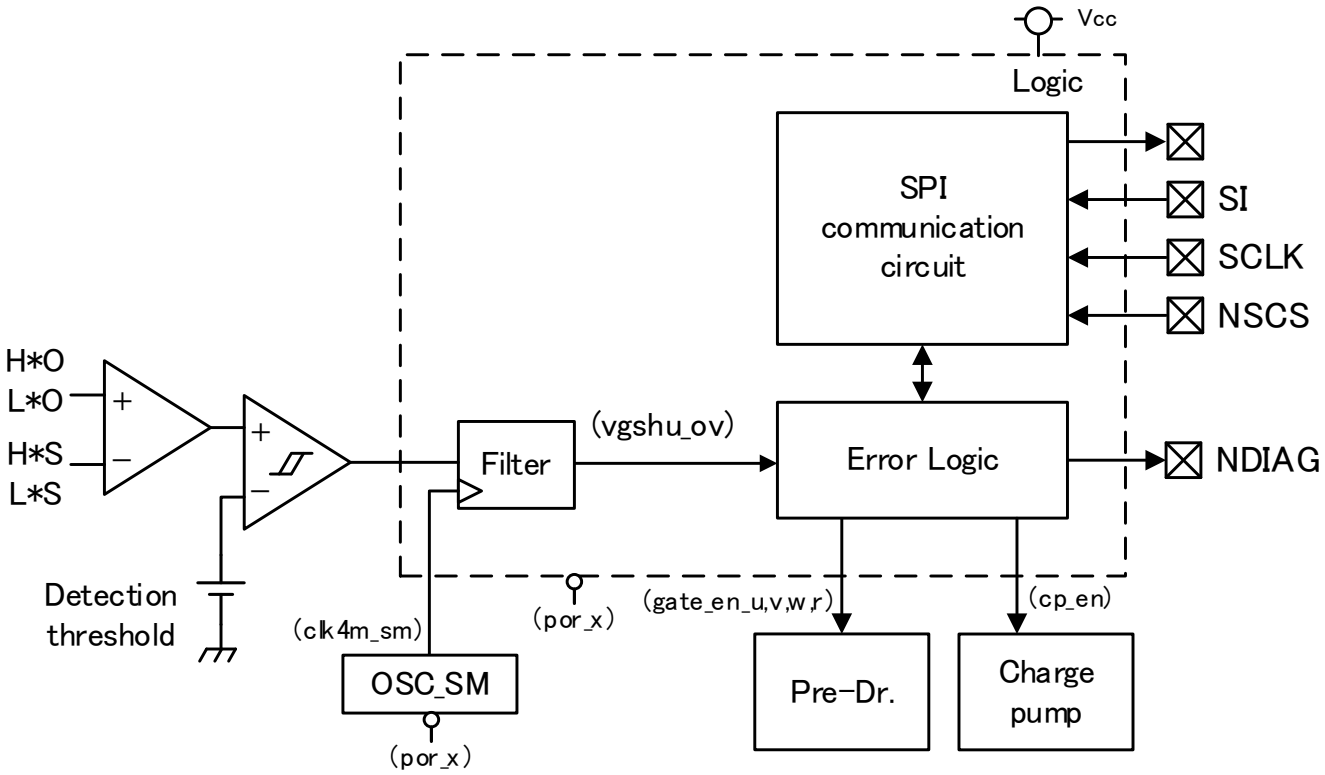


Fig. 7.5.9-b VGS overvoltage detection circuit diagram

➢ ①② VGS overvoltage detected

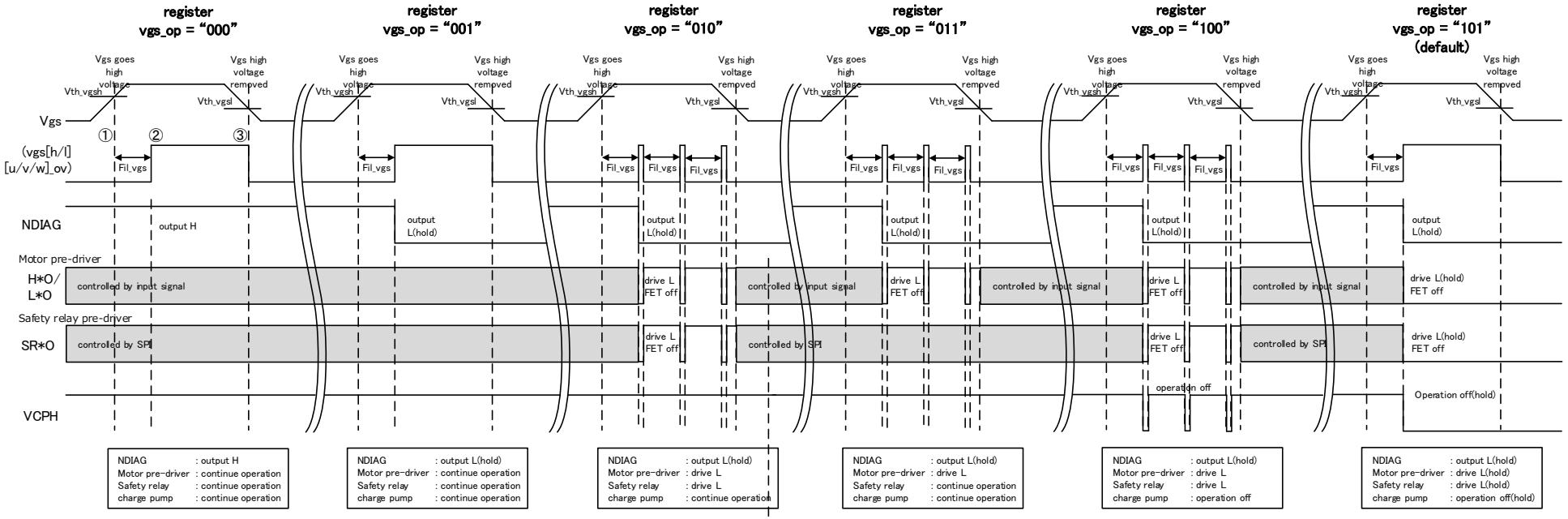
When VGS voltage exceeds Vth_vgsh, VGS overvoltage signal (vgs[h/l][u/v/w]_ov) "H" is generated after the filter time Fil_vgs has elapsed. NDIAG output is "L," except where register vgs_op is "000," in which case the VGS overvoltage is ignored, NDIAG remains at "H" and all circuits continue to operate as normal. At this point one of six operating modes can be selected via the SPI. Note that if the overvoltage response mode register is modified during an overvoltage event, changes will not take effect until the VGS overvoltage has been cancelled and register vgs_[u/v/w][h/l] has been cleared.

➢ ③ VGS overvoltage cancelled

Once the VGS voltage drops below Vth_vgsl, the VGS overvoltage signal (tvgs[h/l][u/v/w]) changes to "L" and the overvoltage is cancelled.

When register vgs_op is "101," the charge pump and pre-drivers remain off after the overvoltage is cancelled and NDIAG remains at "L."

When register vgs_op is "001", "010", "011" or "100," the charge pump and pre-drivers operate normally but the status register is retained and NDIAG remains at "L."



When register vgs[h/l][u/v/w]_ov is cleared via the SPI, NDIAG changes to "H."

During an overvoltage, register vgs[h/l][u/v/w]_ov cannot be cleared and NDIAG output is "L."

Fig. 7.5.9-c Operational chart for VGS overe detection

7.5.10. Two-way internal oscillator frequency monitoring

Each of the two internal oscillators OSC_IF and OSC_SM monitors the other's oscillation frequency. If the OSC_IF frequency is found to be 1/$K_{freqdet}$ or more below the OSC_SM frequency, the err_uf register is set; if the OSC_IF frequency is $K_{freqdet}$ or more above the OSC_SM frequency, the err_of register is set. The OSC_IF and OSC_SM frequencies are monitored at all times except during BIST.

The ferr_op register offers a choice of six modes for the action taken in response to a frequency error. See Table 7.5-a for details. Modifications to the ferr_op register made during a frequency error event will be registered but will not be enabled until the frequency error has been cancelled and the err_of/err_uf register has been cleared.

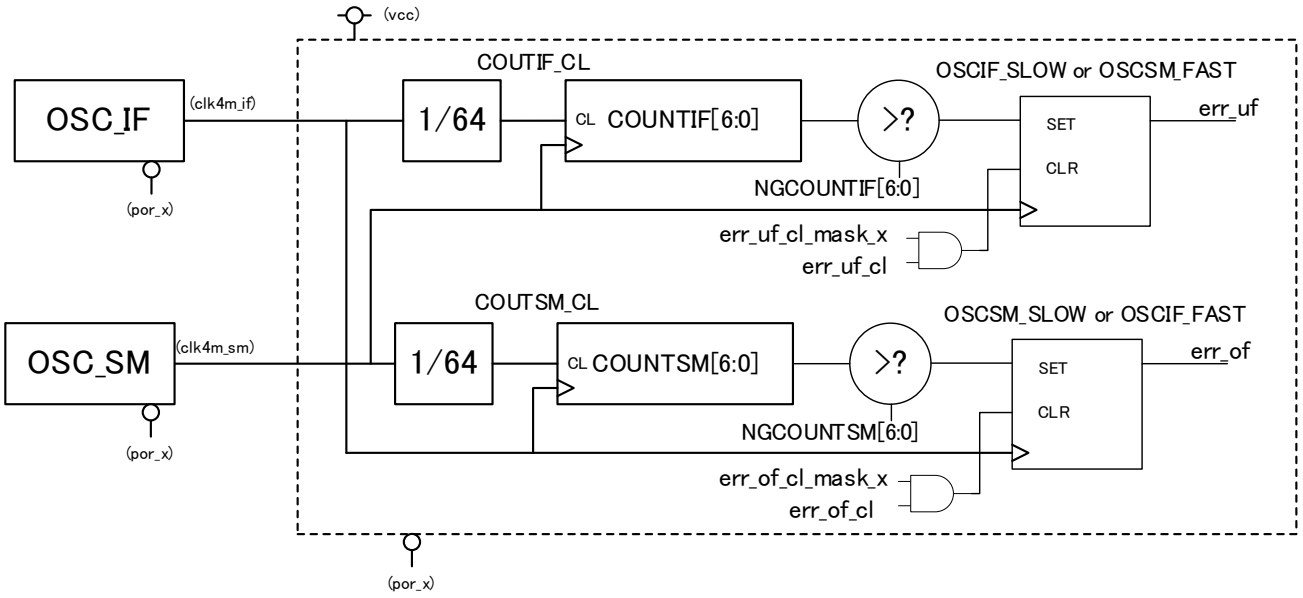


Fig. 7.5.10-a Circuit diagram for two-way internal frequency monitoring

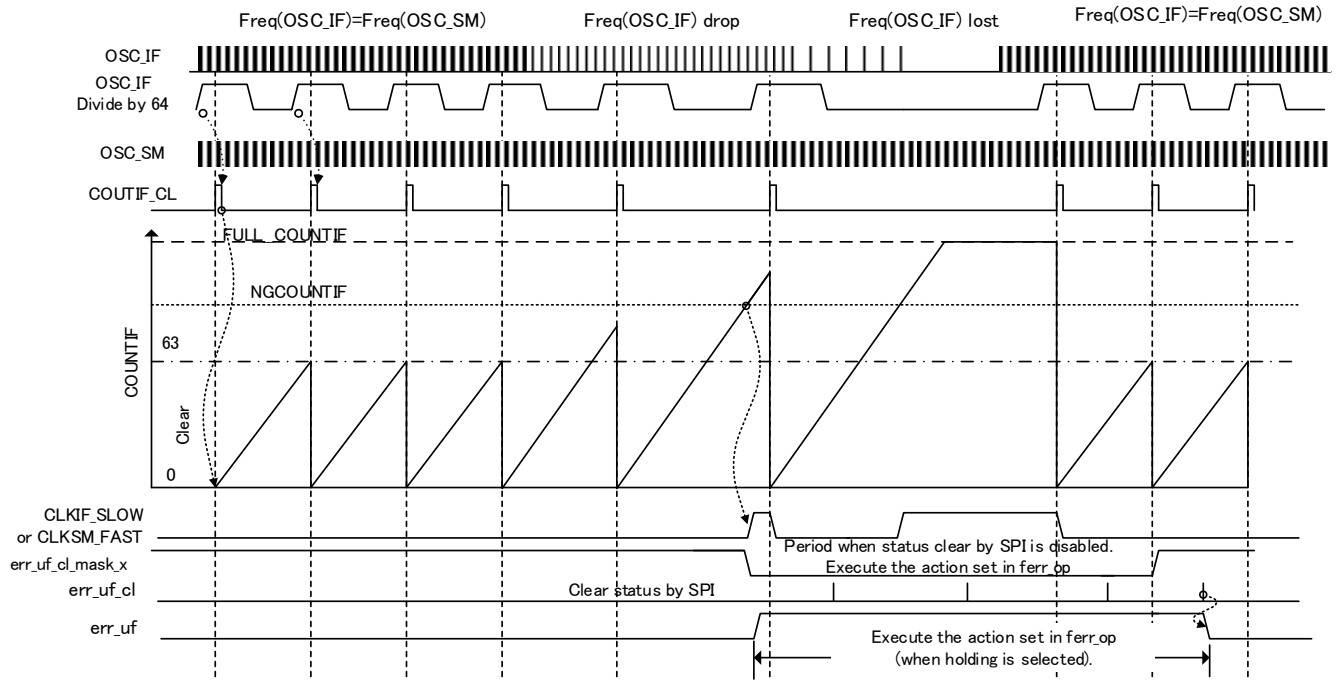


Fig. 7.5.10-b Timing chart for two-way internal frequency monitoring — Part 1

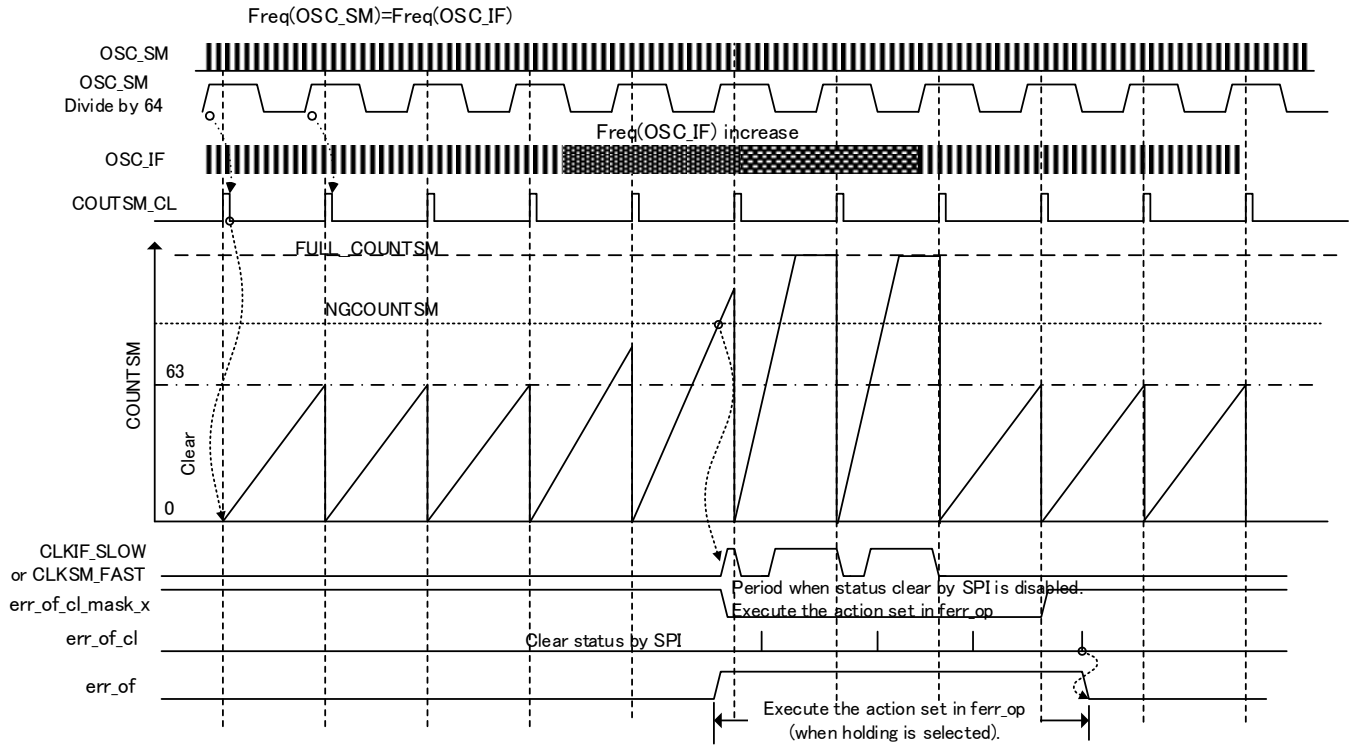


Fig. 7.5.10-c Timing chart for two-way internal frequency monitoring — Part 2

When ferr_op is 000, oscillator frequency detection is disabled.
When ferr_op is any other value, err_of status will be set if the OSC_IF frequency is Kfreqdet or more above the OSC_SM frequency, and err_uf status will be set if the OSC_IF frequency is 1/Kfreqdet or more below the OSC_SM frequency. The NDIAG terminal changes to "L" for both err_uf and err_of statuses. NDIAG can be restored to "H" by clearing the status register. Note that the status register can only be cleared when the most recent frequency comparison shows the OSC_IF frequency within the required range (no higher than Kfreqdet and no lower than 1/Kreqdet).
When ferr_op is 010 and the frequency is outside the required range, pre-drivers and relay output are switched off.
When ferr_op is 011 and the frequency is outside the required range, pre-driver outputs are switched off.
When ferr_op is 100 and the frequency is outside the required range, pre-drivers, relays and the charge pump are switched off.
When ferr_op is 101 and there is a status register set, pre-drivers, relays and the charge pump are switched off.

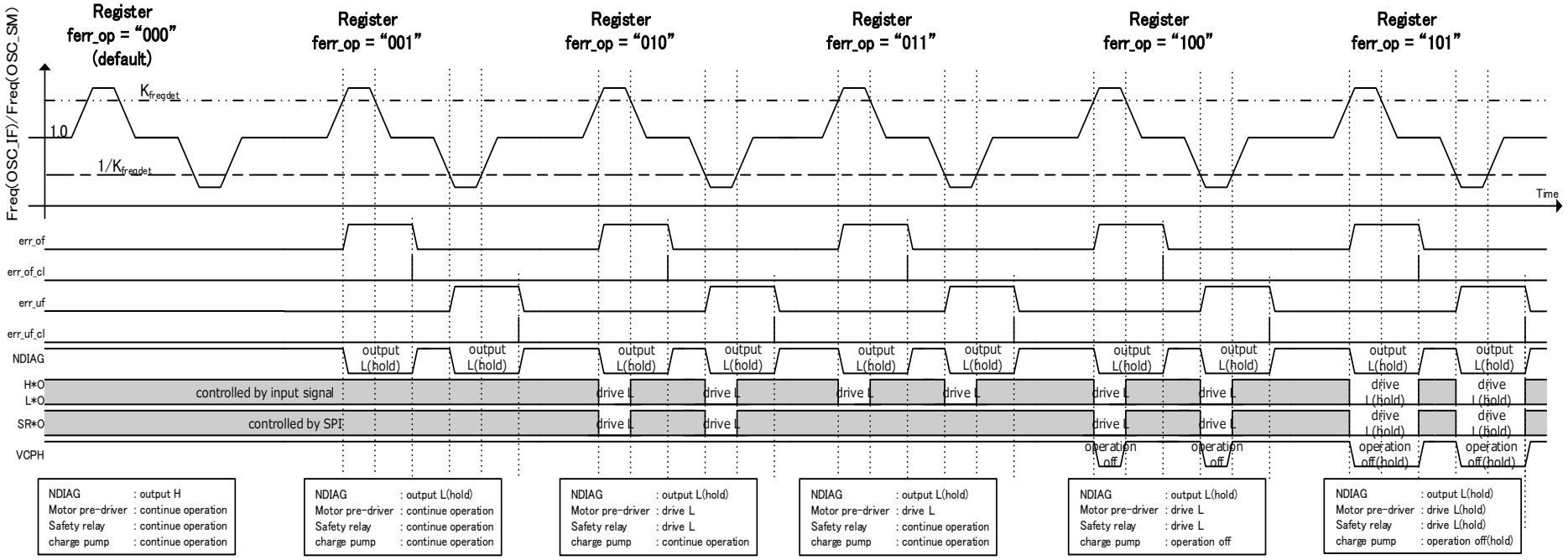


Fig. 7.5.10-d Operating modes in the event of a frequency error

7.5.11. QA detection

The SPI communication block is equipped with a QA detection feature. Refer to Section 7.9.2 and Table 7.5-a for details

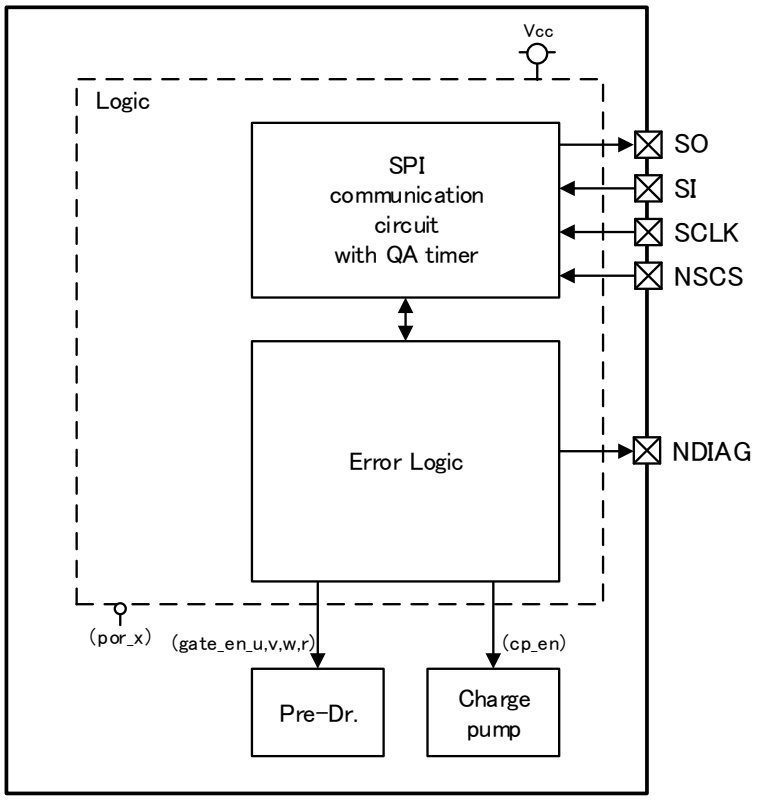


Fig. 7.5.11-a Block diagram for QA detection

➢ I-① QA operation error detection

When a QA operation error is detected, register err_qa changes to "H" and NDIAG changes to "L." If a QA timeout is detected, register err_qato changes to "H" and NDIAG is "L."

➢ I-② QA error cumulative detection

When a cumulative QA error is detected, register err_qac changes to "H" and the action specified in register qat_op is executed.
At this point there are four operating modes that can be selected via the SPI.

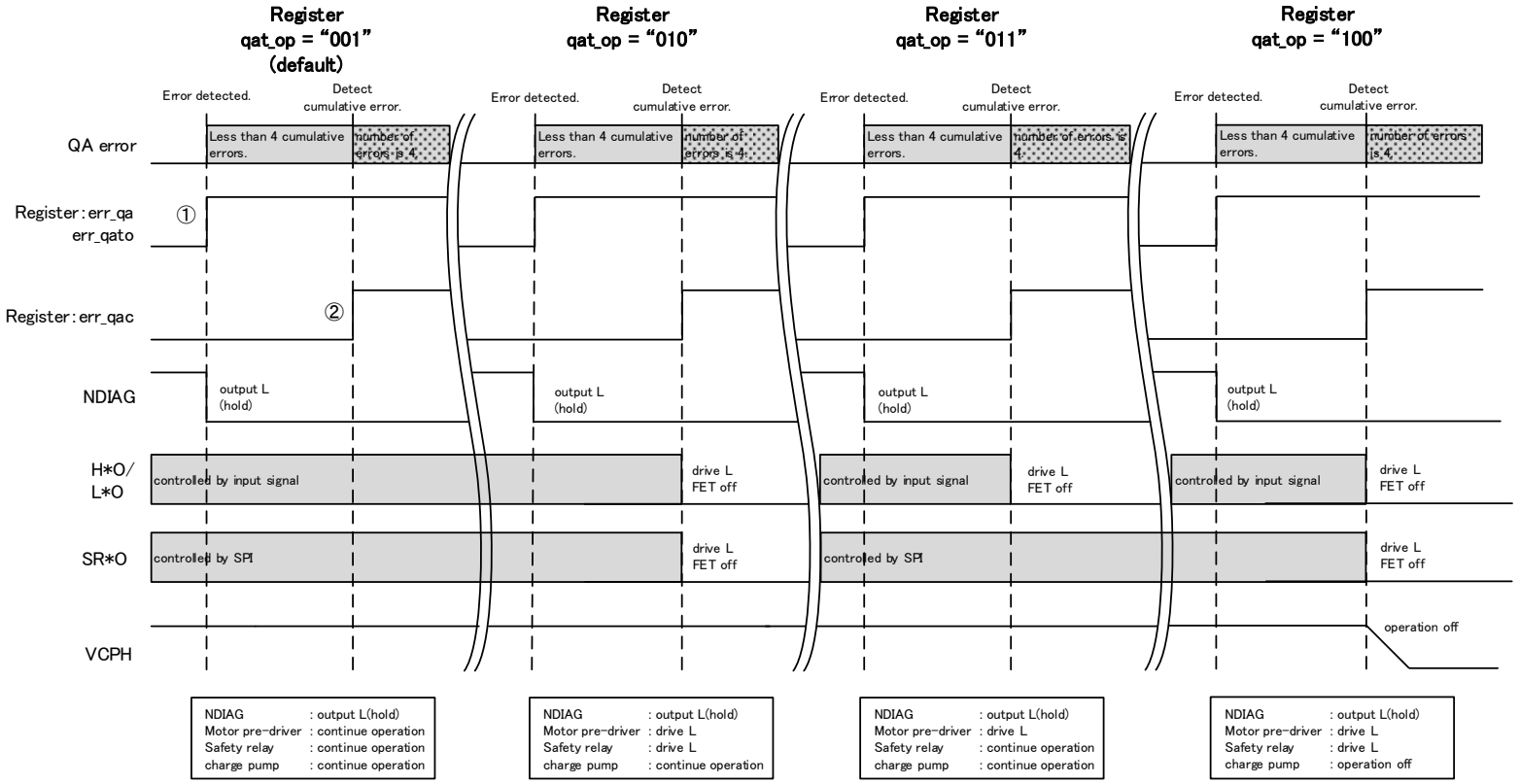


Fig. 7.5.11-b Timing chart for QA error detection

7.6. ALARM input circuit

The ALARM terminal is reserved for microcomputer pre-driver shut down commands. The ALARM signal is an internal signal using either OSC_SM or OSC_IF that is used to enable and disable motor drive and safety relay pre-driver circuits.

- When ALARM is "L," pre-driver circuits specified in the ALM_CTRL register are disabled.
- When ALARM is "H," pre-driver circuit input and internal signal can be used for enable/disable operations.
- The input side of the ALARM terminal is equipped with a digital filter (D.F.) to filter out noise.
- The digital filter time can be enabled in the ALM_CTRL register.
- OSC_SM signals are the only alm_det details in the ALARM detection status STAT1 register that can be accessed through the SPI.

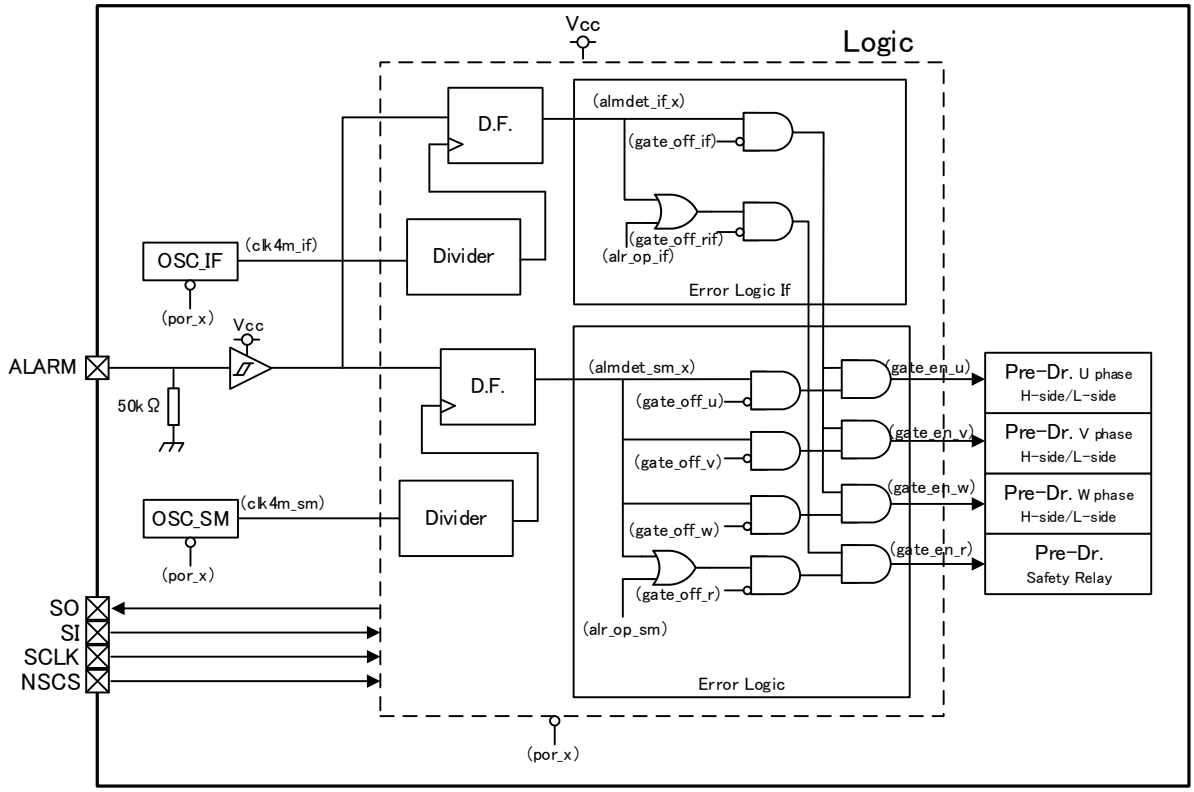


Fig. 7.6-a MOSFET drive circuit control block diagram

Table 7.6-a Truth table for MOSFET driver controller

por_x	alr_op	almdet_if_x	almdet_sm_x	gate_en_u	gate_en_v	gate_en_w	gate_en_r
L	*	*	*	L	L	L	L
		L	*	L	L	L	L
		*	L	L	L	L	L
	L	H	H	to gate_off_u	to gate_off_v	to gate_off_w	to gate_off_r
		L	*	L	L	L	to gate_off_r
		*	L	L	L	L	to gate_off_r
H	H	H	H	to gate_off_u	to gate_off_v	to gate_off_w	to gate_off_r

Note

- * denotes "don't care"
- The gate_off_u, gate_off_v, gate_off_w and gate_off_r commands are used to stop pre-drivers for reasons other than an alarm
- The gate_off_if and gate_off_rif commands are used to stop pre-drivers for reasons other than an alarm (frequency error detection using OSC_IF)

7.7. ABIST/LBIST

ABIST/LBIST performs a diagnosis at IC startup to check that error detection functions are working normally.

• At IC startup, oscillator circuits start after a VCC undervoltage has been cancelled and the ABIST diagnosis begins after LBIST is finished.

• If LBIST returns a NG result, the ABIST diagnosis is cancelled and the charge pump and pre-drivers are disabled.

• Once ABIST starts, turning on the diagnosis switch toggles the comparator input voltage and inverts the detection comparators.

• The diagnosis is synchronized to the clock. Diagnostic data is input to the ABIST evaluation circuit. NDIAG remains at "L" while the diagnosis is in progress.

• When the diagnosis process is completed, the IC switches to normal operation.

• If no errors are detected during diagnosis, NDIAG changes to "H."

• If errors are detected, NDIAG remains at "L" and the diagnostic data is retained.

• Table 7.5-a lists the diagnostics points.

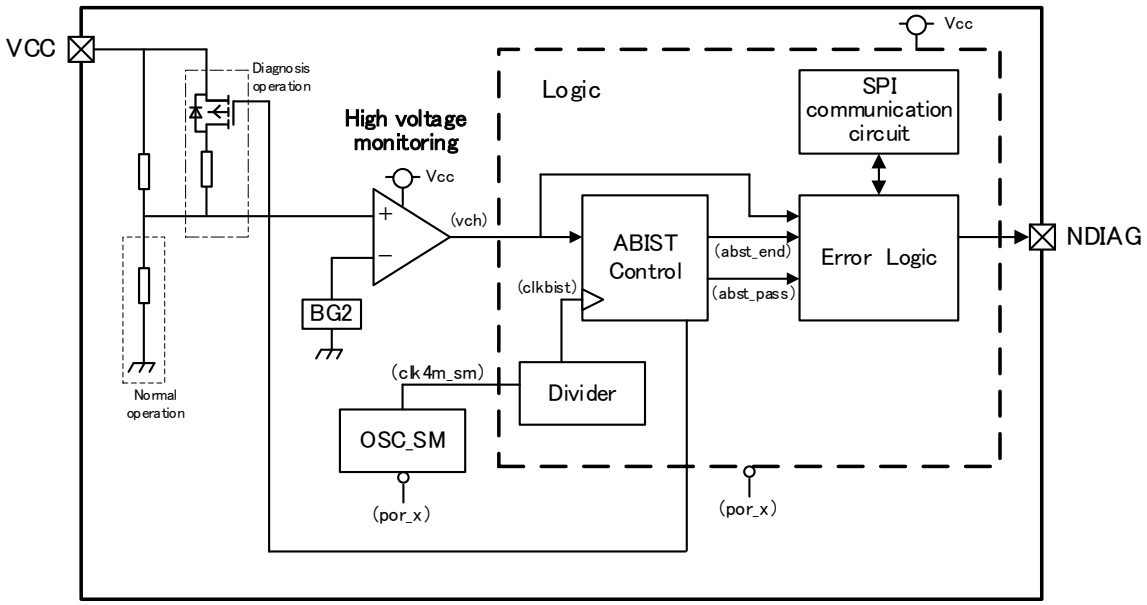


Fig. 7.7-a ABIST block diagram (VCC overvoltage detection)

Since the en_cp bit in the CP_RLY_CTRL register has a default value of 1, the charge pump is enabled when ABIST finishes normally.

Table 7.7-a Truth table for charge pump circuit operations

ABIST	ABSIT results	Abnormalities other than ABSIT are detected.	en_cp [SPI]	Internal signal cp_en	Charge pump circuit
Before ABIST	*	*	*	L	Disable
During ABIST					
After ABSIT	NG				
	OK	TRUE			
		FALSE	L		
			H	H	Enable

Note: Vcph = Vb during ABIST/LBIST since due to influence of internal pull-up/pull-down resistors

Table 7.7-b Truth table for pre-driver circuit operations

ABIST	ABSIT results	Abnormalities other than ABSIT are detected.	Internal signal gete_en_u/v/w	Pre-driver circuit
Before ABIST	*	*	L	Disable
During ABIST				
After ABSIT	NG			
	OK	TRUE		
		FALSE	H	Enable

< ABIST Overall operation/Start-up operation>

➢ ① IC launch

When the IC is launched, as the low voltage of Vcc is released, the divider circuit starts to operate.

➢ ② LBIST execution

The divider circuit starts to operate, starting LBIST.

➢ ③ ABIST launch

After LBIST, ABIST is started. By switching detection comparators periodically, it diagnoses whether the detection comparators correctly output fault detection signals.

➢ ④ Diagnosis

Judgment on the respective comparator below is made.

VB low voltage, VCPH high voltage, VCC high voltage, VCC_OP low voltage, VCC_OP high voltage, overtemperature.

➢ ⑤ ABIST shut-down

When the diagnosis is completed on the all comparators, the IC switches to the normal operation mode, the charge pump circuit starts operating, and the pre-driver circuit can be turned on. And the diagnosis result is output to NDIAG.

When the diagnosis result is NG, the charge pump circuit and pre-driver circuit remain "off."

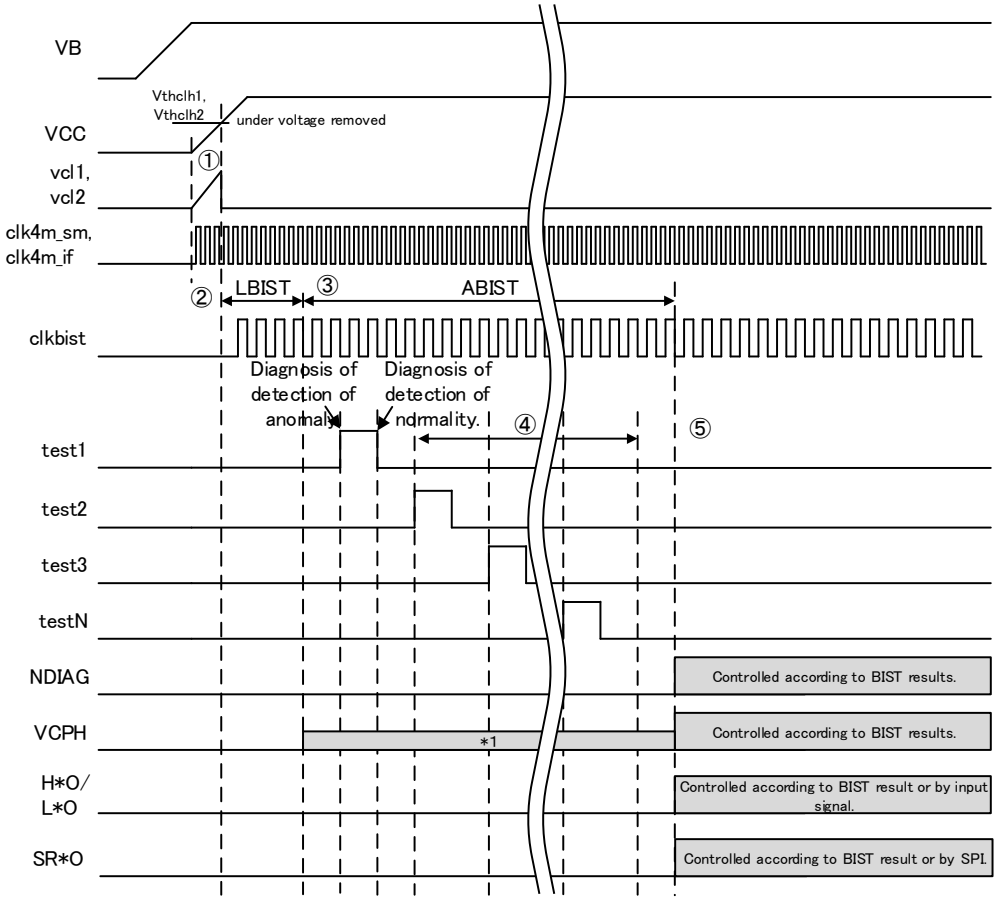


Fig. 7.7-b ABIST timing chart

Note

・Dependent on the internal pull-up/down resistance while ABIST / LBIST is being executed, and Vcph=Vb.

・There is no starting sequence for VB and VCC. If VB undervoltage detection and VCC_OP undervoltage detection are not released at the start of ABIST, the ABIST result will be abnormal.

Slew rates of Vb and Vcc should be within the ranges below.

Vb= less than 8V/μs

Vcc= less than 0.3V/μs

・The execution period of LBIST and ABIST combined is about 2.6ms (typ.), 4.0ms(max). Start SPI communication after LBIST and ABIST are completed.

7.8. Initial diagnosis circuit for external FETs and relays

7.8.1. Block diagram

Fig. 7.8-a shows the block diagram (this is a conceptual diagram and not a practical circuit). An inspection circuit (FET_TEST block) is fitted for executing the initial diagnosis on the external FETs and relays. During the inspection, VDS abnormality detection is disabled and the circuit for detecting VDS abnormality is used for inspecting external FETs and relays (FET_TEST hereafter). Even during FET_TEST, when a "pre-driver off" instruction appears (when gate_en_*="L") for reasons other than VDS abnormality detection, the pre-driver is turned off. During the FET_TEST period, pre-driver control signals for motor control is controlled by the FET_TEST block. Relays always follow CP_RLY_CTRL register setting.

The resistors to maintain HUS, HVS, HWS terminals to the mid-voltage when the pre-drivers are off are connected while an inspection by FET_TEST is being executed.

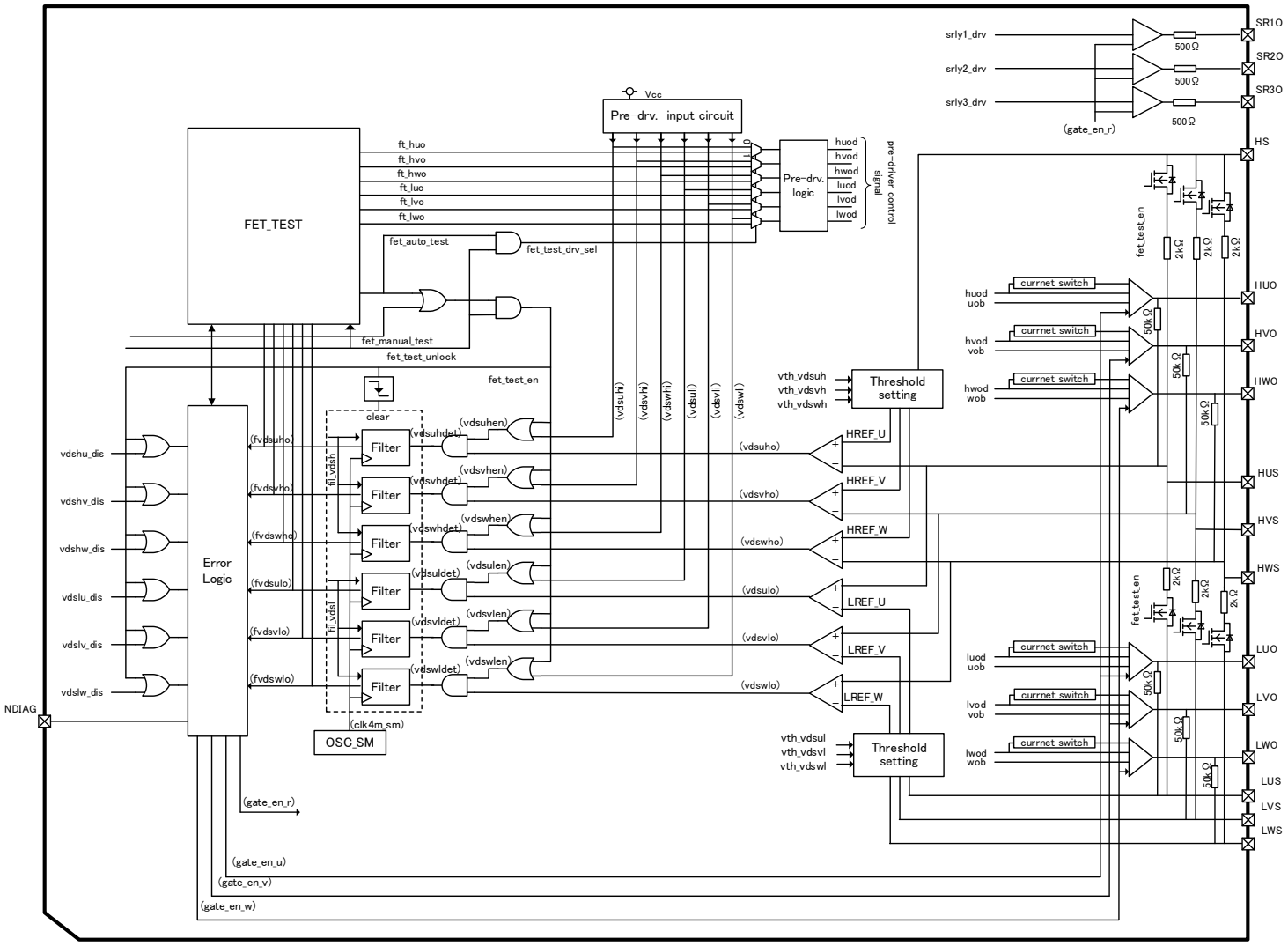


Fig. 7.8-a Block diagram of the diagnosis circuit for external FETs and relays

7.8.2. Classification of inspection modes

Table 7.8-a shows a list of inspection modes. When fet_test_unlock=0, it provides normal operation.

By setting fet_manual_test = 1 during the period of fet_test_unlock = 1, the external FET can be inspected manually. In this mode, relay drive signals are controlled by the register, FET drive signals are controlled by the input terminal, and the control method is the same as in the normal operation. In normal operation, the VDS detection comparator output is input to the noise filter only for the channels where the FET control input terminal is controlled to "H", but in the manual test mode, the comparator output for VDS detection is input to the noise filter regardless of the state of the input terminal for FET control. In manual test mode, VDS detection is disabled because the VDS detection circuit is used for FET inspection. fet_rmidonU, fet_rmidonV, fet_rmidonW are the control bits to set U phase, V phase and W phase of the mid-voltage generating resistors to ON, respectively. Set each bit to ON depending on the inspection method that the user assumes. When multiple bits are turned ON simultaneously, resistors of the corresponding phases are turned ON simultaneously. The inspection is through expectation comparison by the microcomputer that reads the comparator output (after being filtered) for VDS detection from the VDS_COMP_STAT register.

By setting the fet_test_start bit while fet_test_unlock=1, an inspection sequence is started, and when fet_auto_test="H," timing control of FET drive and saving of the output results of VDS detection comparators are performed by this IC automatically. The FET drive patterns are previously assumed pre-defined drive patterns for Type A, B and C, but for Type D, arbitrary patterns can be set by the register. Since the circuit for VDS abnormality detection is used for FET inspection, VDS abnormality detection is disabled. The resistors for generating the mid-voltage are ON for all phases while the automatic sequence is running. Since FETs are driven by previously assumed pre-defined drive patterns for Type A, B and C, the comparator output is automatically compared with expected values within the IC, but since the drive patterns can be arbitrarily set by the user for Type D, expectation comparison is conducted by the microcomputer.

When fet_manual_test and fet_auto_test become valid simultaneously, fet_auto_test is given priority. When fet_manual_test_[U,V,W] sets multiple bits simultaneously, mid-voltage generating resistors of the phases that are set to 1 are turned ON simultaneously. "*" In Table 7.8-a means Don't 'care.

Table 7.8-a List of inspection modes

<table>
<tr><th colspan="7">Register setting or status flag</th><th colspan="5">Operation of each circuit element</th><th rowspan="2">Expected value comparison.</th><th rowspan="2">Overview</th></tr>
<tr><th>fet_test_unlock</th><th>fet_auto_test</th><th>fet_manual_test</th><th>fet_rmidonU</th><th>fet_rmidonV</th><th>fet_rmidonW</th><th>fet_test_type</th><th>Relay drive signal</th><th>FET drive signal</th><th>VDS detection</th><th>VDS detection comparator (with Filter)</th><th>mid-voltage generating resistors</th></tr>
<tr><td>0</td><td>*</td><td>*</td><td>*</td><td>*</td><td>*</td><td rowspan="4">*</td><td rowspan="8">Controlled by register setting by microcomputer.</td><td rowspan="4">Controlled by input terminal.</td><td rowspan="2">Valid</td><td rowspan="2">VDS detection</td><td rowspan="2">OFF</td><td rowspan="2">–</td><td>Normal operation</td></tr>
<tr><td rowspan="4">1</td><td rowspan="3">0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>FET test unlock state.</td></tr>
<tr><td rowspan="3">1</td><td>1</td><td>0</td><td>0</td><td rowspan="3">Invalid</td><td rowspan="5">External FET diagnosis</td><td>U phase ON</td><td rowspan="3">Judgment by microcomputer.</td><td rowspan="3">Manual FET test.</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>V phase ON</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>W phase ON</td></tr>
<tr><td rowspan="4">1</td><td rowspan="4">1</td><td rowspan="4">*</td><td>A</td><td rowspan="4">Automatic control by IC.</td><td rowspan="4">All phases ON</td><td rowspan="3">Expected value comparison by IC.</td><td>Automatic FET test Type A.</td></tr>
<tr><td>B</td><td>Automatic FET test Type B.</td></tr>
<tr><td>C</td><td>Automatic FET test Type C.</td></tr>
<tr><td>D</td><td>Controlled by register setting by microcomputer.</td><td>Judgment by microcomputer.</td><td>Automatic FET test Type D.</td></tr>
</table>

7.8.3. FET manual inspection

By setting fet_manual_test to "H" in the FET_TEST_CNT1 register after setting fet_test_unlock="H" in the FET_TEST_CNT2 register, FET manual inspection can be conducted. In the FET manual inspection mode, FET control signals are controlled from input terminals as in the normal operation. The VDS abnormality detection circuit is changed to FET inspection mode, and the VDS comparator output signal is input to the noise filter regardless of the FET control input signal. Since the circuit for VDS abnormality detection is used for FET inspection, VDS abnormality detection is disabled. In addition, according to the setting of 3 bits of fet_rmidonU, fet_rmidonV, and fet_rmidonW, the U phase, V phase, and W phase mid-voltage generating resistors can be turned ON individually. When multiple bits are turned ON at the same time, the resistance of the corresponding phase is turned ON simultaneously.

By setting ft_comp_sel="H," VDS detection comparator (after being filtered) output can be read from VDS_COMP_STAT register. Have the microcomputer read these values during inspection and confirm the expected operation.

When fet_manual_test and fet_auto_test become valid simultaneously, fet_auto_test is given priority and an automatic inspection sequence is started. And Fig. 7.8-b shows a period "Normal operation," which indicates that the IC operation has exited FET_TEST mode. Please set fet_test_nulock="L" during the period of "normal operation in which actually driving a motor is intended" at the system level to prevent FET_TEST from being invoked incorrectly.

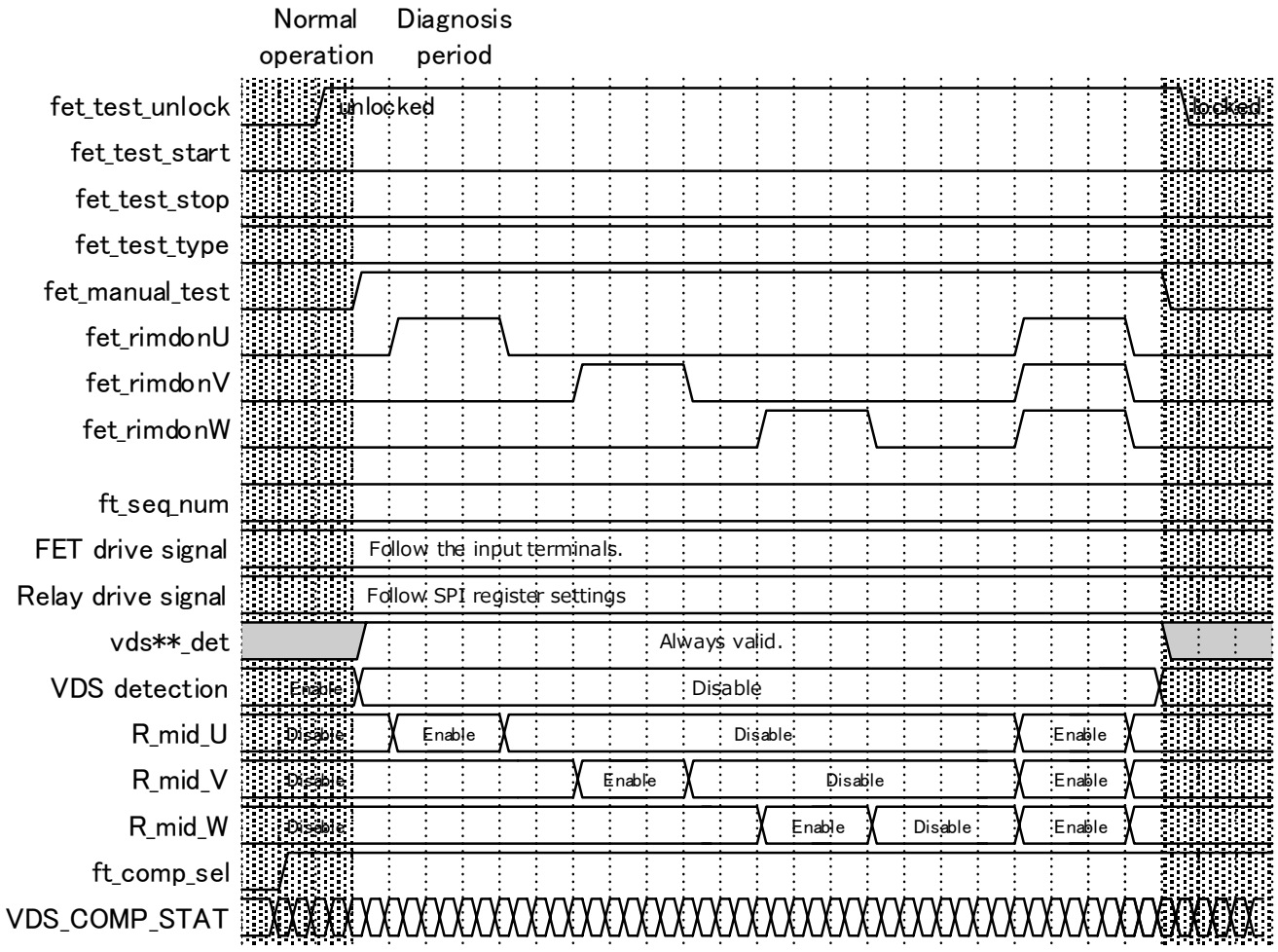


Fig. 7.8-b Operation waveforms in the manual inspection mode

7.8.4. Inspection method Type A

This type is intended to be performed while motor relays are off. Before starting inspection, set motor relays OFF by the CP_RLY_CTRL register. By selecting fet_test_type=A and setting fet_test_start while fet_test_unlock="H," a Type A inspection sequence is started. When a Type A inspection sequence is started, this IC turns on the mid-voltage generating resistors and waits for a certain period of time. After that, this IC turns all pre-drivers for motor control OFF and performs expectation comparison. Then, this IC compares comparator output (after being noise filtered) with expected values while tuning ON the pre-drivers for motor control one by one. While an inspection sequence is being executed, resistors for maintaining HUS, HVS, and HWS at the mid-voltage when pre-drivers are off are tuned ON. During an inspection sequence, VDS comparator (after being filtered) output is stored in registers according to the predefined timing. Have the microcomputer check the inspection result after confirming that the sequence is completed by fet_auto_test="L." When no disagreement with expected values is found, fet_test_err="L" is given. When there is any disagreement with the expected values, the sequence is stopped when a disagreement is found, and at what step the disagreement is generated can be checked by reading ft_seq_num. The comparator (after being noise filtered) output stored when a disagreement is detected can be checked by reading VDS_COMP_STAT after setting ft_comp_sel="L." Where the fault has occurred can be presumed by comparing the sequence number when the expectation disagreement is generated, expected values in Table 7.8-b, with the comparator output.

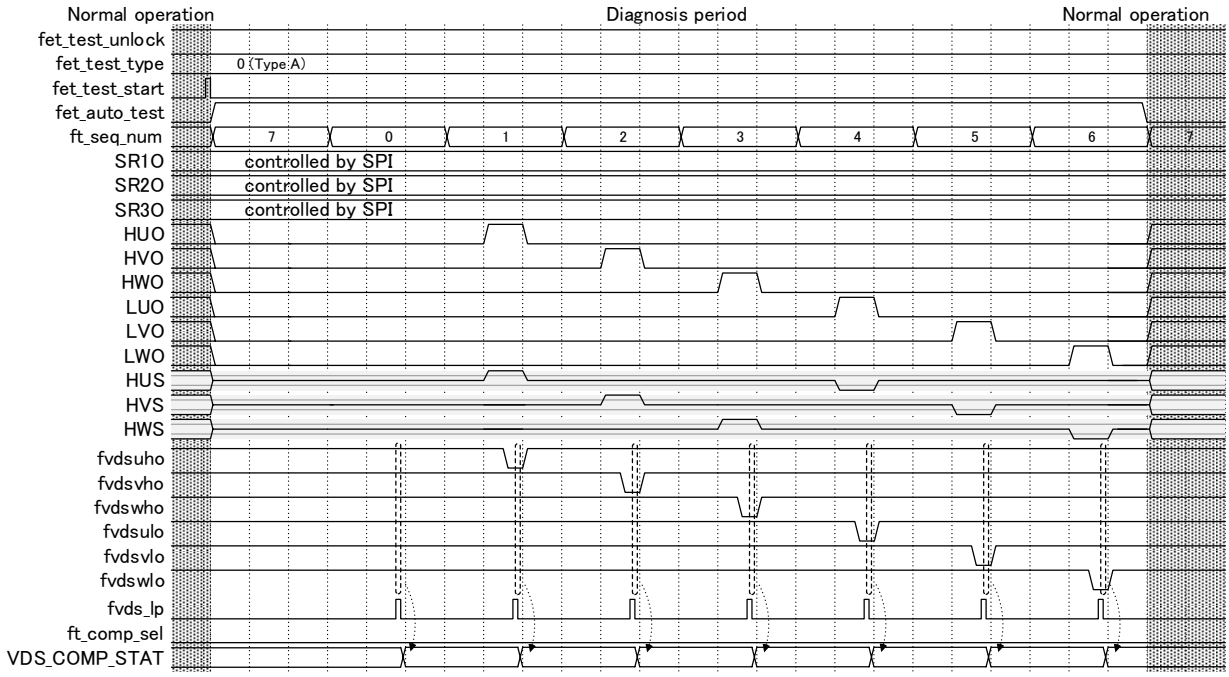


Fig. 7.8-c Operation waveforms in the inspection method Type A

Table 7.8-b Expected values in the inspection method Type A

		VDS_COMP_STAT						
		D10	D8	D6	D4	D2	D0	
		compout_uh	compout_ul	compout_vh	compout_vl	compout_wh	compout_wl	HEX
ft_seq_num	0	1	1	1	1	1	1	0555
	1	0	1	1	1	1	1	0155
	2	1	1	0	1	1	1	0515
	3	1	1	1	1	0	1	0551
	4	1	0	1	1	1	1	0455
	5	1	1	1	0	1	1	0545
	6	1	1	1	1	1	0	0554

7.8.5. Inspection method Type B

This type is intended to be performed while motor relays are ON. Before starting inspection, set motor relays ON by the CP_RLY_CTRL register. By selecting fet_test_type=B and setting fet_test_start while fet_test_unlock="H," a Type B inspection sequence is started. When a Type B inspection sequence is started, this IC turns on the mid-voltage generating resistors and waits for a certain period of time. After that, this IC turns all pre-drivers for motor control OFF and performs expectation comparison. Then, this IC compares comparator output (after being noise filtered) with expected values while tuning ON the pre-drivers for motor control one by one. While an inspection sequence is being executed, resistors for maintaining HUS, HVS, and HWS at the mid-voltage when pre-drivers are off are tuned ON. During an inspection sequence, VDS comparator (after being filtered) output is stored in registers according to the predefined timing. Have the microcomputer check the inspection result after confirming that the sequence is completed by fet_auto_test="L." When no disagreement with expected values is found, fet_test_err="L" is given. When there is any disagreement with the expected values, the sequence is stopped when a disagreement is found, and at what step the disagreement is generated can be checked by reading ft_seq_num. The comparator (after being noise filtered) output stored when a disagreement is detected can be checked by reading VDS_COMP_STAT after setting ft_comp_sel="L." Where the fault has occurred can be presumed by comparing the sequence number when the expectation disagreement is generated, expected values in Table 7.8-c, with the comparator output.

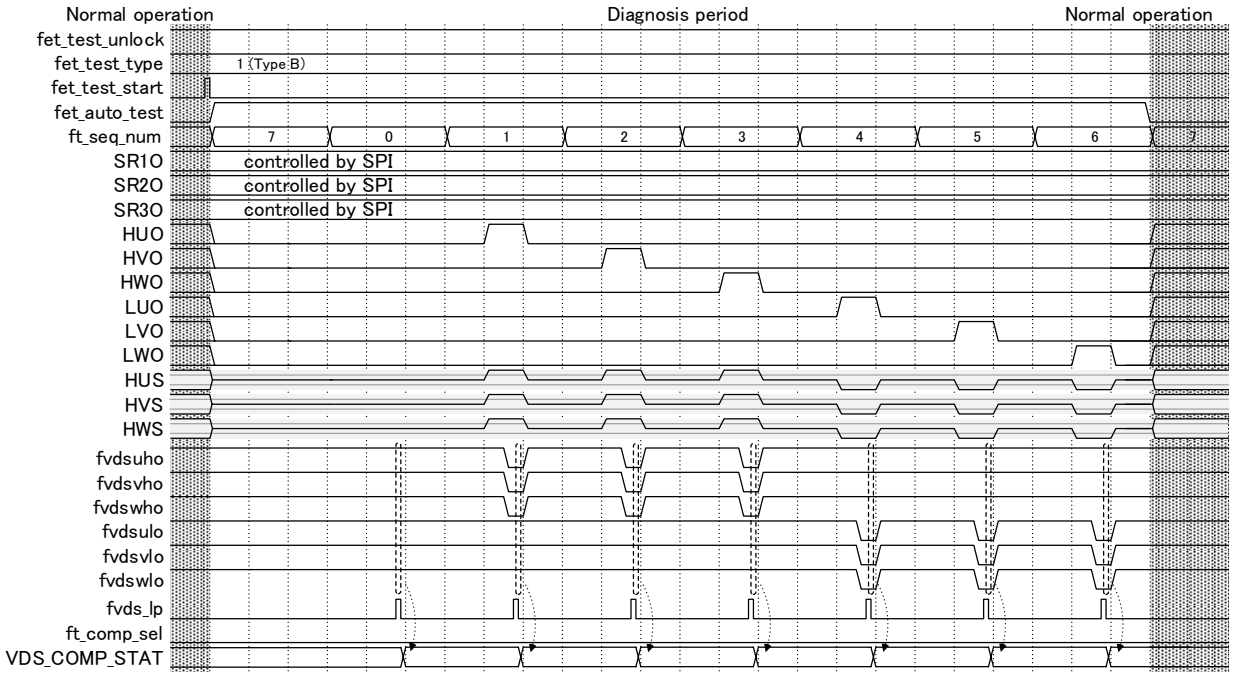


Fig. 7.8-d Operation waveforms in the inspection method Type B

Table 7.8-c Expected values in the inspection method Type B

		VDS_COMP_STAT						
		D10	D8	D6	D4	D2	D0	
		compout_uh	compout_ul	compout_vh	compout_vl	compout_wh	compout_wl	HEX
ft_seq_num	0	1	1	1	1	1	1	0555
	1	0	1	0	1	0	1	0111
	2	0	1	0	1	0	1	0111
	3	0	1	0	1	0	1	0111
	4	1	0	1	0	1	0	0444
	5	1	0	1	0	1	0	0444
	6	1	0	1	0	1	0	0444

7.8.6. Inspection method Type C

This type is intended to be used when inspecting whether pre-drivers for motor control can be stopped when abnormality is detected. When motor relays or power supply relays are used, perform the inspection after stopping the pre-drivers by setting ALARM terminal = "L" on the microcomputer or other means after setting the relay operation by CP_RLY_CTRL register so that FETs for motor control operate normally. At this time, set alr_op="H" in ALM_CTRL so that only the pre-drivers for motor control should stop and relays should not stop when ALARM is detected.

By selecting fet_test_type=C and setting fet_test_start while fet_test_unlock="H," a Type C inspection sequence is started. When a Type C inspection sequence is started, this IC turns on the mid-voltage generating resistors and waits for a certain period of time. After that, this IC turns all pre-drivers for motor control off and performs expectation comparison. Then, this IC compares comparator output (after noise filtered) signals with the expected values for two cases: when three channels of the motor control pre-drivers in the high side are turned ON simultaneously and when three channels in the low side are turned ON simultaneously. While an inspection sequence is being executed, resistors for maintaining HUS, HVS, and HWS at the mid-voltage when pre-drivers are off are tuned ON. During an inspection sequence, VDS comparator (after being filtered) output is stored in registers according to the predefined timing. Have the microcomputer check the inspection result after confirming that the sequence is completed by fet_auto_test="L." When no disagreement with expected values is found, fet_test_err="L" is given. When there is any disagreement with the expected values, the sequence is stopped when a disagreement is found, and at what step the disagreement is generated can be checked by reading ft_seq_num. The comparator (after being noise filtered) output stored when a disagreement is detected can be checked by reading VDS_COMP_STAT after setting ft_comp_sel="L." Where the fault has occurred can be presumed by comparing the sequence number when the expectation disagreement is generated, expected values in Table 7.8-d, with the comparator output.

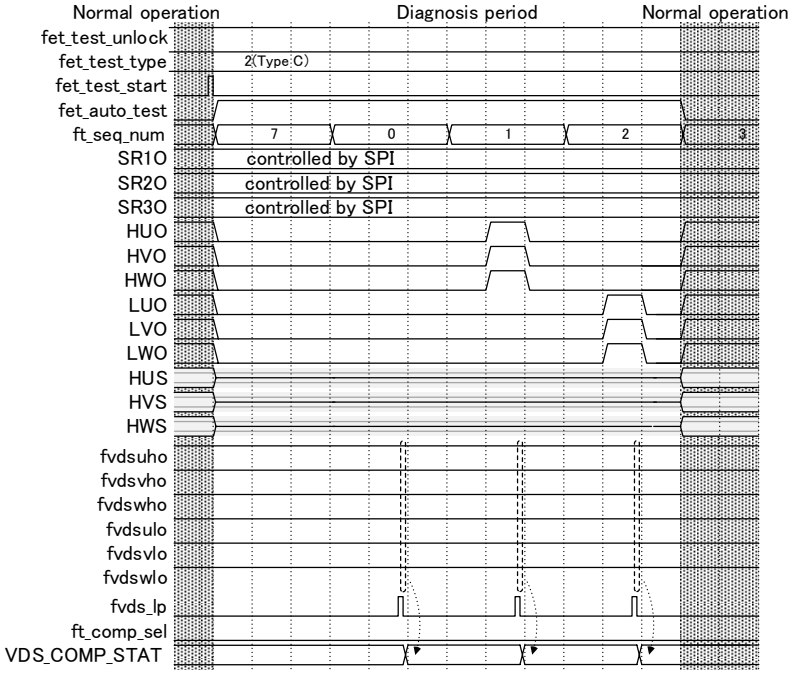


Fig. 7.8-e Operation waveforms in the inspection method Type C

Table 7.8-d Expected values in the inspection method Type C

		VDS_COMP_STAT						
		D10	D8	D6	D4	D2	D0	
		compout_uh	compout_ul	compout_vh	compout_vl	compout_wh	compout_wl	HEX
ft_seq_num	0	1	1	1	1	1	1	0555
	1	1	1	1	1	1	1	0555
	2	1	1	1	1	1	1	0555

7.8.7. Inspection method Type D

This model is intended to be used when inspecting the independence of the motor relays, but allows any combination of FET drives to be set by the FET_TEST_CNT2 register, so can be used for general purposes. A Type D inspection is executed for a single pattern only. The Type D inspection allows any combination of FET drives to be set but uses the values at the timing when the Type D inspection sequence is started, so set the desired values before starting. When a drive pattern in which both high side and low side are ON simultaneously, both the high and low sides are treated as OFF. The IC does not perform expectation comparison but the comparator output (after being noise filtered) signals can be read for six channels. While an inspection sequence is being executed, resistors for maintaining HUS, HVS, and HWS at the mid-voltage when pre-drivers are off are tuned ON.

By selecting fet_test_type=D and setting the fet_test_start during a fet_test_unlock=H period, a Type D inspection sequence is started. When a Type D inspection sequence is started, this IC turns on the mid-voltage generating resistors and waits for a certain period of time. After that, FETs are driven by the drive pattern set in the FET_TEST_CONT2 register. During an inspection sequence, VDS comparator (after being filtered) output is stored in registers according to the predefined timing. Have the microcomputer check the inspection result after confirming that the sequence is completed by fet_auto_test="L." The comparator (after being noise filtered) output stored during the inspection can be checked by reading VDS_COMP_STAT, so, have the microcomputer check whether the operation is as expected or not.

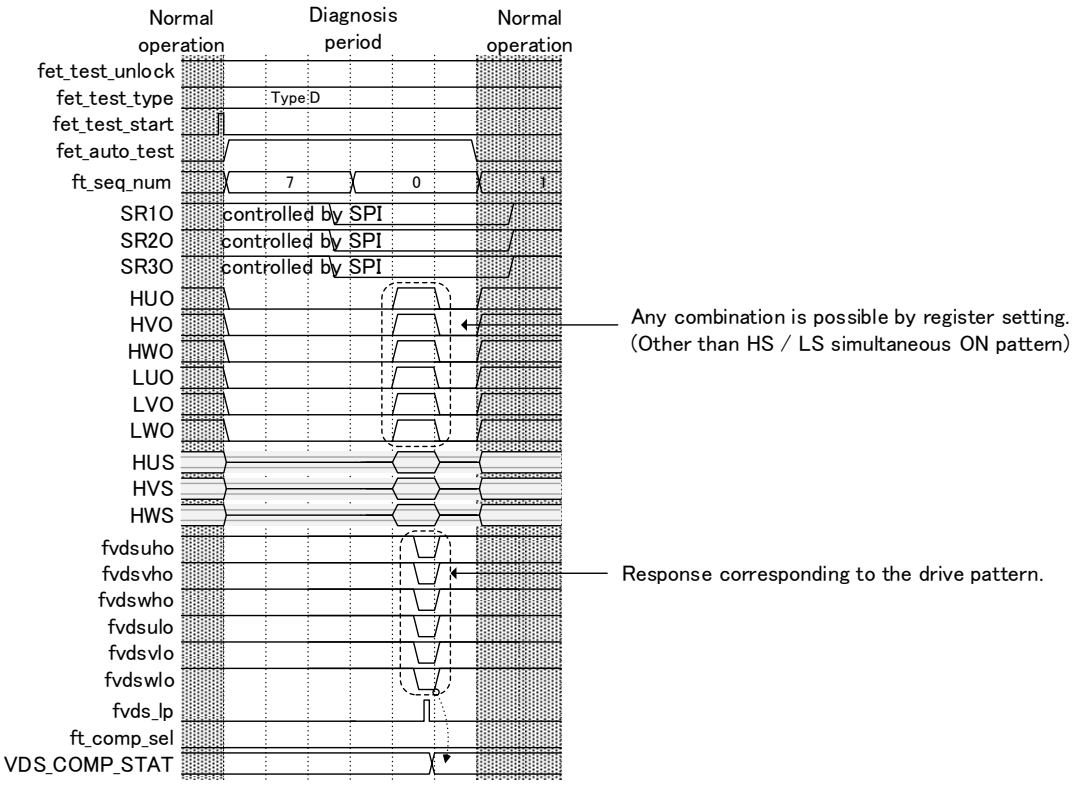


Fig. 7.8-f Operation waveforms in the inspection method Type D

7.8.8. Starting and ending an inspection sequence

By setting the fet_test_start bit after setting fet_test_unlock="H," inspection is started. Fig. 7.8 g shows a period described as "Normal operation, which indicates that the IC's operation has gotten out of the FET_TEST mode. Please set fet_test_nulock="L" during the period of "normal operation in which actually driving a motor is intended" at the system level to prevent FET_TEST from being invoked incorrectly. Even if fet_test_start is received during an inspection, it is ignored. While FET_TEST is being executed, pre-drivers for motor control are controlled by the FET_TEST block. To prevent FETs from being unintentionally driven when FET_TEST is started and ended, have the microcomputer control FETs' control signals (HUI, HVI, HWI, LUI, LVI, LWI terminal input) so that FETs are turned OFF before executing FET_TEST.

There are two ways to stop an inspection: using fet_test_stop and fet_test_unlock="L."

When stopped by fet_test_stop, the inspection stops when a step being executed is completed (the ft_seq_num after the inspection completion is number of the inspection step executed last). However, when fet_test_stop is received in the final inspection step in each inspection sequence, it is ignored (ft_seq_num=6h in a Type A or Type B inspection sequence, ft_seq_num=2h in a Type C inspection sequence, Type D inspection sequence).

When fet_test_unlock="L" is used, the inspection is forced to return to the normal operation state when fet_test_unlock="L" is received irrespective of whether the inspection step being executed has been completed or not (the relation between ft_seq_num and stored comparator output results is not guaranteed).

The vds**_det which is the input signal to the noise filter for VDS detection is enabled only during periods when the applicable channels are controlled to be ON and used for VDS voltage abnormality detection, but is always enabled for FET inspection during the FET_TEST periods. However, VDS abnormality detection is disabled during FET_TEST periods, so VDS abnormality is not detected during a FET_TEST period. While FET_TEST is being executed, resistors for maintaining the mid-voltage are tuned ON.

For inspection methods Type A and Type B, when there is no disagreement with expected values, an inspection stops at ft_seq_num=7h, and for Type C inspection method, at ft_seq_num=3h. The fet_auto_test is a register that can be read and becomes "H" while FET_TEST is being executed.

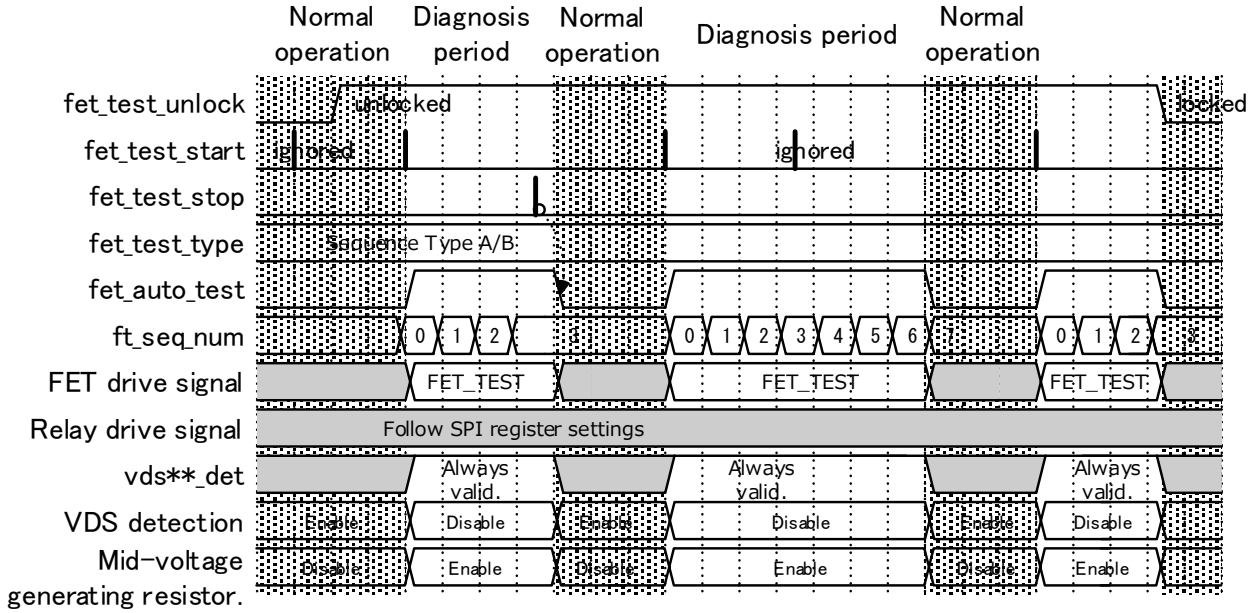


Fig. 7.8-g Operation waveforms related to the starting and ending of FET inspection

7.8.9. Operation when disagreement with any expected value occurs

In an inspection of Type A/Type B/Type C, expectation comparison is performed during the inspection. When disagreement with any expected value occurs, the inspection sequence is stopped and fet_test_err="H" is set. At this time, the number of the inspection sequence at which the expectation disagreement occurred is stored in ft_seq_num. In ft_comp_save (data when VDS_COMP_STAT's ft_comp_sel="L"), the comparator output (after being noise filtered) signals in the inspection performed last (expectation disagreement occurred) are stored for six channels. By reading these values, the microcomputer can check at what output at what inspection step the disagreement occurred. The fet_test_err register and ft_comp_save register are cleared when a new inspection is started or the ft_save_cl bit is set.

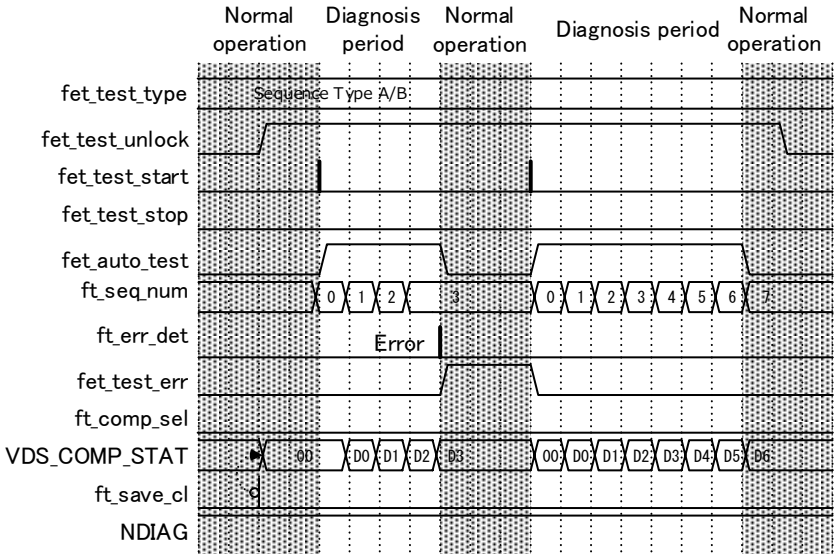


Fig. 7.8-h Operation waveforms when expectation disagreement is detected

7.8.10. Selecting data to be read

Data to be read by the VDS_COMP_STAT register can be selected by setting the ft_comp_sel bit from data during an automatic sequence and current values of VDS comparator output. The ft_comp_sel is only a setting bit to select which data to read, and does not affect data stored in automatic sequences. There is no restriction that ft_comp_sel="L" has to be always set during an automatic sequence. It is enough to set ft_comp_sel="L" when checking the results stored in an automatic sequence.

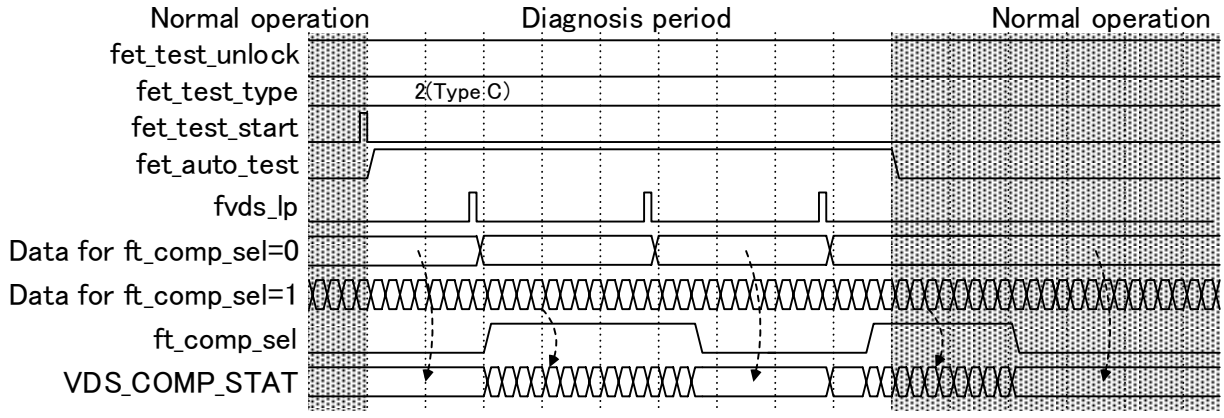


Fig. 7.8-i Selecting data to be read by setting ft_comp_sel

7.8.11. Output to NDIAG during FET inspection

Setting ft_ndiag_sel="H" allows NDIAG="L" to be set while FET_TEST is being executed (during a fet_auto_test="H" period) and when expectation disagreement is detected during an inspection (during a fet_test_err="H" period). The fet_test_err is cleared when a new inspection is started or the ft_save_cl bit.

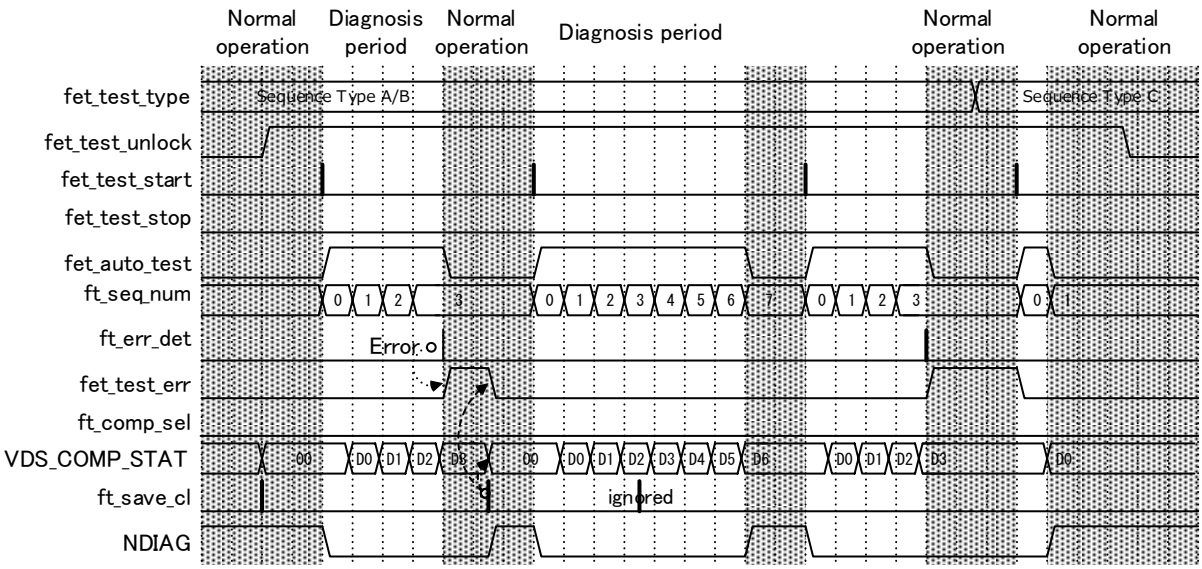


Fig. 7.8-j Operation waveform when outputting to NDIAG during inspection

Table 7.8-e shows the FET inspection time when there is no error. When ft_ndiag_sel = "H" is set it is the same as the length of the NDIAG = "L" period.

Table 7.8-e FET inspection time

Test Type	Typ.	Max
Type A	1024µs	1576µs
Type B	1024µs	1576µs
Type C	512µs	788µs
Type D	256µs	394µs

7.9. SPI communication circuit

The SPI communication circuit consists of the SPI core circuit and register read circuit.
Only when NSCS="L," communication with a microcomputer is possible.
At a rising edge of the clock, the microcomputer writes data to SI and at the next falling edge, the IC reads the data.
And at a rising edge of the clock, the IC writes data to SO and at the next falling edge, the microcomputer reads the data.
SI receives data bits from the microcomputer from MSB to LSB.
SO sends data bits to the microcomputer from MSB to LSB.
The output is in a push-pull configuration and becomes a high impedance when NSCS="H."
And in the IC, the NSCS terminal is pulled up by a resistor, and SCLK and SI terminals are pulled down by resistors.

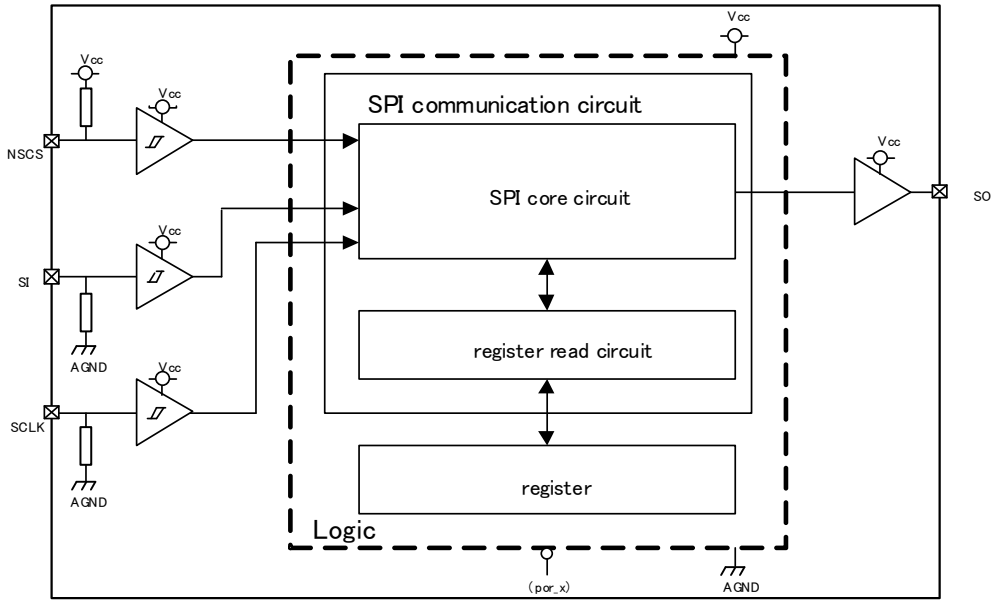


Fig. 7.9-a SPI communication circuit block diagram

7.9.1. SPI communication operation

When NSCS="L," serial data is transmitted in sync with SCLK. When NSCS="H," the SO output becomes a high impedance. The frame length is 32 bits. Two functions are provided: read operation and write operation, and selection between read operation and write operation can be made by "RW" bit (Address [7]). Address [0] is not used for address selection. The "Dummy" bit does not affect operation.

<Write operation>

The data format in the write operation is shown in Fig. 7.9 b.

SI consists of Address[7:0], address specifying bits, Write_Data[15:0], write data specifying bits, and CRC[7:0], bits for checking data. When writing, an address is specified by setting Address[7]=0. Address[0] is not used for address selection. CRC covers Address[7:0] and Write_Data[15:0].

SO outputs data of the address set by SI to Previous_Data[15:0], after dummy data (0x00) is output in 8 bits during the SI's address setting period. At this time, the address data used for SO output is not checked by CRC. For write-only registers, output data from SO is zero. Previous_Data [15: 0] is the data immediately before Write_Data [15: 0] of the register specified by Address [7: 0] to be written. CRC covers Previous_Data[15:0].

After writing, always confirm that correct data is written by reading the data. And empty bits having no register are read as 0 when read.

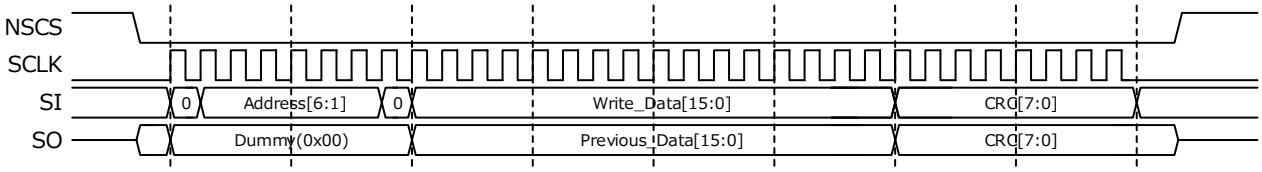


Fig. 7.9-b Data format during write operation

< Read operation>

The data format in the read operation is shown in Fig. 7.9-c.

SI consist of Address[7:0], address specifying bits, Dummy[7:0], dummy data, and CRC[7:0], bits for checking data. When reading, an address is specified by setting Address[7]=1. Address[0] is not used for address selection. CRC covers Address[7:0].

SO outputs of the address set by SI to Read_Data[15:0], after dumy data (0x00) is output during SI's address setting period. Empty bits having no register are read as 0 when read. CRC covers Read_Data[15:0].

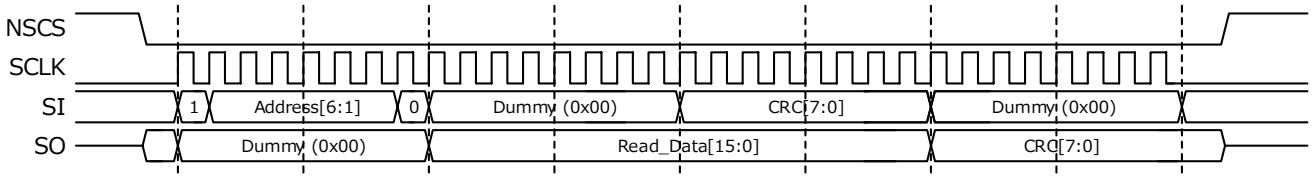


Fig. 7.9-c Data format during read operation

<CRC error check>

CRC error check is conducted to check whether data communication was correctly performed or not.

The generating polynomial is shown below. Its initial value is 0xFF.

$$x^8+x^4+x^3+x^2+1$$

When a CRC error is found, the operation is as shown below.

(1) In write operation

When a CRC error is found, data is not written to the IC.

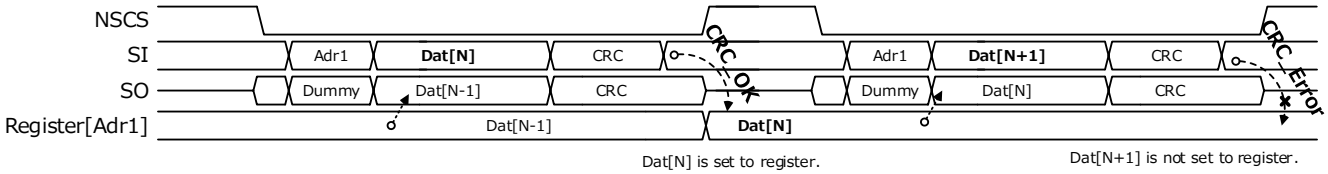


Fig. 7.9-d CRC error during write operation

(2) In read operation

When a CRC error is found, a bad CRC intentionally created is returned from SO in the same frame. This makes the microcomputer detect the CRC error.

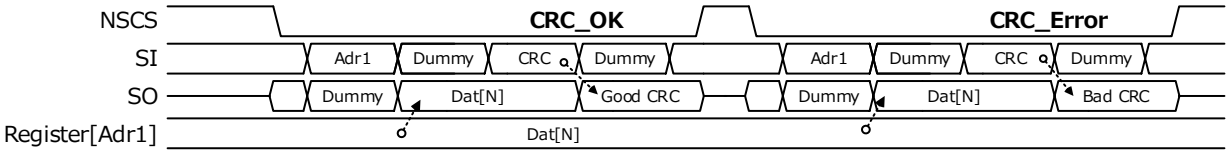


Fig. 7.9-e CRC operation during read operation

<When Vcc drop is detected>

When a Vcc drop is detected, SPI communication cannot be conducted.

When a Vcc drop is detected, SO is fixed to "0." (both in write operation and in read operation)

<During LBIST>

SPI communication cannot be conducted.

<Judged as Fail>

In SPI communication, the IC judges that an communication error has occurred in the following cases, and sets NDIAG="L," and "1" is written to err_spi: register of SPI communication abnormality.

(1) When an address with no register is accessed, an error is generated. For address judgment, Address[7:1] is used (When data is to be written to a register to which any write address is assigned, no data is written to the IC). Address[0] is ignored.

・SO data in write operation is Dummy="0," Previous_Data="0." And since no data is written to registers, register data maintains the previous state (or default values).

・SO data in read operation is "0."

(2) When the frame length is other than 32 bits, a communication error is generated.

・When the frame length in write operation is other than 32 bits, nothing is written to the IC.

・When the frame length is less than 32 bits in read operation, SO is HiZ when NSCS="H."

・When the frame length is 33 bits or longer in read operation, SO is "0" output for the 33rd bit and later in the transmission frame.

(3) When a CRC error is detected, a communication error is generated.

・When a CRC error is detected in write operation, nothing is written to the IC.

・When a CRC error is detected in read operation, an intentionally created bad CRC is returned.

*An intentionally created bad CRC is made of bits generated by inverting all bits of a normal CRC for Read_Data[15:0] output from SO.

7.9.2. QA timer function

The SPI circuit contains QA operation and timer functions, and this IC can perform protection operation such as checking whether the microcomputer's arithmetic function works correctly at a certain level and turning pre-drivers off when pre-defined conditions are not met. With the QA_CTRL register, timeout enabled/disabled, timeout time, and operation when an accumulated error value has exceeded the pre-defined value are set. By using ANSWER_SET register's qa_code[3:0] or qa_dat[3:0], for the QA timer block, starting the QA timer (Start command), setting answers to the QA timer (AnsSet command) and stopping the QA timer (Stop command) can be performed. In the calculation of answer data of the QA timer, by reading the QA_COUNT register, data such as QA timer's sequence number at a read operation and expected value data in the previous sequence can be read. So, use these values to create answer data in the microcomputer side and set them in this IC.

7.9.2.1. Start command

By setting qa_code[3:0]=0xA (Start command) in the ANSWER_SET register, a QA timer sequence is started. Set an initial value that is expected as an answer to qa_dat[3:0] at this time (the initial value cannot be set arbitrarily).

When en_qat="H" has been set, timeout measurement starts at a rising edge of NSCS signal which is a related signal of SPI. As the determination of a sequence start uses qa_code[3:0]=0xA only, the QA timer sequence is started even if the value of qa_dat[3:0] is not valid. However, since the set data is an error, the error accumulation counter is incremented. When a QA timer sequence has already been started and an additional Start command is received, the error accumulation counter is incremented. When a CRC error is generated at the SPI communication level, the sequence is not started as it is discarded as an SPI communication error.

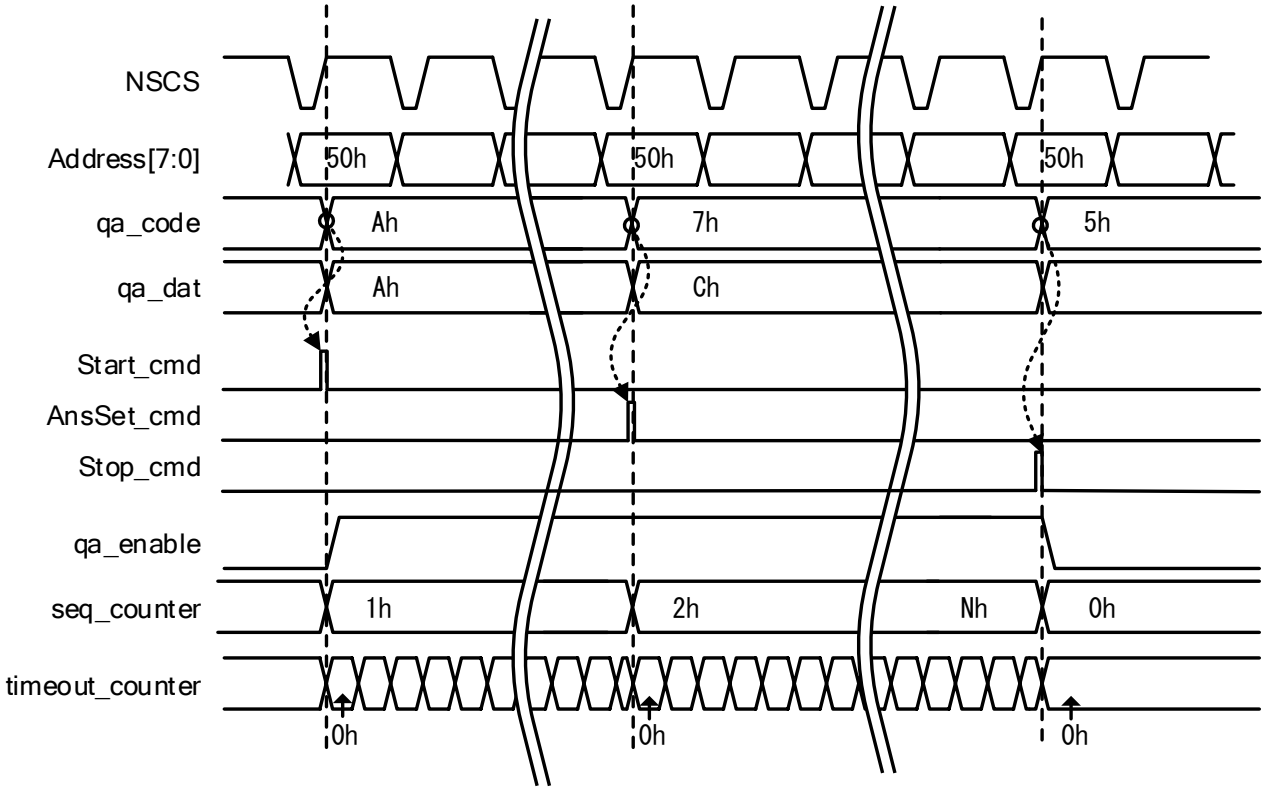


Fig. 7.9-f Start / AnsSet / Stop command

7.9.2.2. AnsSet command

By setting qa_code[3:0]=0x7 (AnsSet command) in the ANSWER_SET register, an answer value in the QA timer's sequence can be set in qa_dat[3:0]. When the setting is for a period when a sequence of the QA timer has not been started, the setting is invalid and discarded.

When en_qat="L," timeout measurement is not performed. When the value of qa_dat[3:0] agrees with the expected value, the error accumulation counter is reset, the sequence counter is incremented, and a next answer is awaited. When the value of qa_dat[3:0] disagrees with the expected value, the error accumulation counter is incremented, the sequence counter is incremented, and a next answer is awaited. When a CRC error is generated at the SPI communication level, QA timer judgment

is not performed as it is discarded as an SPI communication error. The sequence counter is also not incremented.

When en_qat="H," timeout measurement as well as answer value check are performed at the same time. Measurement starts from the rising edge of the NSCS signal of the previous Start command or from the rising edge of the NSCS signal of the previous AnsSet command, and whether the next AnsSet command is set within Tqa which is the timeout time set in the register is checked in advance. When an AnsSet command has not been set within the expected time or the value of qa_dat[3:0] that has been set does not agree with the expected value, the error accumulation counter and sequence counter are incremented to wait for the next answer. The timeout measuring counter is reset when the value of the sequence counter has changed, and measurement is started again. When an CRC error is generated at the SPI communication level, AnsSet command is not set as it is discarded as an SPI communication error.

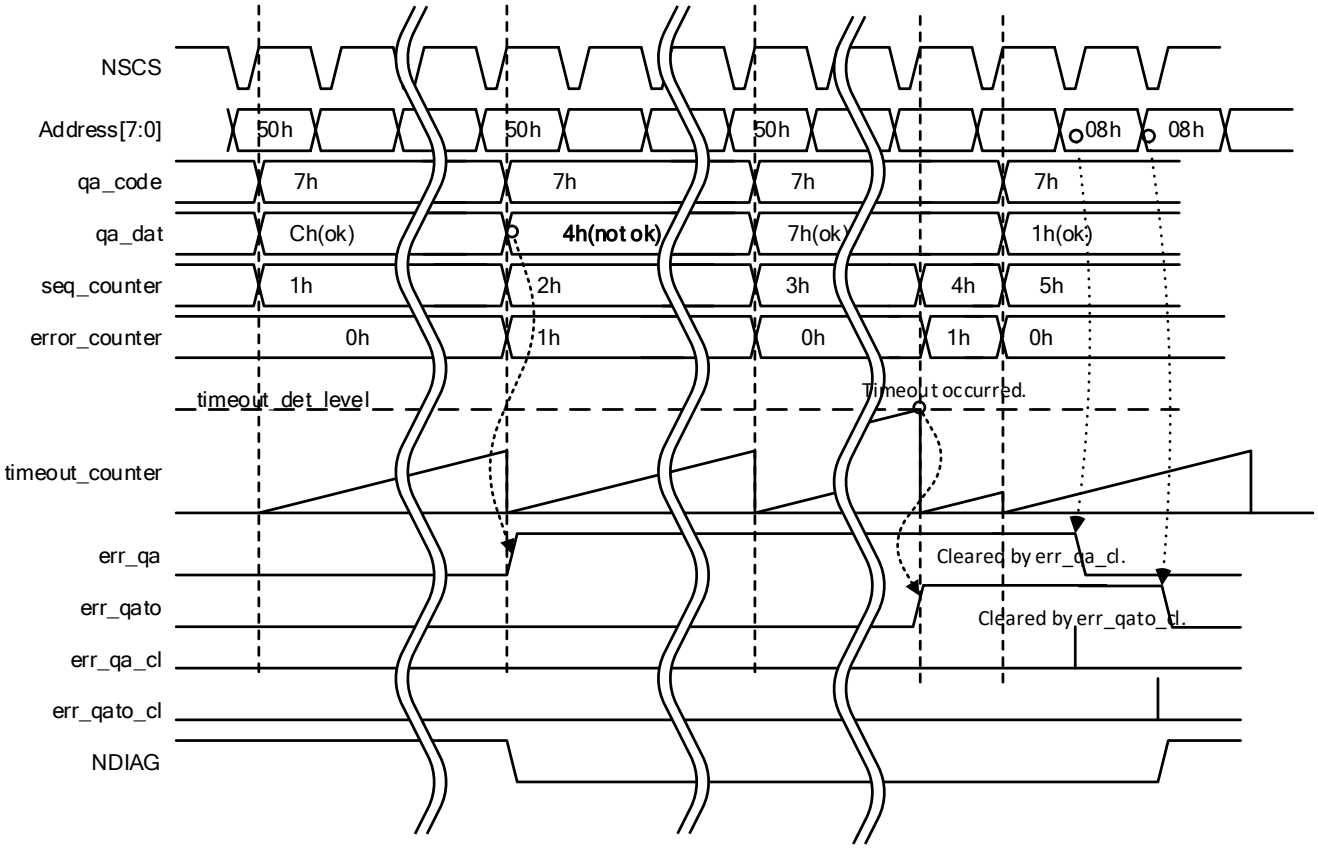


Fig. 7.9-g Operation waveforms when the calculation result is NG, when timeout occurred

7.9.2.3. Stop command

By setting qa_code[3:0]=0x5 (Stop command) in the ANSWER_SET register, the QA timer sequence is stopped. At this time, qa_dat[3:0] is ignored. The Stop command is valid while a QA timer sequence has been started and discarded when issued for other periods. When an CRC error is generated at the SPI communication level, a Stop command is not received as it is discarded as an SPI communication error.

7.9.2.4. Invalid command codes

When a command code other than AnsSet command and Stop command is specified to qa_code[3:0] in the ANSWER_SET register while a QA timer sequence has been started, the error accumulation counter is incremented. The sequence counter is not incremented, and the timeout counter is not cleared.

7.9.2.5. Various statuses and error accumulation counter

The status bit err_qa is set to "H" for a sequence where answer data has turned out to be invalid, and it is maintained until it is cleared by the err_qa_cl bit.
The status bit err_qato is set to "H" for a sequence where answer data has not been obtained within the pre-defined time, and it is maintained until it is cleared by the err_qato_cl bit.
The status bit err_qac is set to "H" for a sequence where the error accumulation counter value has reached 4, and it is maintained until it is cleared by the err_qac_cl bit.

Table 7.9-a Conditions to increment and clear the sequence counter

Increment	Clear
Received Start command / AnsSet command Timeout detected	Received Stop command

Table 7.9-b Conditions to increment and clear the error accumulation counter

Increment	Clear
The data set from the microcomputer is invalid Data was not set within the specified time when en_qat = "H" was set A code other than AnsSet / Stop command was received while the QA timer sequence was valid	Sequence started by Start command When the error accumulation counter is less than 4 and err_qac = "L", and the data set from the microcomputer matches the expected value. Furthermore, when en_qat = "H", data is set within the timeout period. When the error accumulation flag is cleared by the err_qac_cl bit.

Table 7.9-c Conditions to increment and clear the timeout counter

Increment	Clear
Increment automatically by internal clock	When the sequence counter value changes, the timeout counter is cleared and re-measurement is started.

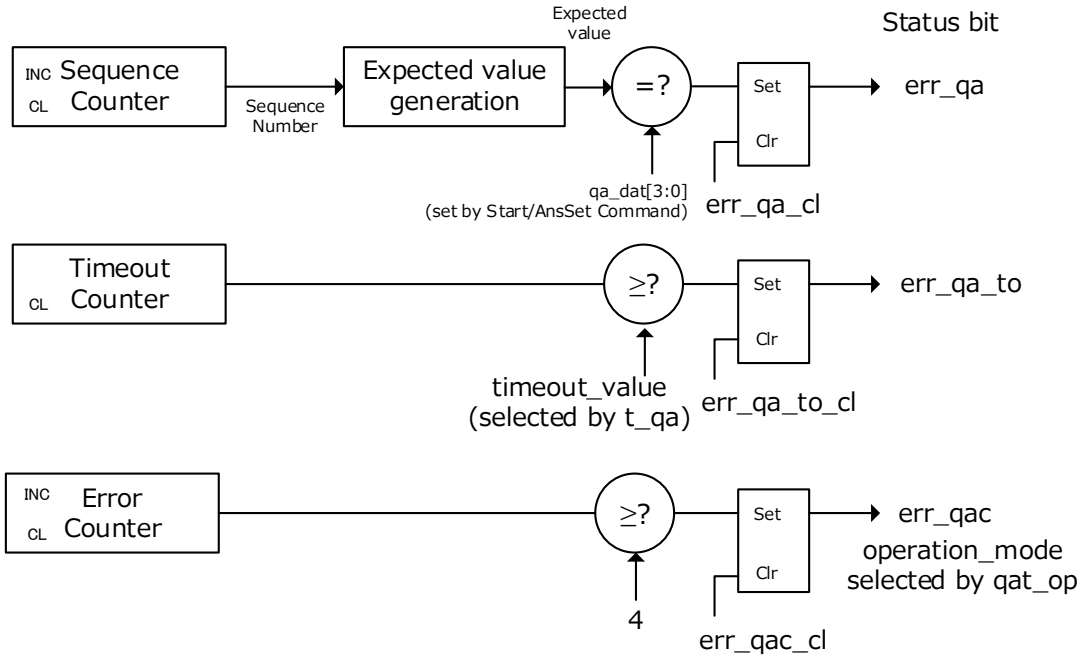


Fig. 7.9-h Generation of various status bits

7.9.2.6. **Operation linked with status bits**

NDIAG becomes "L" while any of err_qa, err_qato, and err_eqc has been set. While err_eqc is set to "H," the operation of the charge pump and pre-drivers follows what has been set by qat_op. The value qat_op can be modified at any time; however, qat_op has no effect on actual operations while err_qac="H", The new qat_op value takes effect after err_qac = "L".

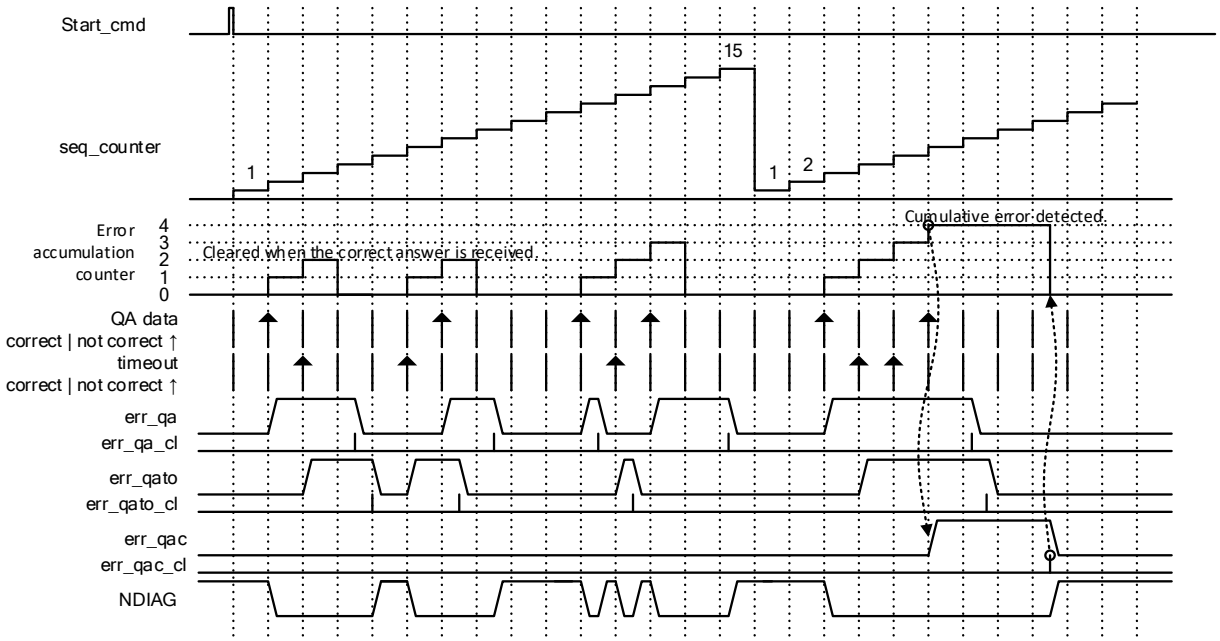


Fig. 7.9-i Behavior by various flags and clear bit at the time of error occurrence

7.9.2.7. Calculation of answer values

By reading current_seq_number of the QA_COUNT register, the QA timer's current sequence number can be read. The microcomputer can use currnet_seq_number when it generates an answer value from the table of expected values. By reading prev_expected_value of the QA_COUNT register, the expected value of the previous sequence can be read. When the microcomputer calculates the answer value, it can obtain the answer value by shifting the value of prev_expected_value by 4 bits according to the generating polynomial.

The formula of the QA arithmetic function compares computation results in 4 bits generated by the formula below and computation results received from the microcomputer.

$$x^4 + x^3 + 1$$

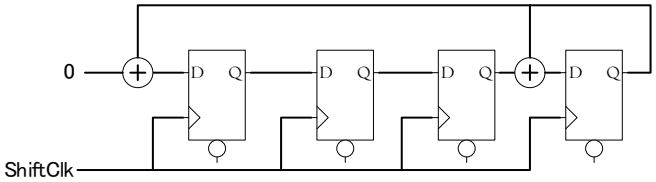


Fig. 7.9-j Set prev_expected_value and shift 4 bits

The number of calculation times has 16 values, and when the number of calculation times is 15, current_seq_number=1.

Table 7.9-d Calculation of expected values from read data

0x0D:QA_COUNT(Read)		0x50:ANSWER_SET
current_seq_number	prev_expected_value	qa_dat
Initial Value 0	Fh	Ah
1	Ah	Ch
2	Ch	8h
3	8h	7h
4	7h	Dh
5	Dh	1h
6	1h	9h
7	9h	Eh
8	Eh	3h
9	3h	2h
10	2h	Bh
11	Bh	5h
12	5h	6h
13	6h	4h
14	4h	Fh
15	Fh	Ah

7.9.3. Register map

Symbol	WRITE_ADDRESS		READ_ADDRESS		D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
OPSEL1	00h	0000_000*	80h	1000_000*	–	ocph_op			–	ovc_op			–	ovccop_op			–	uvccop_op		
OPSEL2	04h	0000_010*	84h	1000_010*	–	–	–	–	–	tsd_op			–	ferr_op			–	uvb_op		
STAT1	–	–	88h	1000_100*	uvb	ovc	ocph	uvccop	ovccop	tsd	err_of	err_uf	err_pl_u	err_pl_v	err_pl_w	alm_det	err_spi	err_qa	err_qato	err_qac
STAT1_CLR	08h	0000_100*	–	–	uvb_cl	ovc_cl	ocph_cl	uvccop_cl	ovccop_cl	tsd_cl	err_of_cl	err_uf_cl	err_pl_u_cl	err_pl_v_cl	err_pl_w_cl	_	err_spi_cl	err_qa_cl	err_qato_cl	err_qac_cl
STAT2	–	–	8Ch	1000_110*	–	–	–	–	vgs_uh	vds_uh	vgs_ul	vds_ul	vgs_vh	vds_vh	vgs_vl	vds_vl	vgs_wh	vds_wh	vgs_wl	vds_wl
STAT2_CLR	0Ch	0000_110*	–	–	–	–	–	–	vgs_uh_cl	vds_uh_cl	vgs_ul_cl	vds_ul_cl	vgs_vh_cl	vds_vh_cl	vgs_vl_cl	vds_vl_cl	vgs_wh_cl	vds_wh_cl	vgs_wl_cl	vds_wl_cl
CP_RLY_CTRL	14h	0001_010*	94h	1001_010*	–	–	–	en_cp	–	–	–	srly3_drv	–	–	–	srly2_drv	–	–	–	srly1_drv
PL_CTRL	18h	0001_100*	98h	1001_100*	–	–	–	pl_op	–	–	–	plu_dis	–	–	–	plv_dis	–	–	–	plw_dis
T_ILIM	1Ch	0001_110*	9Ch	1001_110*	–	–	t_ilim		–	–	–	–	–	–			–	–		
FET_OPSEL	24h	0010_010*	A4h	1010_010*	–	–	–	–	–	vgs_op			vdsh_op				vdsl_op			
HS_VDS_SEL	28h	0010_100*	A8h	1010_100*	–	–	fil_vdsh		vth_vdsuh				vth_vdsvh				vth_vdswh			
LS_VDS_SEL	2Ch	0010_110*	ACh	1010_110*	–	–	fil_vdsl		vth_vdsul				vth_vdsvl				vth_vdswl			
FET_DET_SEL	30h	0011_000*	B0h	1011_000*	–	–	–	–	vgshu_dis	vdshu_dis	vgslu_dis	vdslu_dis	vgshv_dis	vdshv_dis	vgslv_dis	vdslv_dis	vgshw_dis	vdshw_dis	vgslw_dis	vdslw_dis
AMP_CTRL	40h	0100_000*	C0h	1100_000*	–	–	–	–	cal_amp_u	gain_amp_u			cal_amp_v	gain_amp_v			cal_amp_w	gain_amp_w		
AMP_STAT_CLR	44h	0100_010*	–	–	–	–	–	–	–	–	–	calu_pass_cl	–	–	–	calv_pass_cl	–	–	–	calw_pass_cl
AMP_STAT	–	–	C4h	1100_010*	–	–	–	cal_en	–	–	–	calu_pass	–	–	–	calv_pass	–	–	–	calw_pass
ALM_CTRL	48h	0100_100*	C8h	1100_100*	–	–	–	alr_op	–	–	–	–	–	–	–	–	–	–	fil_alm	
QA_CTRL	4Ch	0100_110*	Cch	1100_110*	–	qat_op			–	–	t_qa		–	–	–	–	–	–	–	en_qat
ANSWER_SET	50h	0101_000*	–	–	–	–	–	–	–	–	–	–	qa_code				qa_dat			
QA_COUNT	–	–	D0h	1101_000*	–	–	–	–	acc_count				seq_number				prev_expected_value			
BIST_DIAG	54h	0101_010*	D4h	1101_010*	–	–	–	–	–	–	–	–	–	–	–	rebst	–	–	–	diag_dg
BIST_STAT	–	–	D8h	1101_100*	–	–	–	–	–	–	–	–	–	–	lbst_flag	lbst_end	–	–	abst_flag	abst_end

Symbol	WRITE_ADDRESS		READ_ADDRESS		D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
FET_TEST_CNT1	5Ch	0101_110*	DCh	1101_110*	–	–	–	–	fet_manual_test	fet_rmidonU	fet_rmidonV	fet_rmidonW	ft_save_cl	–	ft_ndiag_sel	ft_comp_sel	fet_test_type1	fet_test_type0	fet_test_start	fet_test_stop
FET_TEST_CNT2	60h	0110_000*	E0h	1110_000*	–	–	–	fet_test_unlock	–	typed_uhd	–	typed_uld	–	typed_vhd	–	typed_vld	–	typed_whd	–	typed_wld
FET_TEST_STAT	–	–	E4h	1110_010*	–	–	–	–	–	–	–	–	–	–	fet_auto_test	fet_test_err	–	ft_seq_num2	ft_seq_num1	ft_seq_num0
VDS_COMP_STAT	–	–	E8h	1110_100*	–	–	–	–	–	compout_uh	–	compout_ul	–	compout_vh	–	compout_vl	–	compout_wh	–	compout_wl
DUMMY	7Ch		FCh		dmy15	dmy14	dmy13	dmy12	dmy11	dmy10	dmy9	dmy8	dmy7	dmy6	dmy5	dmy4	dmy3	dmy2	dmy1	dmy0

Note

When an attempt is made to write data to a bit that is not assigned (described as "－" in the register map) and the data is set, it is discarded. When the bit is read, it is read as "0."

7.9.3.1. OPSEL1 Write Address=00h / Read Address=80h

Bit	D15	D14	D13	D12	D11	D10	D9	D8
Symbol	–	ocph_op			–	ovc_op		
Initial Value	0	0	0	0	0	0	1	0

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Symbol	–	ovccop_op			–	uvccop_op		
Initial Value	0	0	0	0	0	0	0	0

bit	Symbol	R/W	Function
[14:12]	ocph_op	R/W	Operation selection at VCPH high voltage detection "000"=NDIAG:Output "H", continue operation [Detection disabled] "001"=NDIAG:Output "L"(hold), continue operation "010"=NDIAG:Output "L"(hold), 9ch all pre-drivers drive FET off "011"=NDIAG:Output "L"(hold), 6ch motor pre-drivers drive FET off "100"=NDIAG:Output "L"(hold), 9ch all pre-drivers drive FET off, charge pump off "101"=NDIAG:Output "L"(hold), 9ch all pre-drivers drive FET off(hold), Charge pump off(hold)
[10:8]	ovc_op	R/W	Operation selection when VCC high voltage is detected "000"=NDIAG:Output H, continue operation [Detection disabled] "001"=NDIAG:Output "L"(hold), continue operation "010"=NDIAG:Output "L"(hold), 9ch all pre-drivers drive FET off "011"=NDIAG:Output "L"(hold), 6ch motor pre-drivers drive FET off "100"=NDIAG:Output "L"(hold), 9ch all pre-driver drive FET off, Charge pump off "101"=NDIAG:Output "L"(hold), 9ch all pre-driver drive FET off(hold), Charge pump off(hold)
[6:4]	ovccop_op	R/W	Operation selection when VCC_OP high voltage is detected "000"=NDIAG:Output H, continue operation [Detection disabled] "001"=NDIAG:Output "L"(hold), continue operation "010"=NDIAG:Output "L"(hold), 9ch all pre-drivers drive FET off "011"=NDIAG:Output "L"(hold), 6ch motor pre-drivers drive FET off "100"=NDIAG:Output "L"(hold), 9ch all pre-drivers drive FET off, Charge pump off "101"=NDIAG:Output "L"(hold), 9ch all pre-drivers drive FET off(hold), Charge pump off(hold)
[2:0]	uvccop_op	R/W	Operation selection when VCC_OP low voltage is detected "000"=NDIAG:Output H, continue operation [Detection disabled] "001"=NDIAG:Output "L"(hold), continue operation "010"=NDIAG:Output "L"(hold), 9ch all pre-drivers drive FET off "011"=NDIAG:Output "L"(hold), 6ch motor pre-drivers drive FET off "100"=NDIAG:Output "L"(hold), 9ch all pre-drivers drive FET off, Charge pump off "101"=NDIAG:Output "L"(hold), 9ch all pre-drivers drive FET off(hold), Charge pump off(hold)

Note
When a value that is not indicated as a set value is set, the set value for the Symbol is not updated and its previous value is maintained.

7.9.3.2. **OPSEL2 Write Address=04h / Read Address=84h**

Bit	D15	D14	D13	D12	D11	D10	D9	D8
Symbol	–	–	–	–	–	tsd_op		
Initial Value	0	0	0	0	0	0	1	0

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Symbol	–	ferr_op			–	uvb_op		
Initial Value	0	0	0	0	0	0	0	1

bit	Symbol	R/W	Function
[10:8]	tsd_op Note 1	R/W	Operation selection when overtemperature is detected "000"=NDIAG:Output H, continue operation [Detection disabled] "001"=NDIAG:Output "L"(hold), continue operation "010"=NDIAG:Output "L"(hold), 9ch all pre-drivers drive FET off "011"=NDIAG:Output "L"(hold), 6ch motor pre-drivers drive FET off "100"=NDIAG:Output "L"(hold), 9ch all pre-drivers drive FET off, Charge pump off "101"=NDIAG:Output "L"(hold), 9ch all pre-drivers drive FET off(hold), Charge pump off(hold)
[6:4]	ferr_op	R/W	Operation selection when oscillation frequency abnormality is detected "000"=NDIAG:Output "H", continue operation [Detection disabled] "001"=NDIAG:Output "L"(hold), continue operation "010"=NDIAG:Output "L"(hold), 9ch all pre-drivers drive FET off "011"=NDIAG:Output "L"(hold), 6ch motor pre-drivers drive FET off "100"=NDIAG:Output "L"(hold), 9ch all pre-drivers drive FET off, Charge pump off "101"=NDIAG:Output "L"(hold), 9ch all pre-drivers drive FET off(hold), Charge pump off(hold)
[2:0]	uvb_op	R/W	Operation selection when VB low voltage is detected "000"=NDIAG:Output "L"(hold), 9ch all pre-drivers drive FET off "001"=NDIAG:Output "L",9ch all pre-drivers drive FET off "010"=NDIAG:Output "H",9ch all pre-drivers drive FET off "011"=NDIAG:Output "L"(hold),6ch motor pre-drivers drive FET off "100"=NDIAG:Output "L",6ch motor pre-drivers drive FET off "101"=NDIAG:Output "H",6ch motor pre-drivers drive FET off

Note When a value that is not indicated as a set value is set, the set value for the Symbol is not updated and its previous value is maintained.

Note 1 If the pin short between the VCPH and CP2L pins and between the CP2H and CP1L pins cannot be countereasureed externally to the IC, select "charge pump off" or "charge pump off(hold)" for tsd_op.

7.9.3.3. **STAT1_CLR Write Address=08h**

Bit	D15	D14	D13	D12	D11	D10	D9	D8
Symbol	uvb_cl	ovc_cl	ocph_cl	uvccop_cl	ovccop_cl	tsd_cl	err_of_cl	err_uf_cl
Initial Value	0	0	0	0	0	0	0	0

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Symbol	err_pl_u_cl	err_pl_v_cl	err_pl_w_cl	–	err_spi_cl	err_qa_cl	err_qato_cl	err_qac_cl
Initial Value	0	0	0	0	0	0	0	0

bit	Symbol	R/W	Function
15	uvb_cl	W	Clear status bit uvb (valid when uvb_op = 3'b000, 3'b011) "0"=Invalid "1" = Clear status bit
14	ovc_cl	W	Clear status bit ovc "0"=Invalid "1" = Clear status bit
13	ocph_cl	W	Clear status bit ocph "0"=Invalid "1" = Clear status bit
12	uvccop_cl	W	Clear status bit uvccop "0"=Invalid "1" = Clear status bit
11	ovccop_cl	W	Clear status bit ovccop "0"=Invalid "1" = Clear status bit
10	tsd_cl	W	Clear status bit tsd "0"=Invalid "1" = Clear status bit
9	err_of_cl	W	Clear status bit err_of "0"=Invalid "1" = Clear status bit
8	err_uf_cl	W	Clear status bit err_uf "0"=Invalid "1" = Clear status bit
7	err_pl_u_cl	W	Clear status bit err_pl_u "0"=Invalid "1" = Clear status bit
6	err_pl_v_cl	W	Clear status bit err_pl_v "0"=Invalid "1" = Clear status bit
5	err_pl_w_cl	W	Clear status bit err_pl_w "0"=Invalid "1" = Clear status bit
3	err_spi_cl	W	Clear status bit err_spi "0"=Invalid "1" = Clear status bit
2	err_qa_cl	W	Clear status bit err_qa "0"=Invalid "1" = Clear status bit
1	err_qato_cl	W	Clear status bit err_qato "0"=Invalid "1" = Clear status bit
0	err_qac_cl	W	Clear status bit err_qac "0"=Invalid "1" = Clear status bit

Note After migrating to the normal state, the status bit is cleared by writing "1." The cleared register becomes "0" (initial value). In this case, NDIAG="H," returning to the normal operation. Writing "0" is invalid.
Note In a state where abnormality has been detected, even if "1" is written, the status registers to be cleared are not cleared.
Note The clear bit of a status bit does not need to be returned to 0 after 1 is written.

7.9.3.4. **STAT1 / Read Address=88h**

Bit	D15	D14	D13	D12	D11	D10	D9	D8
Symbol	uvb	ovc	ocph	uvccop	ovccop	tsd	err_of	err_uf
Initial Value	0	0	0	0	0	0	0	0

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Symbol	err_pl_u	err_pl_v	err_pl_w	alm_det	err_spi	err_qa	err_qato	err_qac
Initial Value	0	0	0	0	0	0	0	0

bit	Symbol	R/W	Function
15	uvb	R	VB undervoltage detection "0"=undetected "1"=detected
14	ovc	R	VCC overvoltage detection "0"=undetected "1"=detected
13	ocph	R	VCPH overvoltage detection "0"=undetected "1"=detected
12	uvccop	R	VCC_OP undervoltage detection "0"=undetected "1"=detected
11	ovccop	R	VCC_OP overvoltage detection "0"=undetected "1"=detected
10	tsd	R	Overtemperature detection "0"=undetected "1"=detected
9	err_of	R	Anomaly detection by Two-way internal oscillator frequency monitoring(OSC_IF high frequency anomaly) "0"=undetected "1"=detected
8	err_uf	R	Anomaly detection by Two-way internal oscillator frequency monitoring(OSC_IF low frequency anomaly) "0"=undetected "1"=detected
7	err_pl_u	R	Inhibit input error detection of U-phase pre-driver "0"=undetected "1"=detected
6	err_pl_v	R	Inhibit input error detection of V-phase pre-driver "0"=undetected "1"=detected
5	err_pl_w	R	Inhibit input error detection of W-phase pre-driver "0"=undetected "1"=detected
4	alm_det	R	ARALRM pin input detection "0"=undetected "1"=detected
3	err_spi	R	SPI communication error detection "0"=undetected "1"=detected
2	err_qa	R	QA calculation error detection "0"=undetected "1"=detected
1	err_qato	R	QA timeout error detection "0"=undetected "1"=detected

bit	Symbol	R/W	Function
0	err_qac	R	QA calculation error accumulation detection "0"=undetected "1"=detected

7.9.3.5. **STAT2_CLR Write Address=0Ch**

Bit	D15	D14	D13	D12	D11	D10	D9	D8
Symbol	–	–	–	–	vgs_uh_cl	vds_uh_cl	vgs_ul_cl	vds_ul_cl
Initial Value	0	0	0	0	0	0	0	0

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Symbol	vgs_vh_cl	vds_vh_cl	vgs_vl_cl	vds_vl_cl	vgs_wh_cl	vds_wh_cl	vgs_wl_cl	vds_wl_cl
Initial Value	0	0	0	0	0	0	0	0

bit	Symbol	R/W	Function
11	vgs_uh_cl	W	Clear status bit vgs_uh "0"=Invalid "1" = Clear status bit
10	vds_uh_cl	W	Clear status bit vds_uh "0"=Invalid "1" = Clear status bit
9	vgs_ul_cl	W	Clear status bit vgs_ul "0"=Invalid "1" = Clear status bit
8	vds_ul_cl	W	Clear status bit vds_ul "0"=Invalid "1" = Clear status bit
7	vgs_vh_cl	W	Clear status bit vgs_vh "0"=Invalid "1" = Clear status bit
6	vds_vh_cl	W	Clear status bit vds_vh "0"=Invalid "1" = Clear status bit
5	vgs_vl_cl	W	Clear status bit vgs_vl "0"=Invalid "1" = Clear status bit
4	vds_vl_cl	W	Clear status bit vds_vl "0"=Invalid "1" = Clear status bit
3	vgs_wh_cl	W	Clear status bit vgs_wh "0"=Invalid "1" = Clear status bit
2	vds_wh_cl	W	Clear status bit vds_wh "0"=Invalid "1" = Clear status bit
1	vgs_wl_cl	W	Clear status bit vgs_wl "0"=Invalid "1" = Clear status bit
0	vds_wl_cl	W	Clear status bit vds_wl "0"=Invalid "1" = Clear status bit

Note After migrating to the normal state, the status bit is cleared by writing "1." The cleared register becomes "0" (initial value). In this case, NDIAG="H," returning to the normal operation. Writing "0" is invalid.

Note In a state where abnormality has been detected, even if "1" is written, the status registers to be cleared are not cleared.

Note The clear bit of a status bit does not need to be returned to 0 after 1 is written.

7.9.3.6. **STAT2 / Read Address=8Ch**

Bit	D15	D14	D13	D12	D11	D10	D9	D8
Symbol	–	–	–	–	vgs_uh	vds_uh	vgs_ul	vds_ul
Initial Value	0	0	0	0	0	0	0	0

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Symbol	vgs_vh	vds_vh	vgs_vl	vds_vl	vgs_wh	vds_wh	vgs_wl	vds_wl
Initial Value	0	0	0	0	0	0	0	0

bit	Symbol	R/W	Function
11	vgs_uh	R	External MOSFET VGS overvoltage detection(U phase high side) "0"=undetected "1"=detected
10	vds_uh	R	External MOSFET VDS detection(U phase high side) "0"=undetected "1"=detected
9	vgs_ul	R	External MOSFET VGS overvoltage detection(U phase low side) "0"=undetected "1"=detected
8	vds_ul	R	External MOSFET VDS detection(U phase low side) "0"=undetected "1"=detected
7	vgs_vh	R	External MOSFET VGS overvoltage detection(V phase high side) "0"=undetected "1"=detected
6	vds_vh	R	External MOSFET VDS detection(V phase high side) "0"=undetected "1"=detected
5	vgs_vl	R	External MOSFET VGS overvoltage detection(V phase low side) "0"=undetected "1"=detected
4	vds_vl	R	External MOSFET VDS detection(V phase low side) "0"=undetected "1"=detected
3	vgs_wh	R	External MOSFET VGS overvoltage detection(W phase high side) "0"=undetected "1"=detected
2	vds_wh	R	External MOSFET VDS detection(W phase high side) "0"=undetected "1"=detected
1	vgs_wl	R	External MOSFET VGS overvoltage detection(W phase low side) "0"=undetected "1"=detected
0	vds_wl	R	External MOSFET VDS detection(W phase low side) "0"=undetected "1"=detected

7.9.3.7. CP_RLY_CTRL Write Address=14h / Read Address=94h

Bit	D15	D14	D13	D12	D11	D10	D9	D8
Symbol	–	–	–	en_cp	–	–	–	srly3_drv
Initial Value	0	0	0	1	0	0	0	0

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Symbol	–	–	–	srly2_drv	–	–	–	srly1_drv
Initial Value	0	0	0	0	0	0	0	0

bit	Symbol	R/W	Function
12	en_cp	R/W	Charge pump control "0"=Charge pump output OFF "1"=Charge pump output ON
8	srly3_drv	R/W	Safety relay 3 control "0"=Safety relay OFF "1"=Safety relay ON
4	srly2_drv	R/W	Safety relay 2 control "0"=Safety relay OFF "1"=Safety relay ON
0	srly1_drv	R/W	Safety relay 1 control "0"=Safety relay OFF "1"=Safety relay ON

7.9.3.8. PL_CTRL Write Address=18h / Read Address=98h

Bit	D15	D14	D13	D12	D11	D10	D9	D8
Symbol	–	–	–	pl_op	–	–	–	plu_dis
Initial Value	0	0	0	0	0	0	0	0

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Symbol	–	–	–	plv_dis	–	–	–	plw_dis
Initial Value	0	0	0	0	0	0	0	0

bit	Symbol	R/W	Function
12	pl_op	R/W	Select operation when inhibited input of pre-driver controll signal is detected. "0"=Inhibit input detection result is not set in the status register. NDIAG:"H" "1"=Inhibit input detection result is set in the status register. NDIAG:"L"(hold)
8	plu_dis	R/W	Enable / disable selection of inhibited input of pre-driver controll signal detection (phase U) "0"=Enable "1"=Disable
4	plv_dis	R/W	Enable / disable selection of inhibited input of pre-driver controll signal detection (phase V) "0"=Enable "1"=Disable
0	plw_dis	R/W	Enable / disable selection of inhibited input of pre-driver controll signal detection (phase W) "0"=Enable "1"=Disable

Note When detection of inhibited input is disabled by the pl*_dis bit, detection itself is disabled. So, even if H*I=L*I="H" is input, the output is H*O=L*O="H," the status bit is not set, and the DIAG terminal does not become "L." (* is U/V/W.) Refer to Table 7.2-b.

7.9.3.9. T_ILIM Write Address=1Ch / Read Address=9Ch

Bit	D15	D14	D13	D12	D11	D10	D9	D8
Symbol	–	–	t_ilim		–	–	–	–
Initial Value	0	0	0	0	0	0	0	0

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Symbol	–	–			–	–		
Initial Value	0	0	0	0	0	0	0	0

bit	Symbol	R/W	Function
[13:12]	t_ilim	R/W	Select pre-driver output current limit time "00"=8μs "01"=16μs "10"=32μs "11"= No current limit.

Note When a value that is not indicated as a set value is set, the set value for the Symbol is not updated and its previous value is maintained.

※1) "No current limit" modes for pre-driver output current limit time are not recommended to select normally becauase continuous large current may go through H*O pin and L*O pin.

7.9.3.10. FET_OPSEL Write Address=24h / Read Address=A4h

Bit	D15	D14	D13	D12	D11	D10	D9	D8
Symbol	–	–	–	–	–	vgs_op		
Initial Value	0	0	0	0	0	1	0	1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Symbol	vdsh_op				vdsl_op			
Initial Value	0	1	1	1	0	1	1	1

bit	Symbol	R/W	Function
[10:8]	vgs_op Note 1	R/W	Operation selection when detecting VGS overvoltage of external MOSFET "000"=NDIAG:Output H, continue operation [Detection disabled] "001"=NDIAG:Output "L"(hold), continue operation "010"=NDIAG:Output "L"(hold), 9ch all pre-drivers drive FET off "011"=NDIAG:Output "L"(hold), 6ch motor pre-drivers drive FET off "100"=NDIAG:Output "L"(hold), 9ch all pre-drivers drive FET off, Charge pump off "101"=NDIAG:Output "L"(hold), 9ch all pre-drivers drive FET off(hold),Charge pump off(hold)
[7:4]	vdsh_op Note 2	R/W	Operation selection when VDS abnormality of external MOSFET is detected (high side) "0000"=NDIAG:Output H, continue operation [Detection disabled] "0001"=NDIAG:Output "L"(hold), continue operation "0010"=NDIAG:Output "L"(hold), detected phase H / L pre-drivers drive FET off "0011"=NDIAG:Output "L"(hold), detected phase H / L pre-drivers drive FET off(hold) "0100"=NDIAG:Output "L"(hold), 9ch all pre-drivers drive FET off "0101"=NDIAG:Output "L"(hold), 9ch all pre-drivers drive FET off(hold) "0110"=NDIAG:Output "L"(hold), 6ch motor pre-drivers drive FET off "0111"=NDIAG:Output "L"(hold), 6ch motor pre-drivers drive FET off(hold) "1000"=NDIAG:Output "L"(hold), 9ch all pre-drivers drive FET off, Charge pump off "1001"=NDIAG:Output "L"(hold), 9ch all pre-drivers drive FET off(hold),Charge pump off(hold)
[3:0]	vdsl_op Note 3	R/W	Operation selection when VDS abnormality of external MOSFET is detected (low side) "0000"=NDIAG:Output H, continue operation [Detection disabled] "0001"=NDIAG:Output "L"(hold), continue operation "0010"=NDIAG:Output "L"(hold), detected phase H / L pre-drivers drive FET off "0011"=NDIAG:Output "L"(hold), detected phase H / L pre-drivers drive FET off(hold) "0100"=NDIAG:Output "L"(hold), 9ch all pre-drivers drive FET off "0101"=NDIAG:Output "L"(hold), 9ch all pre-drivers drive FET off(hold) "0110"=NDIAG:Output "L"(hold), 6ch motor pre-drivers drive FET off "0111"=NDIAG:Output "L"(hold), 6ch motor pre-drivers drive FET off(hold) "1000"=NDIAG:Output "L"(hold), 9ch all pre-drivers drive FET off, Charge pump off "1001"=NDIAG:Output "L"(hold), 9ch all pre-drivers drive FET off(hold), Charge pump off(hold)

Note When a value that is not indicated as a set value is set, the set value for the Symbol is not updated and its previous value is maintained.

Note 1 The selection of "010"/"011"/"100" to drive "FET OFF" is not recommended for normal use because it is not the expected operation.

Note 2 The selection of "0010"/"0100"/"0110"/"1000" to drive "FET OFF" is not recommended for normal use because it is not the expected operation.

Note 3The selection of "0010"/"0100"/"0110"/"1000" to drive "FET OFF" is not recommended for normal use because it is not expected operation.

7.9.3.11. HS_VDS_SEL Write Address=28h / Read Address=A8h

Bit	D15	D14	D13	D12	D11	D10	D9	D8
Symbol	–	–	fil_vdsh		vth_vdsuh			
Initial Value	0	0	0	0	0	1	0	0

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Symbol	vth_vdsvh				vth_vdswh			
Initial Value	0	1	0	0	0	1	0	0

bit	Symbol	R/W	Function
[13:12]	fil_vdsh	R/W	External MOSFET VDS detection filter time (high side) selection "00"=6µs "01"=8µs "10"=10µs "11"=12µs
[11:8]	vth_vdsuh	R/W	External MOSFET VDS detection threshold voltage (U-phase high side) selection "0000"=0.1V "0001"=0.2V "0010"=0.3V "0011"=0.4V "0100"=0.5V "0101"=0.6V "0110"=0.7V "0111"=0.8V "1000"=0.9V "1001"=1.0V "1010"=1.1V "1011"=1.2V
[7:4]	vth_vdsvh	R/W	External MOSFET VDS detection threshold voltage (V-phase high side) selection "0000"=0.1V "0001"=0.2V "0010"=0.3V "0011"=0.4V "0100"=0.5V "0101"=0.6V "0110"=0.7V "0111"=0.8V "1000"=0.9V "1001"=1.0V "1010"=1.1V "1011"=1.2V
[3:0]	vth_vdswh	R/W	External MOSFET VDS detection threshold voltage (W-phase high side) selection "0000"=0.1V "0001"=0.2V "0010"=0.3V "0011"=0.4V "0100"=0.5V "0101"=0.6V "0110"=0.7V "0111"=0.8V "1000"=0.9V "1001"=1.0V "1010"=1.1V "1011"=1.2V

Note
When a value that is not indicated as a set value is set, the set value for the Symbol is not updated and its previous value is maintained.

7.9.3.12. LS_VDS_SEL Write Address=2Ch / Read Address=ACh

Bit	D15	D14	D13	D12	D11	D10	D9	D8
Symbol	–	–	fil_vdsl		vth_vdsul			
Initial Value	0	0	0	0	0	1	0	0

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Symbol	vth_vdsvl				vth_vdswl			
Initial Value	0	1	0	0	0	1	0	0

bit	Symbol	R/W	Function
[13:12]	fil_vdsl	R/W	External MOSFET VDS detection filter time (low side) selection "00"=6µs "01"=8µs "10"=10µs "11"=12µs
[11:8]	vth_vdsul	R/W	External MOSFET VDS detection threshold voltage (U-phase low side) selection "0000"=0.1V "0001"=0.2V "0010"=0.3V "0011"=0.4V "0100"=0.5V "0101"=0.6V "0110"=0.7V "0111"=0.8V "1000"=0.9V "1001"=1.0V "1010"=1.1V "1011"=1.2V
[7:4]	vth_vdsvl	R/W	External MOSFET VDS detection threshold voltage (V-phase low side) selection "0000"=0.1V "0001"=0.2V "0010"=0.3V "0011"=0.4V "0100"=0.5V "0101"=0.6V "0110"=0.7V "0111"=0.8V "1000"=0.9V "1001"=1.0V "1010"=1.1V "1011"=1.2V
[3:0]	vth_vdswl	R/W	External MOSFET VDS detection threshold voltage (W-phase low side) selection "0000"=0.1V "0001"=0.2V "0010"=0.3V "0011"=0.4V "0100"=0.5V "0101"=0.6V "0110"=0.7V "0111"=0.8V "1000"=0.9V "1001"=1.0V "1010"=1.1V "1011"=1.2V

Note When a value that is not indicated as a set value is set, the set value for the Symbol is not updated and its previous value is maintained.

7.9.3.13. FET_DET_SEL Write Address=30h / Read Address=B0h

Bit	D15	D14	D13	D12	D11	D10	D9	D8
Symbol	–	–	–	–	vgshu_dis	vdshu_dis	vgslu_dis	vdslu_dis
Initial Value	0	0	0	0	0	0	0	0

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Symbol	vgshv_dis	vdshv_dis	vgslv_dis	vdslv_dis	vgshw_dis	vdshw_dis	vgslw_dis	vdslw_dis
Initial Value	0	0	0	0	0	0	0	0

bit	Symbol	R/W	Function
11	vgshu_dis	R/W	selection of VGS detection of external MOSFET (U phase high side) "0"=enable "1"=disable (No new detection, status already detected is not affected)
10	vdshu_dis	R/W	selection of VDS detection of external MOSFET (U phase high side) "0"=enable "1"=disable (No new detection, status already detected is not affected)
9	vgslu_dis	R/W	selection of VGS detection of external MOSFET (U phase low side) "0"=enable "1"=disable (No new detection, status already detected is not affected)
8	vdslu_dis	R/W	selection of VDS detection of external MOSFET (U phase low side) "0"=enable "1"=disable (No new detection, status already detected is not affected)
7	vgshv_dis	R/W	selection of VGS detection of external MOSFET (V phase high side) "0"=enable "1"=disable (No new detection, status already detected is not affected)
6	vdshv_dis	R/W	selection of VDS detection of external MOSFET (V phase high side) "0"=enable "1"=disable (No new detection, status already detected is not affected)
5	vgslv_dis	R/W	selection of VGS detection of external MOSFET (V phase low side) "0"=enable "1"=disable (No new detection, status already detected is not affected)
4	vdslv_dis	R/W	selection of VDS detection of external MOSFET (V phase low side) "0"=enable "1"=disable (No new detection, status already detected is not affected)
3	vgshw_dis	R/W	selection of VGS detection of external MOSFET (W phase high side) "0"=enable "1"=disable (No new detection, status already detected is not affected)
2	vdshw_dis	R/W	selection of VDS detection of external MOSFET (W phase high side) "0"=enable "1"=disable (No new detection, status already detected is not affected)
1	vgslw_dis	R/W	selection of VGS detection of external MOSFET (W phase low side) "0"=enable "1"=disable (No new detection, status already detected is not affected)
0	vdslw_dis	R/W	selection of VDS detection of external MOSFET (W phase low side) "0"=enable "1"=disable (No new detection, status already detected is not affected)

7.9.3.14. AMP_CTRL Write Address=40h / Read Address=C0h

Bit	D15	D14	D13	D12	D11	D10	D9	D8
Symbol	–	–	–	–	cal_amp_u	gain_amp_u		
Initial Value	0	0	0	0	0	0	1	1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Symbol	cal_amp_v	gain_amp_v			cal_amp_w	gain_amp_w		
Initial Value	0	0	1	1	0	0	1	1

BIT	SYMBOL	R/W	FUNCTION
11	CAL_AMP_U	W	OPAMP CALIBRATION SELECTION (U PHASE) "0"=INVALID "1"= EXECUTE OPAMP CALIBRATION (CLEARED REGARDLESS OF WHETHER CALIBRATION IS COMPLETED.)
[10:8]	GAIN_AMP_U	R/W	CURRENT DETECTION OPAMP GAIN SELECTION (U PHASE) "000"=x7.5 "001"=x10 "010"=x12.5 "011"=x15 "100"=x20 "101"=x27.4 "111"=x27.4
7	CAL_AMP_V	W	OPAMP CALIBRATION SELECTION (V PHASE) "0"=INVALID "1"= EXECUTE OPAMP CALIBRATION (CLEARED REGARDLESS OF WHETHER CALIBRATION IS COMPLETED.)
[6:4]	GAIN_AMP_V	R/W	CURRENT DETECTION OPAMP GAIN SELECTION (V PHASE) "000"=x7.5 "001"=x10 "010"=x12.5 "011"=x15 "100"=x20 "101"= x27.4 "111"= x27.4
3	CAL_AMP_W	W	OPAMP CALIBRATION SELECTION (W PHASE) "0"=INVALID "1"= EXECUTE OPAMP CALIBRATION (CLEARED REGARDLESS OF WHETHER CALIBRATION IS COMPLETED.)
[2:0]	GAIN_AMP_W	R/W	CURRENT DETECTION OPAMP GAIN SELECTION (W PHASE) "000"=x7.5 "001"=x10 "010"=x12.5 "011"=x15 "100"=x20 "101"= x27.4 "111"= x27.4

Note When a value that is not indicated as a set value is set, the set value for the Symbol is not updated and its previous value is maintained.

7.9.3.15. AMP_STAT_CLR Write Address=44h

Bit	D15	D14	D13	D12	D11	D10	D9	D8
Symbol	–	–	–	–	–	–	–	calu_pass_cl
Initial Value	0	0	0	0	0	0	0	0

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Symbol	–	–	–	calv_pass_cl	–	–	–	calw_pass_cl
Initial Value	0	0	0	0	0	0	0	0

bit	Symbol	R/W	Function
8	calu_pass_cl	W	Clear current detection AMP offset calibration test result flag (U phase) "0"=invalid "1"=Clear the flag (There is no need to write this bit back to zero.)
4	calv_pass_cl	W	Clear current detection AMP offset calibration test result flag (V phase) "0"=invalid "1"=Clear the flag (There is no need to write this bit back to zero.)
0	calw_pass_cl	W	Clear current detection AMP offset calibration test result flag (W phase) "0"=invalid "1"=Clear the flag (There is no need to write this bit back to zero.)

Note The clear bit of a status bit does not need to be returned to 0 after 1 is written.

7.9.3.16. AMP_STAT / Read Address=C4h

Bit	D15	D14	D13	D12	D11	D10	D9	D8
Symbol	–	–	–	cal_en	–	–	–	calu_pass
Initial Value	0	0	0	0	0	0	0	0

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Symbol	–	–	–	calv_pass	–	–	–	calw_pass
Initial Value	0	0	0	0	0	0	0	0

bit	Symbol	R/W	Function
12	cal_en	R	Current detection AMP offset calibration operation flag "0"=Calibration stopped "1"=During calibration
8	calu_pass	R	Current detection AMP offset calibration test result flag (U phase) "0"=Failed or not calibrated "1"=Pass
4	calv_pass	R	Current detection AMP offset calibration test result flag (V phase) "0"=Failed or not calibrated "1"=Pass
0	calw_pass	R	Current detection AMP offset calibration test result flag (W phase) "0"=Failed or not calibrated "1"=Pass

Note When the electric current detection AMP calibration of the executed phase is completed normally and its result is Pass, register: cal*_pass becomes "1."

When the result of the electric current detection AMP calibration of the executed phase is failure, register: cal*_pass becomes "0."

Note * is U, V, or W.

7.9.3.17. ALM_CTRL Write Address=48h / Read Address=C8h

Bit	D15	D14	D13	D12	D11	D10	D9	D8
Symbol	–	–	–	alr_op	–	–	–	–
Initial Value	0	0	0	0	0	0	0	0

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Symbol	–	–	–	–	–	–	fil_alm	
Initial Value	0	0	0	0	0	0	0	0

bit	Symbol	R/W	Function
12	alr_op	R/W	Operation selection when ALARM is detected "0"=NDIAG:Output "L",9ch all pre-drivers drive FET off "1"=NDIAG:Output "L",6ch motor pre-drivers drive FET off
[1:0]	fil_alm	R/W	ALARM digital filter setting (high side / low side common) "00"=16μs *16x2^2x(1/4MHz)+(1/4MHz) "01"=1ms Note 1000x2^2x(1/4MHz)+(1/4MHz) "10"=2ms Note 2000x2^2x(1/4MHz)+(1/4MHz) "11"=4ms Note 4000x2^2x(1/4MHz)+(1/4MHz)

7.9.3.18. QA_CTRL Write Address=4Ch / Read Address=CCh

Bit	D15	D14	D13	D12	D11	D10	D9	D8
Symbol	–	qat_op			–	–	t_qa	
Initial Value	0	0	0	1	0	0	0	0

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Symbol	–	–	–	–	–	–	–	en_qat
Initial Value	0	0	0	0	0	0	0	0

bit	Symbol	R/W	Function
[14:12]	qat_op	R/W	Operation selection when QA accumulated error is detected "001"=NDIAG:Output "L"(hold), continue operation "010"=NDIAG:Output "L"(hold),9ch all pre-drivers drive FET off(hold) "011"=NDIAG:Output "L"(hold),6ch motor pre-drivers drive FET off(hold) "100"=NDIAG:Output "L"(hold),9ch all pre-drivers drive FET off(hold),Charge pump off(hold)
[9:8]	t_qa	R/W	QA timeout period "00"=1ms "01"=2ms "10"=4ms "11"=8ms
0	en_qat	R/W	selection of QA timeout detection "0"= QA timeout detection disabled "1"= QA timeout detection enabled

Note When a value that is not indicated as a set value is set, the set value for the Symbol is not updated and its previous value is maintained.

Note This register is always rewritable, but the set value actually used by the QA timer is the value when the start command is set by qa_code of the ANSWER_SET register.

7.9.3.19. **ANSWER_SET Write Address=50h**

Bit	D15	D14	D13	D12	D11	D10	D9	D8
Symbol	–	–	–	–	–	–	–	–
Initial Value	0	0	0	0	0	0	0	0

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Symbol	qa_code				qa_dat			
Initial Value	0	0	0	0	0	0	0	0

bit	Symbol	R/W	Function
[7:4]	qa_code	W	Command selection for QA timer function "5h" = Stop command "7h" = AnsSet command "Ah" = Start command 0h-4h, 6h, 8h, 9h, Bh-Fh: QA command not assigned (If set during the QA sequence, the error accumulation counter is incremented)
[3:0]	qa_dat	W	QA timer response data setting area

7.9.3.20. **QA_COUNT / Read Address=D0h**

Bit	D15	D14	D13	D12	D11	D10	D9	D8
Symbol	–	–	–	–	acc_count			
Initial Value	0	0	0	0	0	0	0	0

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Symbol	current_seq_num				prev_expected_value			
Initial Value	0	0	0	0	1	1	1	1

bit	Symbol	R/W	Function
[11:8]	acc_count	R	Cumulative error count of QA timer function
[7:4]	current_seq_num	R	Current sequence number of QA timer function
[3:0]	prev_expected_value	R	Expected data in the previous sequence of QA timer function

7.9.3.21. BIST_DIAG Write Address=54h / Read Address=D4h

Bit	D15	D14	D13	D12	D11	D10	D9	D8
Symbol	–	–	–	–	–	–	–	–
Initial Value	0	0	0	0	0	0	0	0

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Symbol	–	–	–	rebst	–	–	–	diag_dg
Initial Value	0	0	0	0	0	0	0	0

bit	Symbol	R/W	Function
4	rebst	W	BIST restart setting "0"=No restart of LBIST / ABIST (normal) "1"=LBIST / ABIST restart execution
0	diag_dg	R/W	NDIAG function diagnosis selection by SPI communication "0"=NDIAG normal operation "1"=Force NDIAG to output "L"

Note Register: rebst is enabled only when either LBIST or ABIST is judged NG. When BIST is restarted, register: rebst is cleared. In normal operation, even if register: rebst="1" is set, BIST is not restarted.

7.9.3.22. BIST_STAT / Read Address=D8h

Bit	D15	D14	D13	D12	D11	D10	D9	D8
Symbol	–	–	–	–	–	–	–	–
Initial Value	0	0	0	0	0	0	0	0

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Symbol	–	–	lbst_flag	lbst_end	–	–	abst_flag	abst_end
Initial Value	0	0	0	0	0	0	0	0

bit	Symbol	R/W	Function
5	lbst_flag	R	LBIST result flag "0"=Failure "1"=Pass
4	lbst_end	R	LBIST end flag "0"=LBIST not finished (SPI communication is not possible while LBIST is running) "1"=LBSIT finished
1	abst_flag	R	ABIST result flag "0"=Failure "1"=Pass
0	abst_end	R	ABISTend flag "0"=ABIST not finished "1"=ABIST finished

Note When ABIST and LBIST are completed normally and the results are Pass, registers: abst_flag, lbst_ flag become "1."
When the results of ABIST and LBIST are failures, registers: abst_ flag, lbst_ flag become"0."

Note When ABIST and LBIST are completed, registers: abst_end, lbst_end become "1."
ABIST and LBIST are not completed due to abnormality, registers: abst_end, lbst_end become "0."

7.9.3.23. FET_TEST_CNT1 Write Address=5Ch / Read Address=DCh

Bit	D15	D14	D13	D12	D11	D10	D9	D8
Symbol	–	–	–	–	fet_manual_test	fet_rmidonU	fet_rmidonV	fet_rmidonW
Initial Value	0	0	0	0	0	0	0	0

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Symbol	ft_save_cl	_	ft_ndiag_sel	ft_comp_sel	fet_test_type1	fet_test_type0	fet_test_start	fet_test_stop
Initial Value	0	0	0	0	0	0	0	0

bit	Symbol	R/W	Function
11	fet_manual_test	R/W	Mode selection for VDS detection and VDS detection comparator output. (acceptable when fet_test_unlock = "H") "0"=Normal operation "1"= Disable VDS detection and set VDS detection comparator output to FET test mode
10	fet_rmidonU	R/W	Control the U-phase mid-voltage generating resistors. (acceptable when fet_test_unlock = "H") "0"=Turn off U-phase mid-voltage generating resistors. "1"=Turn on U-phase mid-voltage generating resistors.
9	fet_rmidonV	R/W	Control the V-phase mid-voltage generating resistors. (acceptable when fet_test_unlock = "H") "0"=Turn Off V-phase mid-voltage generating resistors. "1"=Turn On V-phase mid-voltage generating resistors.
8	fet_rmidonW	R/W	Control the W-phase mid-voltage generating resistors. (acceptable when fet_test_unlock = "H") "0"=Turn Off W-phase mid-voltage generating resistors. "1"=Turn On W-phase mid-voltage generating resistors.
7	ft_save_cl	R/W	Clear VDS comparator output (after noise filter) of VDS_COMP_STAT register and error flag FET_TEST_STAT / fet_test_err saved by FET_TEST. "0"=Invalid "1"=Clear (No need to write back to 0. 0 can be read when reading)
5	ft_ndiag_sel	R/W	Select whether to output to NDIAG when executing FET_TEST "0"=Does not output to NDIAG when executing FET_TEST. "1"= Set NDIAG to "L" during FET_TEST and when expected value mismatch is detected
4	ft_comp_sel	R/W	Select the contents to read from VDS_COMP_STAT "0"=VDS detection comparator output saved with FET_TEST (after noise filter) "1"= Current value of VDS detection comparator (after noise filter)
[3:2]	fet_test_type[1:0]	R/W	Select the test type to be executed with FET_TEST "00"=Type A "01"=Type B "10"=Type C "11"=Type D
1	fet_test_start	R/W	Start FET_TEST sequence (acceptable when fet_test_unlock = "H") "0"=Invalid "1"=Sequence start (There is no need to write back to 0. 0 can be read when reading.)
0	fet_test_stop	R/W	Stop the FET_TSET sequence "0"=Invalid "1"=Stop sequence (fet_test_stop has priority if set at the same time as fet_test_start)

Note fet_manual_test, fet_rmidon[U,V,W] bits and fet_test_start bit can be set only when fet_test_unlock="H."

Note fet_manual_test, fet_rmidon[U,V,W] bits cannot be set when fet_test_unlock="L." A previously set value is cleared by fet_test_unlock="L."

7.9.3.24. FET_TEST_CNT2 Write Address=60h / Read Address=E0h

Bit	D15	D14	D13	D12	D11	D10	D9	D8
Symbol	—	—	—	fet_test_unlock	—	typed_uhd	—	typed_uld
Initial Value	0	0	0	0	0	0	0	0

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Symbol	—	typed_vhd	—	typed_vld	—	typed_whd	—	typed_wld
Initial Value	0	0	0	0	0	0	0	0

bit	Symbol	R/W	Function
12	fet_test_unlock	R/W	Allow test operation by FET_TEST (both automatic / manual) "0"=Does not accept start of FET_TEST operation, forcibly cancels test operation when set during FET_TEST execution "1"= Accept start of FET_TEST operation
10	typed_uhd	R/W	Specify U-phase high-side pre-driver output value for Type D test sequence "0"=off "1"=on
8	typed_uld	R/W	Specify U-phase low-side pre-driver output value for Type D test sequence "0"=off "1"=on
6	typed_vhd	R/W	Specify V-phase high-side pre-driver output value for Type D test sequence "0"=off "1"=on
4	typed_vld	R/W	Specify V-phase low-side pre-driver output value for Type D test sequence "0"=off "1"=on
2	typed_whd	R/W	Specify W-phase high-side pre-driver output value for Type D test sequence "0"=off "1"=on
0	typed_wld	R/W	Specify W-phase low-side pre-driver output value for Type D test sequence "0"=off "1"=on

Note When a phase which is set to ON for both high and low sides, the phase is controlled to OFF for high and low sides.

7.9.3.25. **FET_TEST_STAT / Read Address=E4h**

Bit	D15	D14	D13	D12	D11	D10	D9	D8
Symbol	–	–	–	–	–	–	–	–
Initial Value	0	0	0	0	0	0	0	0

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Symbol	–	–	fet_auto_test	fet_test_err	–	ft_seq_num2	ft_seq_num1	ft_seq_num0
Initial Value	0	0	0	0	0	0	0	0

bit	Symbol	R/W	Function
5	fet_auto_test	R	FET_TEST sequence execution flag "0"=FET_TEST is stopped "1"=FET_TSET is running
4	fet_test_err	R	Whether or not an expected value mismatch occurred during execution of FET_TEST (only valid for Type A / Type B / Type C) "0"=No expected value mismatch detected "1"=Expected value mismatch detected
[2:0]	ft_seq_num[2:0]	R	Sequence number executed last by FET_TEST (when the expected value mismatch occurs, it is the step number where the mismatch occurred)

7.9.3.26. VDS_COMP_STAT / Read Address=E8h

Bit	D15	D14	D13	D12	D11	D10	D9	D8
Symbol	–	–	–	–	–	compout_uh	–	compout_ul
Initial Value	0	0	0	0	0	0	0	0

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Symbol	–	compout_vh	–	compout_vl	–	compout_wh	–	compout_wl
Initial Value	0	0	0	0	0	0	0	0

bit	Symbol	R/W	Function	
			ft_comp_sel="L"	ft_comp_sel="H"
10	compout_uh	R	Last saved data with FET_TEST (U phase high side) "0"= FET_TEST saved data is "L" "1"= FET_TEST saved data is "H"	External MOSFET VDS monitor (U phase high side) "0" = Comparator output (after filter) is "L" "1" = Comparator output (after filter) is "H"
8	compout_ul	R	Last saved data with FET_TEST (U phase low side) "0"= FET_TEST saved data is "L" "1"= FET_TEST saved data is "H"	External MOSFET VDS monitor (U phase low side) "0" = Comparator output (after filter) is "L" "1" = Comparator output (after filter) is "H"
6	compout_vh	R	Last saved data with FET_TEST (V phase high side) "0"= FET_TEST saved data is "L" "1"= FET_TEST saved data is "H"	External MOSFET VDS monitor (V phase high side) "0" = Comparator output (after filter) is "L" "1" = Comparator output (after filter) is "H"
4	compout_vl	R	Last saved data with FET_TEST (V phase low side) "0"= FET_TEST saved data is "L" "1"= FET_TEST saved data is "H"	External MOSFET VDS monitor (V phase low side) "0" = Comparator output (after filter) is "L" "1" = Comparator output (after filter) is "H"
2	compout_wh	R	Last saved data with FET_TEST (W phase high side) "0"= FET_TEST saved data is "L" "1"= FET_TEST saved data is "H"	External MOSFET VDS monitor (W phase high side) "0" = Comparator output (after filter) is "L" "1" = Comparator output (after filter) is "H"
0	compout_wl	R	Last saved data with FET_TEST (W phase low side) "0"= FET_TEST saved data is "L" "1"= FET_TEST saved data is "H"	External MOSFET VDS monitor (W phase low side) "0" = Comparator output (after filter) is "L" "1" = Comparator output (after filter) is "H"

7.9.3.27. DUMMY Write Address=7Ch / Read Address=FCh

Bit	D15	D14	D13	D12	D11	D10	D9	D8
Symbol	dmy15	dmy14	dmy13	dmy12	dmy11	dmy10	dmy9	dmy8
Initial Value	0	0	0	0	0	0	0	0

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Symbol	dmy7	dmy6	dmy5	dmy4	dmy3	dmy2	dmy1	dmy0
Initial Value	0	0	0	0	0	0	0	0

bit	Symbol	R/W	Function
[15:0]	dummy	R/W	dummy bit

8. Absolute maximum ratings

Voltages are all based on AGND unless otherwise specified.

Parameter	Applied Pins	Symbol	Ratings	Unit	Condition
Power supply voltage	VB	Vb	-0.3 to 28(DC), 28 to 40(≤1s)	V	–
	VCPH	Vcph	-0.3 to 44.5(DC), 44.5 to 60(≤1s)	V	–
	VCC	Vcc	-0.3 to 6	V	–
	VCC_OP	Vccop	-0.3 to 6	V	–
Voltage difference between AGND-PGND	AGND1, AGND2, PGND	Vgnd	-0.3 to 0.3	V	–
Input voltage	HS	Vin1	-18 to 28(DC), 28 to 40(≤1s)	V	Vin1≤40V
	HUS, HVS, HWS	Vin2	-7 to Vcph +0.3, -14 to -7(≤1μs,20kHz)	V	Vin2≤40V Voltage between HUO-HUS, HVO-HVS, HWO-HWS ≤ 40V
	LUS, LVS, LWS	Vin3	-7 to Vcph +0.3, -10 to -7(≤1μs,20kHz)		Vin3≤40V Voltage between LUO-LUS, LVO-LVS, LWO- LWS ≤ 40V
	LUI, LVI, LWI, HUI, HVI, HWI, SCLK, NSCS, SI, ALARM	Vin4	-0.3 to Vcc+0.3	V	Vin4≤6V
	AMPU_P, AMPV_P, AMPW_P, AMPU_N, AMPV_N, AMPW_N	Vin5	-7 to 28(DC), 28 to 40(≤1s), -10 to -7(≤1μs,20kHz)	V	–
Output voltage	SR1O, SR2O, SR3O, CP1H, CP2H	Vout1	-0.3 to Vcph+0.3	V	Vout1≤60V
	HUO, HVO, HWO	Vout2	-7 to Vcph+0.6(DC), -14 to -7(≤1μs,20kHz)	V	Vout2≤60V Voltage between HUO-HUS, HVO-HVS, HWO-HWS ≤ 40V
	CP1L, CP2L	Vout3	-0.3 to Vb+0.3	V	Vout3≤28V(DC), Vout3≤40V(≤1s)
	LUO, LVO, LWO	Vout4	-7 to Vcph+0.3(DC), -10 to -7(≤1μs,20kHz)	V	Vout4≤60V Voltage between LUO-LUS, LVO-LVS, LWO- LWS ≤ 40V
	AMPU_O, AMPV_O, AMPW_O	Vout5	-0.3 to Vccop+0.3	V	Vout5≤6V
	NDIAG, SO	Vout6	-0.3 to Vcc+0.3	V	Vout6≤6V
Input current	HUS, HVS, HWS	Iin1	1.2	A	t=200ns (Reference values)
	AMPU_P,AMPV_P,AMPW_P, AMPU_N,AMPV_N,AMPW_N	Iin2	-0.5 to 2	mA	–
Output current	HUO, HVO, HWO,LUO, LVO, LWO	Iout1	±20	mA	–
		Iout2	±1	A	Time shorter than output current switching time (Tsw)
	AMPU_O, AMPV_O, AMPW_O	Iout3	±5	mA	–
	NDIAG, SO	Iout4	±10	mA	–
Operating ambient temperature	–	Ta	-40 to 150	°C	–
Junction temperature (Maximum value)	–	Tj	175	°C	–
Storage temperature	–	Tstg	-55 to 150	°C	–
Allowable power dissipation	–	PD	1.096	W	Mounted on board, JEDEC 4 layers , Ta=150°C, Rthj-a=30°C /W

≪Notes for users≫

・ The absolute maximum rating is a standard that must not be exceeded even for a moment and even a single item must not be exceeded for use.

・ Electric current flowing into this IC is shown with '+' and electric current flowing out of this IC is shown with '－.'

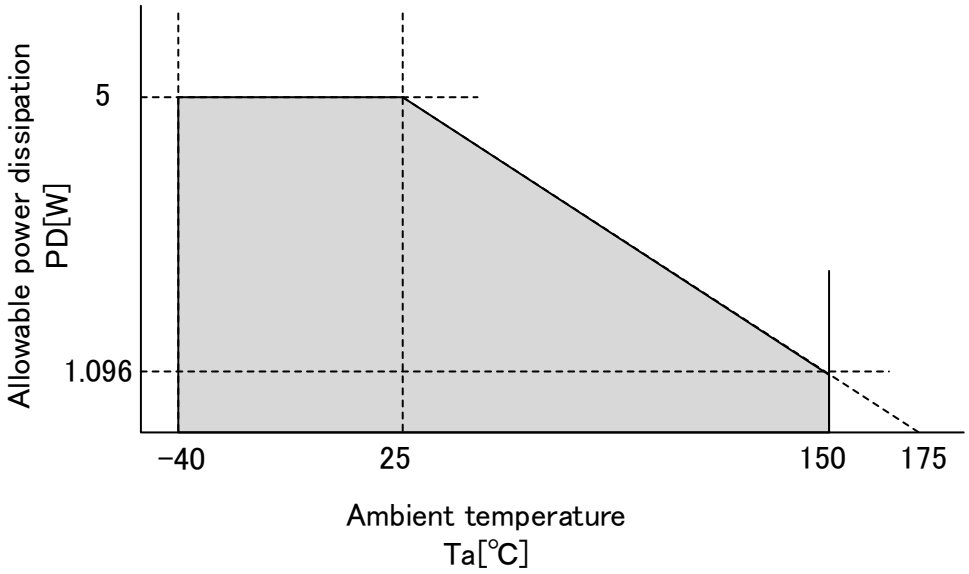
・ Absolute maximum rating values limit the ranges in the condition fields.

・ Marks in the above maximum absolute maximum ratings (Vb, Vcph, Vcc, Vccop) mean the added voltages and output voltages of respective terminals (VB, VCPH, VCC, VCC_OP).

・ The slew rates of Vb and Vcc shall be within the following ranges.

Vb: less than 8V/μs, Vcc: less than 0.3V/μs

・ This product assumes to be used with a 12V battery.



Allowable dissipation curve

(For reference)
Board: JEDEC 4 layers board
Thermal resistance: 22.8°C/W

9. Electrical characteristics

Operating voltage ranges

Parameter	Applied pin	Symbol	Operating voltage range	Unit	Condition
Input voltage	VB	Vb	4.5 to 28	V	DC
	VCC	Vcc	3.0 to 5.5	V	DC
	VCC_OP	Vccop	3.0 to 5.5	V	DC

Note This product assumes to be used with a 12V battery.

Note It is not recommended to use this product at Vb<3.6V all the time.

Consumption current

Vb=4.5 to 28V, Vcc=3.0 to 5.5V, Vccop=3.0 to 5.5V, Tj=-40 to 175°C unless specified otherwise

Parameter	Applied pin	Symbol	Test conditions	Min	Typ.	Max	Unit
Standby current (Vb)	VB	Istb1	Vb=12V, Vcc=Vccop=0V, -40≤Ta≤85°C	–	0.05	3.5	μA
		Istb2	Vb=12V, Vcc=Vccop=0V, 85≤Ta≤125°C	–	–	6.0	μA
		Istb3	Vb=12V, Vcc=Vccop=0V, 125≤Ta≤150°C	–	–	7.0	μA
Supply current (Vb)	VB	Ib1	Vb=13.5V HUO, HVO, HWO=20kHz LUO, LVO, LWO=20kHz Pre-driver output load: Rload=0Ω、Cload=15000pF Safety Relay output load: Rload=1.5kΩ、Cload=15000pF	–	90	180	mA
		Ib2	Vb=17V HUO,HVO,HWO=20kHz LUO,LVO,LWO=20kHz Pre-driver output load: Rload=0Ω、Cload=15000pF Safety Relay output load: Rload=1.5kΩ、Cload=15000pF	–	60	120	mA
		Ib3	Vb=28V HUO,HVO,HWO=20kHz LUO,LVO,LWO=20kHz Pre-driver output load: Rload=0Ω、Cload=15000pF Safety Relay output load: Rload=1.5kΩ、Cload=15000pF	–	60	120	mA
Supply current (Vcc)	VCC	Icc1	Vcc=5V	4	8	16	mA
		Icc2	Vcc=3.3V	1.2	2.5	5.0	mA
Supply current (Vccop)	VCC_OP	Iccop1	Vccop=5V	3	6	12	mA
		Iccop2	Vccop=3.3V	3	6	12	mA

Note A drop in Vcc leads to a stand-by state. The electric current in the stand-by state is provided by Istb1, Istb2, Istb3.

Note External constants of the charge pumps of Ib1, Ib2, Ib3 are those of the application circuit example.

Charge pump circuit

Vb=4.5 to 28V, Vcc=3.0 to 5.5V, Tj=-40 to 175°C unless otherwise specified

Parameter	Applied pin	Symbol	Test conditions	Min	Typ.	Max	Unit	Remark
Output voltage	VCPH	Vcph1	Vb=4.5 to 5.5V Output load =28mA	Vb+5.6	–	3×VB-1.5	V	–
		Vcph2	Vb=5.5 to 7V Output load =28mA	Vb+6.1	–	3×VB-1.5	V	–
		Vcph3	Vb=7 to 28V Output load =28mA	Vb+9.6	Vb+14	Vb+16.5	V	–
Rise time	VCPH	Tcp	From 10% to 90% of VCPH voltage	–	–	1	ms	–
Operating frequency	–	clk_cp	–	185	286	386	kHz	–
Pre-charging time	–	Tpch_cp	–	290	400	620	μs	–
Enable time for pre-driver	–	Tpre_en	The time between when register [en_cp="1"] is written and when pre-driver is allowed to turn on	0.85	1.2	1.9	ms	–

Note Reference values of Ccp (charge pump capacitance), Cvcph (charge pump voltage terminal capacitance) are as follows.
Ccp = 0.47 [μF],Cvcph = 2.2 [μF]
Determine the external circuits after a sufficient evaluation and check on a unit board, assuming the conditions of the operating environment.

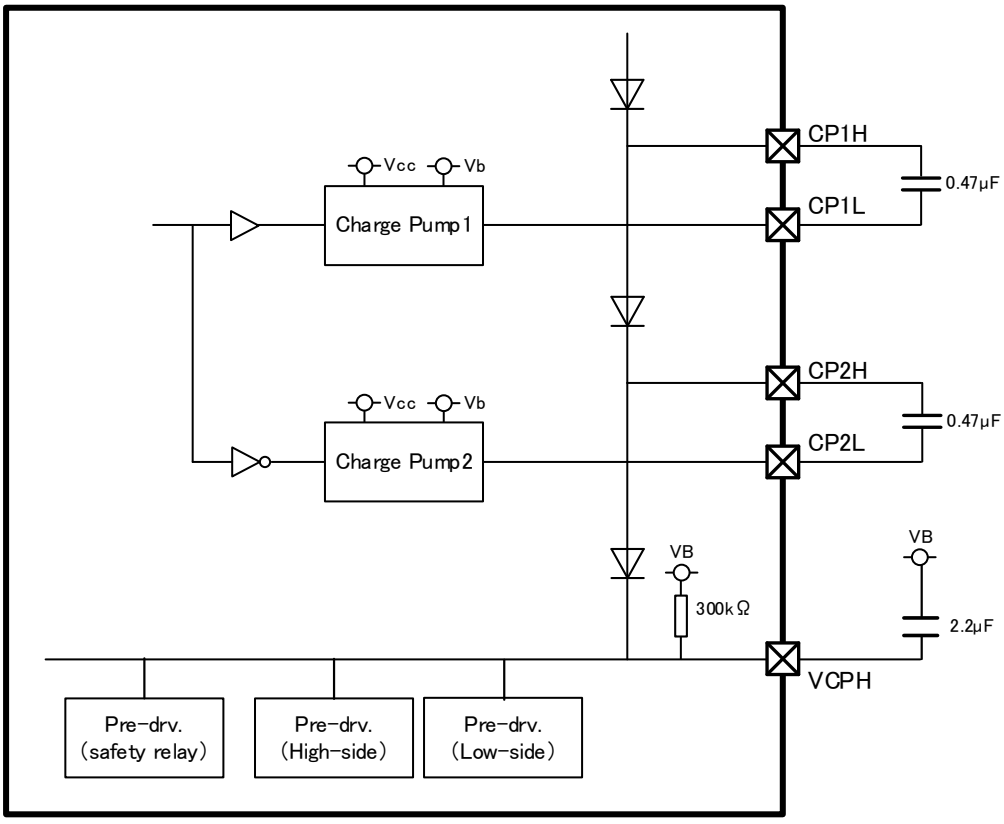


Fig. 9-a Charge pump application circuit diagram

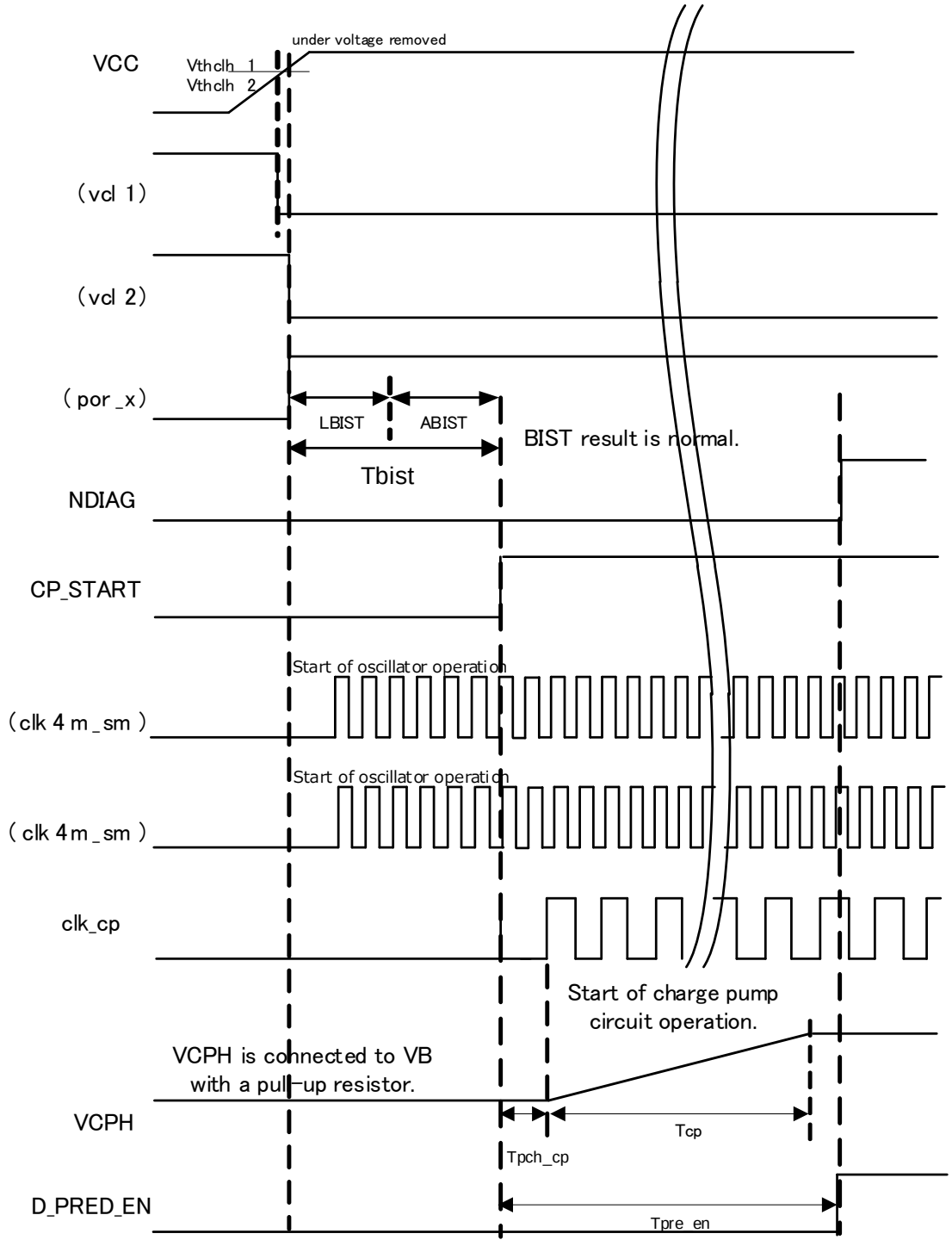


Fig. 9-b Charge pump circuit timing chart

Note Since the initial value of the en_cp bit is 1, the charge pump is enabled as soon as ABIST is successfully completed.

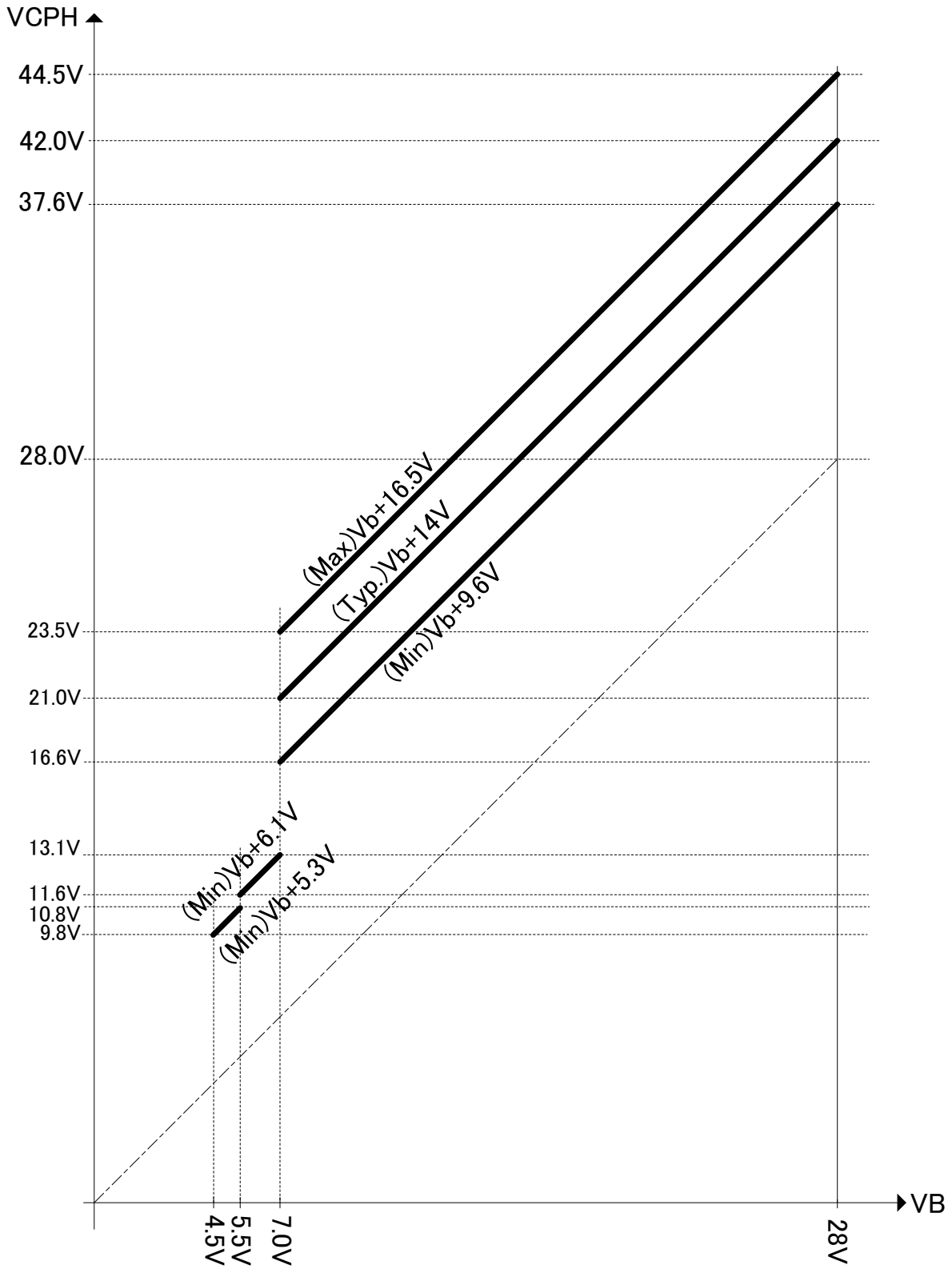


Fig. 9-c Charge pump voltage dependence

Pre-driver circuit

Vb=4.5 to 28V, Vcc=3.0 to 5.5V, Tj=-40 to 175°C unless specified otherwise

Parameter	Applied pin	Symbol	Test conditions	Min	Typ.	Max	Unit	Remark
High level input current	HUI, HVI, HWI, LUI, LVI, LWI	Iih	Vcc= 5.0V, Vin = 5.0V	50	100	200	μA	–
Low level input current	HUI, HVI, HWI, LUI, LVI, LWI	Iil	Vcc = 5.0V, Vin = 0V	-5	–	5	μA	–
High level input detection voltage	HUI, HVI, HWI, LUI, LVI, LWI	Vih	–	0.75× Vcc	–	–	V	–
Low level input detection voltage	HUI, HVI, HWI, LUI, LVI, LWI	Vil	–	–	–	0.25× Vcc	V	–
Output voltage1	HUO,HVO,HWO	Voh1	Voltage between HUO(HVO, HWO) and HUS(HVS, HWS), Iload=-100μA Vb=6.5 to 28V, HUS(HVS, HWS)=0V	6.7	10	12	V	–
		Voh1_2	Voltage between HUO(HVO, HWO) and HUS(HVS, HWS) Iload=-100μA Vb=4.5 to 7.0V HUS(HVS, HWS)=0V	Vcph--0.3	–	Vcph	V	–
		Vol1	Voltage between HUO(HVO, HWO) and HUS(HVS,HWS), Iload=100μA	0	–	0.2	V	–
Output voltage2+	LUO, LVO, LWO	Voh2	Voltage between LUO(LVO, LWO) and LUS(LVS,LWS), LUS(LVS,LWS)=0 V, Iload=-100μA	6.7	11	12	V	–
		Vol2	Voltage between LUO(LVO, LWO) and LUS(LVS,LWS) =0V, Iload=100μA	0	–	0.2	V	–
Output voltage3	SR1O, SR2O, SR3O	Voh3	Iload=-100μA	Vcph-0.1	–	Vcph	V	
		Vol3	Iload=100μA	–	–	0.9	V	
Output resistance1	HUO,HVO,HWO	Rohh	HUI,HVI,HWI = VCC Iload = -50 mA	–	4.4	12	Ω	–
		Roh l	HUI,HVI,HWI = 0V Iload = 50 mA	–	1.2	3	Ω	–
Output resistance2	LUO, LVO, LWO	Rolh	LUI,LVI,LWI = VCC Iload = -50 mA	–	4.4	12	Ω	–
		Roll	LUI,LVI,LWI = 0V Iload = 50 mA	–	1.2	3	Ω	–

Note Safety relay output: SR1O, SR2O, SR3O do not contain pull-down resistors. When pull-down resistors are required for the system, add them on the ECU board. When connecting a pull-down resistor close to MOSFET, determine the resistor's constant taking into consideration the drop of the output voltage of the safety relay.

Note For the measurement circuit, see Fig. 9-d.

Vb=4.5 to 28V, Vcc=3.0 to 5.5V, Tj=-40 to 175°C unless specified otherwise

Parameter	Applied pin	Symbol	Test conditions	Min	Typ.	Max	Unit	Remark
Output resistance	SR1O, SR2O, SR3O	Rosh	srly1_drv="1", srly2_drv="1", srly3_drv="1" Iload=-5mA	350	500	750	Ω	–
		Rosl	srly1_drv="0", srly2_drv="0", srly3_drv="0" Rosl =Vd/4mA	350	500	750	Ω	Refer to Fig. 9-f
Pull-down resistance 1	HUO,HVO,HWO	Rpd1	ALARM=0V	25	50	100	kΩ	–
Pull-down resistance 2	LUO, LVO, LWO	Rpd2	ALARM=0V	25	50	100	kΩ	–
On reverse connection VB leakage current	SR1O, SR2O, SR3O	Iol	SR1O, SR2O, SR3O=-18V PGND=0V	0	0.01	1.0	μA	–
Output limit current	HUO,HVO,HWO ,LUO, LVO, LWO	Io_lmth	When turned on, after Tsw	–	-10	–	mA	Refer to Fig. 9-e
		Io_lmtl	When turned off, after Tsw	–	10	–	mA	Refer toFig. 9-e
Output current switching time	HUO,HVO,HWO,LUO, LVO, LWO	Tsw0	–	5	8	14	μs	t_ilim = "00" Refer to Fig. 9-e
		Tsw1	–	10	16	28	μs	t_ilim = "01" Refer toFig. 9-e
		Tsw2	–	20	32	56	μs	t_ilim = "10" Refer to Fig. 9-e
When turned on, input propagation delay time	HUI, HVI, HWI, HUO,HVO,HWO	Tdonh	–	20	120	250	ns	Refer to Fig.9-d and Fig. 9-e
	LUI, LVI, LWI, LUO, LVO, LWO	Tdonl	–	20	120	250	ns	Refer to Fig.9-d and Fig. 9-e
When turned off, input propagation delay time	HUI, HVI, HWI, HUO,HVO,HWO	Tdoffh	–	20	180	300	ns	Refer to Fig.9-d and Fig. 9-e
	LUI, LVI, LWI, LUO, LVO, LWO	Tdoffl	–	20	180	300	ns	Refer to Fig.9-d and Fig. 9-e
Input propagation delay time difference	HUI, HVI, HWI, LUI, LVI, LWI, HUO,HVO,HWO ,LUO, LVO, LWO	Dtd	Tdonh-Tdoffl, Tdonl-Tdoffh	-125	–	125	ns	Time difference between high side and low side (U/V/W)

Note To safety relay output: SR1O, SR2O, SR3O, connect an external series resistor of 1.5kΩ or larger.

Note Safety relay output: SR1O, SR2O, SR3O do not contain pull-down resistors. When pull-down resistors are required for the system, add them on the ECU board. When connecting a pull-down resistor close to MOSFET, determine the resistor's constant taking into consideration the drop of the output voltage of the safety relay.

Note For the measurement circuit, see Fig. 9-d

Note Specifications shown in (brackets) are design values and not tested for deliv

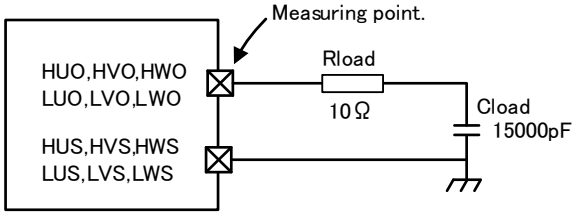


Fig. 9-d Measurement circuit diagram (high side/low side)

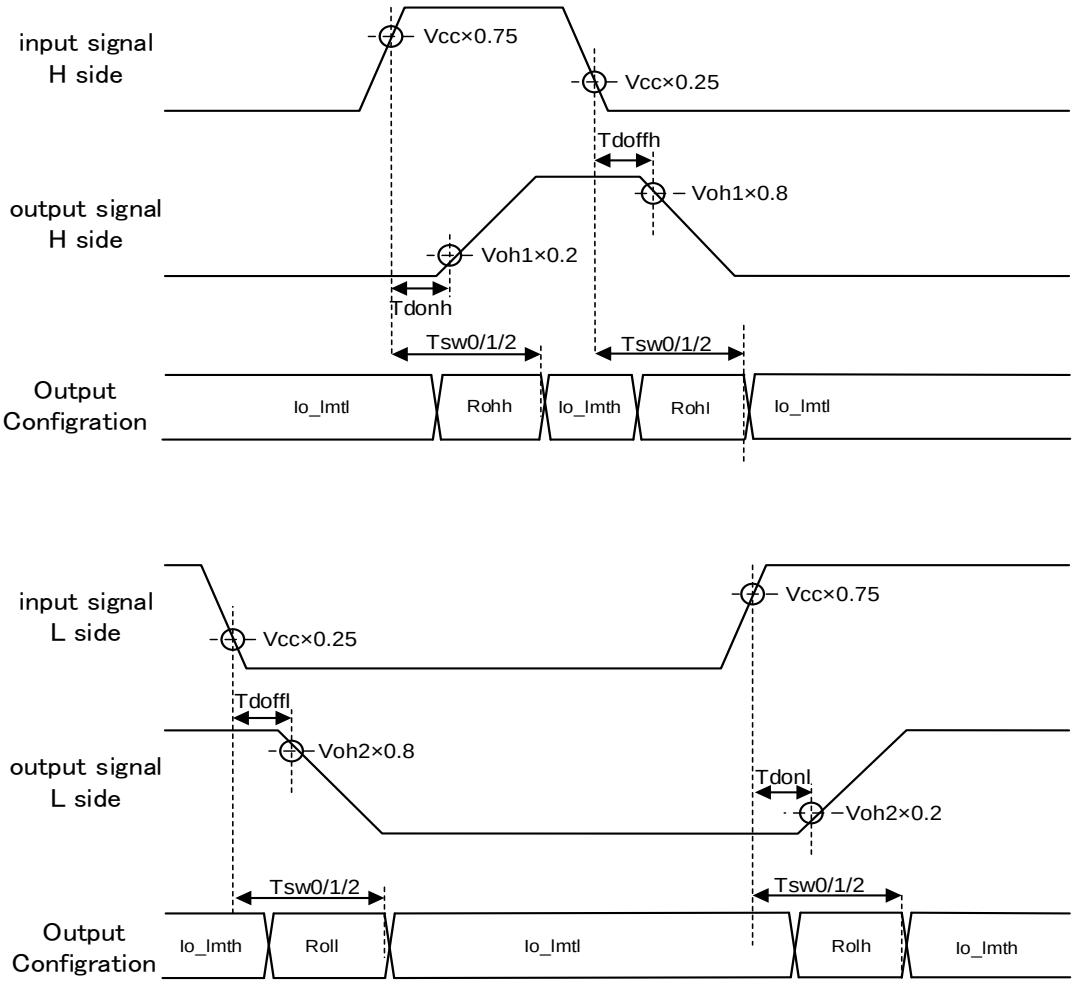


Fig. 9-e Timing charts of output current switching time, input propagation delay time

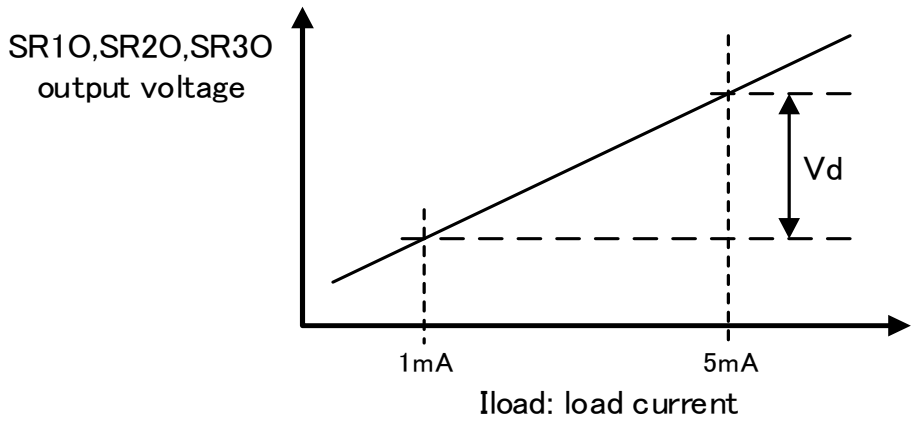


Fig. 9-f How to measure SR1O,SR2O,SR3O output resistance

Current detection circuit

Vb=4.5 to 28V, Vccop=3.0 to 5.5V, Tj=-40 to 175°C unless specified otherwise

Parameter	Applied pin	Symbol	Test conditions	Min	Typ.	Max	Unit	Remark
Input offset voltage 1	AMPU_P, AMPV_P, AMPW_P, AMPU_N, AMPV_N, AMPW_N	Voff1	After calibration, Ta=25°C Gain=15 Comvin=0V Iload=0.5mA	-1	–	1	mV	gain_amp_u="011", gain_amp_v="011", gain_amp_w="011"
Input offset voltage 2	AMPU_P, AMPV_P, AMPW_P, AMPU_N, AMPV_N, AMPW_N	Voff2	Before calibration, Ta=25°C Gain=15 Comvin=0V Iload=0.5mA	-7	–	7	mV	gain_amp_u="011", gain_amp_v="011", gain_amp_w="011"
Input offset voltage temperature characteristic 1	AMPU_P, AMPV_P, AMPW_P, AMPU_N, AMPV_N, AMPW_N	VoffdT1	After calibration, Gain=15 Comvin=0V Iload=0.5mA	(-10)	–	(10)	µV/°C	gain_amp_u="011", gain_amp_v="011", gain_amp_w="011" shown in (brackets) are design values
Input offset voltage temperature characteristic 2	AMPU_P, AMPV_P, AMPW_P, AMPU_N, AMPV_N, AMPW_N	VoffdT2	Before calibration, Gain=15, Comvin=0V Iload=0.5mA	(-10)	–	(10)	µV/°C	gain_amp_u="011", gain_amp_v="011", gain_amp_w="011" shown in (brackets) are design values
Input bias current	AMPU_P, AMPV_P, AMPW_P, AMPU_N, AMPV_N, AMPW_N	Iin	Measurement target terminal = 0V	-100	–	100	µA	–
Output voltage 1	AMPU_O, AMPU_O, AMPU_O	Vohop	Gain=15 Vinr=0.1×Vccop Iload = -500µA	Vccop -0.15	–	Vccop	V	–
		Volop	Gain=15 Vinr=-0.1×Vccop Iload = +500µA	0	–	0.15	V	–
Reference voltage	–	Vref	–	(Typ.-9)	Vccop/2	(Typ.+9)	mV	shown in (brackets) are design values
Reference temperature characteristic	–	Vref_dT	–	(-10)	–	(10)	µV/°C	shown in (brackets) are design values
GAIN	AMPU_P, AMPV_P, AMPW_P, AMPU_N, AMPV_N, AMPW_N, AMPU_O, AMPV_O, AMPW_O	Gain0	Vinr=-0.5V to 0.5V, Iload=No load	-1%	7.5	1%	–	gain_amp_u="000", gain_amp_v="000", gain_amp_w="000"
		Gain1	Vinr=-0.5V to 0.5V, Iload=No load	-1%	10	1%	–	gain_amp_u="001", gain_amp_v="001", gain_amp_w="001"
		Gain2	Vinr=-0.5V to 0.5V, Iload=No load	-1%	12.5	1%	–	gain_amp_u="010", gain_amp_v="010", gain_amp_w="010"
		Gain3	Vinr=-0.5V to 0.5V, Iload=No load	-1%	15	1%	–	gain_amp_u="011", gain_amp_v="011", gain_amp_w="011"
		Gain4	Vinr=-0.5V to 0.5V, Iload=No load	-1%	20	1%	–	gain_amp_u="100", gain_amp_v="100", gain_amp_w="100"
		Gain5	Vinr=-0.5V to 0.5V, Iload=No load	-1%	27.4	1%	–	gain_amp_u="101", gain_amp_v="101", gain_amp_w="101"

Note For the amplifier configuration, use the polarity in Fig. 9-g.

Note Specifications shown in (brackets) are design values and not tested for delivery.

Vb=4.5 to 28V, Vccop=3.0 to 5.5V, Tj=-40 to 175°C unless specified otherwise

Parameter	Applied pin	Symbol	Test conditions	Min	Typ.	Max	Unit	Remark
Slew rate	AMPU_O, AMPV_O, AMPW_O	Sr1	VCC_OP=5.0V Gain=15 Rload=1kΩ,Cload=220pF Slew rate from 20% of Vout to 80%	4.5	10	20	V/μs	Refer to Fig. 9- Gain is set to register by SPI.
			VCC_OP=3.3V Gain=15 Rload=1kΩ,Cload=220pF Slew rate from 20% of Vout to 80%	2.5	10	20	V/μs	Refer to Fig. 9-h Gain is set to register by SPI.
		Sr2	VCC_OP=5.0V Gain=15 Rload=1kΩ,Cload=220pF Slew rate from 20% of Vout to 80%	-20	-10	-4.5	V/μs	Refer to Fig. 9-h Gain is set to register by SPI.
			VCC_OP=3.3V Gain=15 Rload=1kΩ,Cload=220pF Slew rate from 20% of Vout to 80%	-20	-10	-2.5	V/μs	Refer to Fig. 9-h Gain is set to register by SPI.
Settling time	AMPU_O, AMPV_O, AMPW_O	Tset	Rload=1kΩ,Cload=220pF Time for output voltage to converge to ±2%.	–	–	(1.5)	μs	shown in (brackets) are design values
Input common mode voltage	AMPU_P, AMPV_P, AMPW_P, AMPU_N, AMPV_N, AMPW_N	Comvin	Input range where amplifier outputs can ensure ±1% gain error with AMP*_P and AMP*_N shorted	-0.5	–	2.0	V	–
PSRR	VCC_OP	Psrrop	1KHz input to VCC_OP, but excluding the effect of VREF	–	(60)	–	dB	shown in (brackets) are design values
CMRR	AMPU_P, AMPV_P, AMPW_P, AMPU_N, AMPV_N, AMPW_N, AMPU_O, AMPV_O, AMPW_O	Cmrrop	Gain=15, Comvin=200mVp-p,100KHz	(80)	(100)	–	dB	shown in (brackets) are design values
Offset calibration time	–	$T_{ampofscal}$	–	–	–	108	μs	–

Note For the amplifier configuration, use the polarity in Fig. 9-g

Note Specifications shown in (brackets) are design values and not tested for delivery.

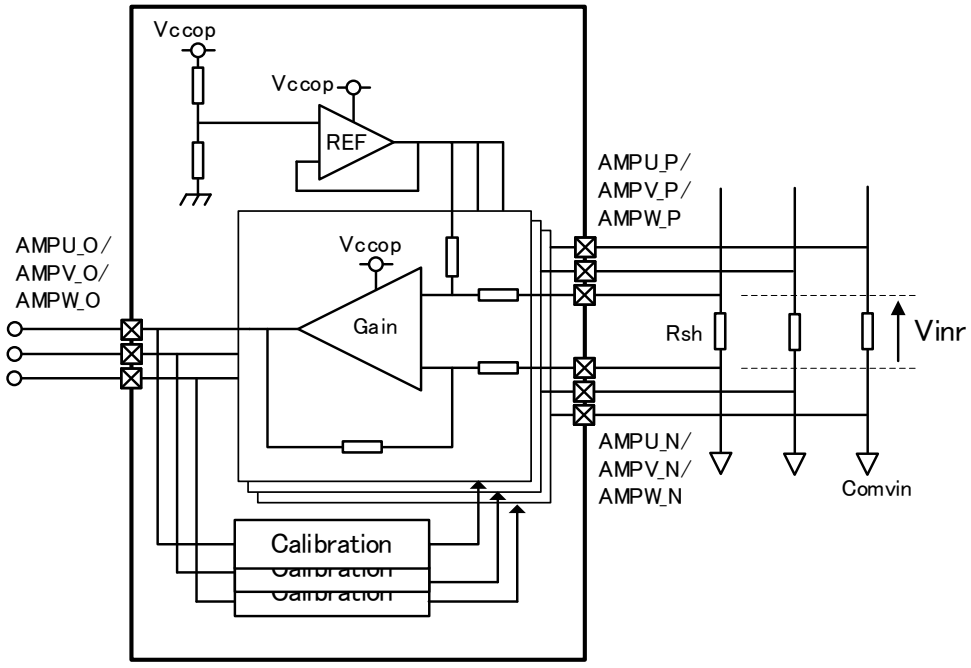


Fig. 9-g Measurement circuit diagram

※SR1 = 0.6x(Vccop−0.3)/ΔTr
※SR2 = −0.6x(Vccop−0.3)/ΔTf

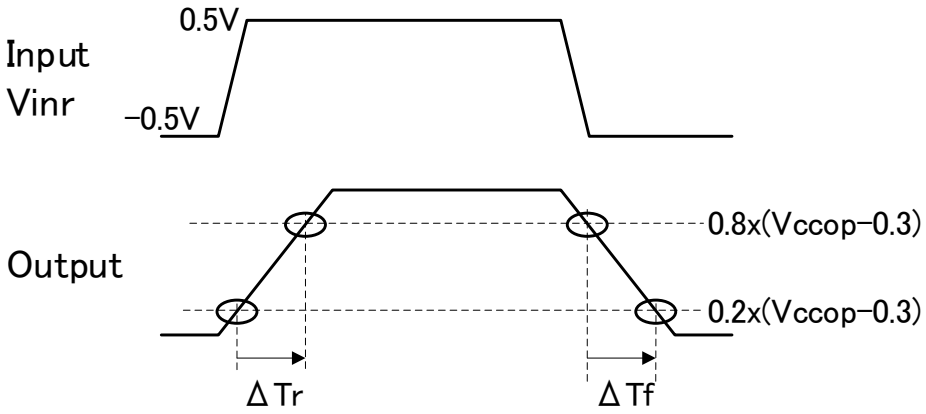


Fig. 9-h Slew rate timing

Oscillation circuit

Vb=4.5 to 28V, Vcc=3.0 to 5.5V, Tj=-40 to 175°C unless specified otherwise

Parameter	Applied pin	Symbol	Test conditions	Min	Typ.	Max	Unit	Remark
Internal oscillation frequency	–	Fc	–	2.6	4	5.4	MHz	–
Frequency for monitor	–	Fcsm	–	2.6	4	5.4	MHz	–

Abnormality detection circuit

Vb=4.5 to 28V, Vcc=3.0 to 5.5V, Tj=-40 to 175°C unless specified otherwise

Parameter	Applied pin	Symbol	Test conditions	Min	Typ.	Max	Unit	Remark
VCC undervoltage detection threshold 1, 2	VCC	Vthcll1, Vthcll2	–	2.55	2.75	2.95	V	–
VCC undervoltage detection threshold 1,2 for removal		Vthclh1, Vthclh2	–	2.65	2.85	3.05	V	–
Filtering time for VCC undervoltage	VCC	Tcl	–	10	20	40	μs	–
VB undervoltage detection threshold	VB	Vthbll	–	3.6	3.9	4.2	V	–
Threshold for VB undervoltage detection removal		Vthblh	–	3.9	4.2	4.5	V	–
Filtering time for VB undervoltage detection		Tbl	–	12	20	34	μs	–
VCPH overvoltage detection threshold	VCPH	Vthcphhh	–	53.0	56.0	59.0	V	–
Threshold for VCPH overvoltage detection removal		Vthcphhl	–	52.0	55.0	58.0	V	–
Filtering time for VCPH overvoltage detection		Tcphh	–	12	20	34	μs	–
VCC overvoltage detection threshold	VCC	Vthchh	–	5.5	5.75	6.0	V	–
Threshold for VCC overvoltage detection removal		Vthchl	–	5.4	5.65	5.9	V	–
Filtering time for VCC overvoltage detection	VCC	Tch	–	12	20	34	μs	–
VCC_OP undervoltage detection threshold	VCC_OP	Vthccopll	–	2.55	2.75	2.95	V	–
Threshold for VCC_OP undervoltage detection removal		Vthccoplh	–	2.65	2.85	3.05	V	–
Filtering time for VCC_OP overvoltage detection	VCC_OP	Tccopl	–	12	20	34	μs	–
VCC_OP overvoltage detection threshold	VCC_OP	Vthccophh	–	5.5	5.75	6.0	V	–
Threshold for VCC_OP overvoltage detection removal		Vthccophl	–	5.4	5.65	5.9	V	–
Filtering time for VCC_OP overvoltage detection	VCC_OP	Tccoph	–	12	20	34	μs	–
Overtemperature detection	–	Tsdh	–	(175)	(195)	(215)	°C	shown in (brackets) are design values
Temperature for overtemperature detection removal		Tsdl	–	(165)	(185)	(205)	°C	shown in (brackets) are design values
Filtering time for overtemperature detection		Ttsd	–	(12)	(20)	(34)	μs	shown in (brackets) are design values
VDS detection input current 1 for external MOSFET	HUS, HVS, HWS	I_vds1_Roff	VB=HS=H*S=13.5V, HUI(HVI,HWI)=Lo	-650	-400	-250	μA	–
		I_vds1_Ron	VB=HS=H*S=13.5V, HUI(HVI,HWI) In external MOSFET inspection mode.	4.5	6.8	8.5	mA	–
VDS detection input current 2 for external MOSFET	HUS, HVS, HWS	I_vds2_Roff	VB=HS=13.5V HUI(HVI,HWI)=Lo HUS(HVS,HWS)=0V	-650	-450	-250	μA	–
		I_vds2_Ron	VB=HS=13.5V HUI(HVI,HWI)=Lo HUS(HVS,HWS)=0V In external MOSFET inspection mode.	-8.5	-6.8	-4.5	mA	–

Parameter	Applied pin	Symbol	Test conditions	Min	Typ.	Max	Unit	Remark
Midpoint voltage divider ratio	HUS, HVS, HWS	—	In external MOSFET test mode	0.4	0.5	0.6	—	—
BIST time	—	Tbist	—	—	2.6	4	ms	—

Note Specifications shown in (brackets) are design values and not tested for delivery.
Note When Vcc drops below the Vcc low voltage detection voltage, it leads to a stand-by state.
Note Low voltage detection (VB, VCC, VCC_OP), high voltage detection (VCPH, VCC, VCC_OP) and overtemperature detection circuits are equipped with hysteresis.

Vb=4.5 to 28V, Vcc=3.0 to 5.5V, Tj=-40 to 175°C unless specified otherwise

Parameter	Applied pin	Symbol	Test conditions	Min	Typ.	Max	Unit	Remark
High side filtering time for external MOSFET VDS detection	—	Fil_vdsh0	HS=4.5 to 28V	3.9	6	8.1	µs	fil_vdsh="00"
		Fil_vdsh1		5.2	8	10.8	µs	fil_vdsh="01"
		Fil_vdsh2		6.5	10	13.5	µs	fil_vdsh="10"
		Fil_vdsh3		7.8	12	16.2	µs	fil_vdsh="11"
Low side filtering time for external MOSFET VDS detection	—	Fil_vdsl0	HS=4.5 to 28V	3.9	6	8.1	µs	fil_vdsl="00"
		Fil_vdsl1		5.2	8	10.8	µs	fil_vdsl="01"
		Fil_vdsl2		6.5	10	13.5	µs	fil_vdsl="10"
		Fil_vdsl3		7.8	12	16.2	µs	fil_vdsl="11"
Threshold voltage for external MOSFET VDS detection high side	HS, HUS, HVS, HWS	Vth_vdsh0	HS=4.5 to 28V	0.04	0.1	0.16	V	vth_vdsuh="0000", vth_vdsvh="0000", vth_vdswh="0000"
		Vth_vdsh1	HS=4.5 to 28V	0.14	0.2	0.26	V	vth_vdsuh="0001", vth_vdsvh="0001", vth_vdswh="0001"
		Vth_vdsh2	HS=4.5 to 28V	0.24	0.3	0.36	V	vth_vdsuh="0010", vth_vdsvh="0010", vth_vdswh="0010"
		Vth_vdsh3	HS=4.5 to 28V	0.34	0.4	0.46	V	vth_vdsuh="0011", vth_vdsvh="0011", vth_vdswh="0011"
		Vth_vdsh4	HS=4.5 to 28V	0.44	0.5	0.56	V	vth_vdsuh="0100", vth_vdsvh="0100", vth_vdswh="0100"
		Vth_vdsh5	HS=4.5 to 28V	0.54	0.6	0.66	V	vth_vdsuh="0101", vth_vdsvh="0101", vth_vdswh="0101"
		Vth_vdsh6	HS=4.5 to 28V	0.63	0.7	0.77	V	vth_vdsuh="0110", vth_vdsvh="0110", vth_vdswh="0110"
		Vth_vdsh7	HS=4.5 to 28V	0.72	0.8	0.88	V	vth_vdsuh="0111", vth_vdsvh="0111", vth_vdswh="0111"
		Vth_vdsh8	HS=4.5 to 28V	0.81	0.9	0.99	V	vth_vdsuh="1000", vth_vdsvh="1000", vth_vdswh="1000"
		Vth_vdsh9	HS=4.5 to 28V	0.9	1.0	1.1	V	vth_vdsuh="1001", vth_vdsvh="1001", vth_vdswh="1001"
		Vth_vdshA	HS=4.5 to 28V	0.99	1.1	1.21	V	vth_vdsuh="1010", vth_vdsvh="1010", vth_vdswh="1010"
		Vth_vdshB	HS=4.5 to 28V	1.08	1.2	1.32	V	vth_vdsuh="1011", vth_vdsvh="1011", vth_vdswh="1011"

Note VDS detection threshold voltage (high side) is provided by the voltage between the IC terminals: HS－HNote S.
Note VDS detection threshold voltage (low side) is provided by the voltage between the IC terminals: HNote S-LNote S.
Note * is U, V, W.

Vb=4.5 to 28V, Vcc=3.0 to 5.5V, Tj=-40 to 175°C unless specified otherwise

Parameter	Applied pin	Symbol	Test conditions	Min	Typ.	Max	Unit	Remark
External MOSFET VDS detection low side voltage threshold	HUS, HVS, HWS, LUS, LVS, LWS	Vth_vdsl0	HS=4.5 to 28V	0.04	0.1	0.16	V	vth_vdsul="0000", vth_vdsvl="0000", vth_vdswl="0000"
		Vth_vdsl1	HS=4.5 to 28V	0.14	0.2	0.26	V	vth_vdsul="0001", vth_vdsvl="0001", vth_vdswl="0001"
		Vth_vdsl2	HS=4.5 to 28V	0.24	0.3	0.36	V	vth_vdsul="0010", vth_vdsvl="0010", vth_vdswl="0010"
		Vth_vdsl3	HS=4.5 to 28V	0.34	0.4	0.46	V	vth_vdsul="0011", vth_vdsvl="0011", vth_vdswl="0011"
		Vth_vdsl4	HS=4.5 to 28V	0.44	0.5	0.56	V	vth_vdsul="0100", vth_vdsvl="0100", vth_vdswl="0100"
		Vth_vdsl5	HS=4.5 to 28V	0.54	0.6	0.66	V	vth_vdsul="0101", vth_vdsvl="0101", vth_vdswl="0101"
		Vth_vdsl6	HS=4.5 to 28V	0.63	0.7	0.77	V	vth_vdsul="0110", vth_vdsvl="0110", vth_vdswl="0110"
		Vth_vdsl7	HS=4.5 to 28V	0.72	0.8	0.88	V	vth_vdsul="0111", vth_vdsvl="0111", vth_vdswl="0111"
		Vth_vdsl8	HS=4.5 to 28V	0.81	0.9	0.99	V	vth_vdsul="1000", vth_vdsvl="1000", vth_vdswl="1000"
		Vth_vdsl9	HS=4.5 to 28V	0.9	1.0	1.1	V	vth_vdsul="1001", vth_vdsvl="1001", vth_vdswl="1001"
		Vth_vdslA	HS=4.5 to 28V	0.99	1.1	1.21	V	vth_vdsul="1010", vth_vdsvl="1010", vth_vdswl="1010"
		Vth_vdslB	HS=4.5 to 28V	1.08	1.2	1.32	V	vth_vdsul="1011", vth_vdsvl="1011", vth_vdswl="1011"
External MOSFET VGS overvoltage detection threshold	HUO, HVO, HWO, HUS, HVS, HWS, LUO, LVO, LWO, LUS, LVS, LWS	Vth_vgsh	–	15.5	17.5	19.5	V	–
Threshold for external MOSFET VGS overvoltage detection removal	HUO, HVO, HWO, HUS, HVS, HWS, LUO, LVO, LWO, LUS, LVS, LWS	Vth_vgsl	–	14.5	16.5	18.5	V	–
Filtering time for external MOSFET VGS overvoltage detection	–	Fil_vgs	–	5.2	8	10.8	µs	–

Parameter	Applied pin	Symbol	Test conditions	Min	Typ.	Max	Unit	Remark
NDIAG output voltage	NDIAG	Voh	Ioh = -5mA	0.9×Vcc	–	–	V	–
		Vol	Iol = 5mA	–	–	0.1×Vcc	V	–
L hold voltage	NDIAG	Vlk	Vcc=1.1V to Vthcll Iol = 100μA	0	–	0.3	V	Refer to Fig. 9-i
Frequency mutual comparison error detection coefficient	–	Kfreqdet	OSC_IF<12MHz OSC_SM<12MHz	–	2.1	–	A.U.	OSC_IF[MHz]/OSC_SM[MHz] or OSC_SM[MHz]/OSC_IF[MHz]

Note VDS detection threshold voltage (high side) is provided by the voltage between the IC terminals: HS-H*S.
Note VDS detection threshold voltage (low side) is provided by the voltage between the IC terminals: H*S-L*S.
Note * is U, V, W.
Note A.U. is an abbreviation for Arbitrary Unit.

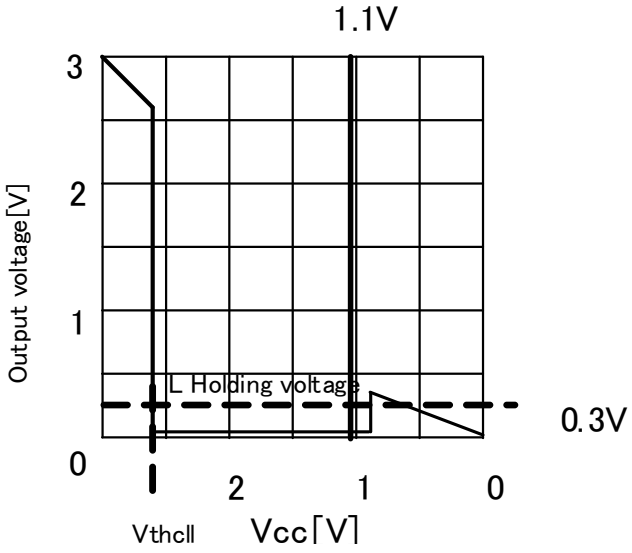


Fig. 9-i L Holding voltage

ALARM input circuit

Vb=4.5 to 28V, Vcc=3.0 to 5.5V, Tj=-40 to 175°C unless specified otherwise

Parameter	Applied pin	Symbol	Test conditions	Min	Typ.	Max	Unit	Remark
High level input current	ALARM	Iih	Vcc = 5.0V, Vin = 5.0V	50	100	200	μA	—
Low level input current		Iil	Vcc = 5.0V, Vin = 0V	-5	—	5	μA	—
High level input detection voltage	ALARM	Vih	—	0.75×Vcc	—	—	V	—
Low level input detection voltage		Vil	—	—	—	0.25×Vcc	V	—
Pulse width of input detection	ALARM	Twmin0	High, Low level detection	16.25	—	—	μs	fil_alm="00" $16x2^2x(1/4MHz)+(1/4MHz)$
		Twmin1		1.00025	—	—	ms	fil_alm="01" $1000x2^2x(1/4MHz)+(1/4MHz)$
		Twmin2		2.00025	—	—	ms	fil_alm="10" $2000x2^2x(1/4MHz)+(1/4MHz)$
		Twmin3		4.00025	—	—	ms	fil_alm="11" $4000x2^2x(1/4MHz)+(1/4MHz)$
Pulse width of input removal	ALARM	Twmax0	High, Low level detection	—	—	14.75	μs	fil_alm="00" $15x2^2x(1/4MHz)-(1/4MHz)$
		Twmax1		—	—	0.99875	ms	fil_alm="01" $999x2^2x(1/4MHz)-(1/4MHz)$
		Twmax2		—	—	1.99875	ms	fil_alm="10" $1999x2^2x(1/4MHz)-(1/4MHz)$
		Twmax3		—	—	3.99875	ms	fil_alm="11" $3999x2^2x(1/4MHz)-(1/4MHz)$

Note The input detection pulse width (Twmin) means the width of pulses appearing in the output after passing the digital filter, and input elimination pulse width (Twmax) means the width of pulses eliminated by the digital filter (**Fig.** 9-j).

Note Calculated, assuming ALARM digital filter setting: (1/4MHz)=250[ns].

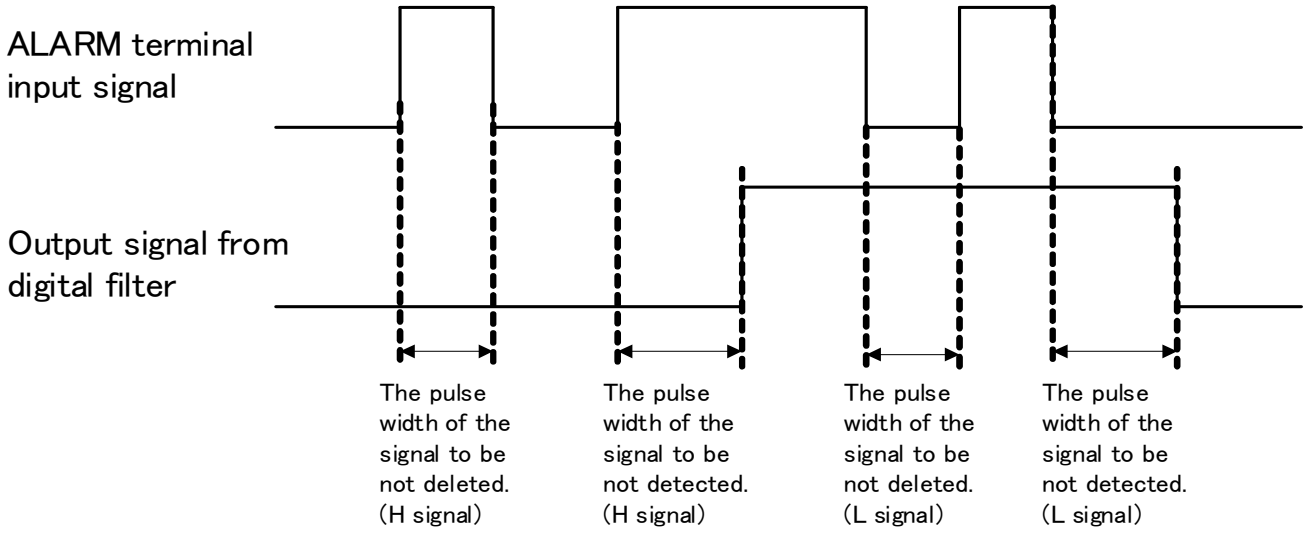


Fig. 9-j Input elimination pulse width (with a filter) and input detection pulse width (with a filter)

SPI communication circuit

SPI communication specifications (AC)

Vb=4.5 to 28V, Vcc=3.0 to 5.5V, Tj=-40 to 175°C unless specified otherwise

Parameter	Applied pin	Symbol	Test conditions	Min	Typ.	Max	Unit	Remark
Delay time from NSCS falling edge to SO	NSCS, SO	Tcsdo	Cload=100pF	–	–	100	ns	Time from NSCS falling edge to SO removed from HiZ state
Valid standby time	NSCS, SCLK	Tcsck	Fop = 2MHz	100	–	–	ns	Time from NSCS falling edge to SCLK rising edge
Invalid standby time	SCLK, NSCS	Tckcs	–	100	–	–	ns	Time from falling edge of the last pulse of SCLK to NSCS rising edge
SI setup time	SI, SCLK	Tdick	–	50	–	–	ns	SI data setup time
SI hold time	SI, SCLK	Tckdi	–	50	–	–	ns	SI data hold time
SO valid time	SCLK, SO	Tckdo	Cload=100pF	–	–	100	ns	Time from SCLK rising edge to SO data output
NSCS invalid time	NSCS	Tcsh	–	2	–	–	µs	Time from NSCS rising edge to NSCS falling edge
Delay time from SO to NSCS rising edge	NSCS, SO	Tdocs	Cload=100pF	–	–	100	ns	Time from NSCS rising edge to SO turning to HiZ state
Communication frequency	SCLK	Fop	–	–	–	2	MHz	–

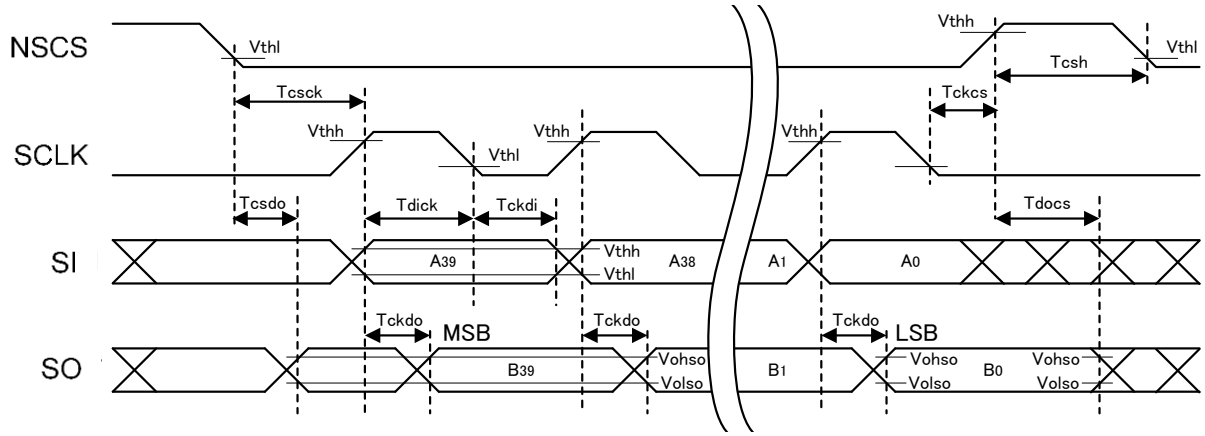


Figure 9-k SPI timing chart

SPI communication specifications (DC)

Vb=4.5 to 28V, Vcc=3.0 to 5.5V, Tj=-40 to 175°C unless specified otherwise

Parameter	Applied pin	Symbol	Test conditions	Min	Typ.	Max	Unit	Remark
High level input voltage	SI, SCLK, NSCS	Vthh	–	0.75× Vcc	–	–	V	–
Low level input voltage		Vthl		–	–	0.25× Vcc	V	–
High level input current	NSCS	Iih	Vcc = 5.0V, Vin = 5.0V	-5	–	5	μA	–
Low level input current		Iil	Vcc = 5.0V, Vin = 0V	-200	-100	-50	μA	–
High level input current	SI, SCLK	Iih	Vcc = 5.0V, Vin = 5.0V	50	100	200	μA	–
Low level input current		Iil	Vcc = 5.0V, Vin = 0V	-5	–	5	μA	–
High level output voltage	SO	Vohso	Iohso = -5mA	0.9× Vcc	–	–	V	–
Low level output voltage		Volso	Iolso = 5mA	–	–	0.1× Vcc	V	–

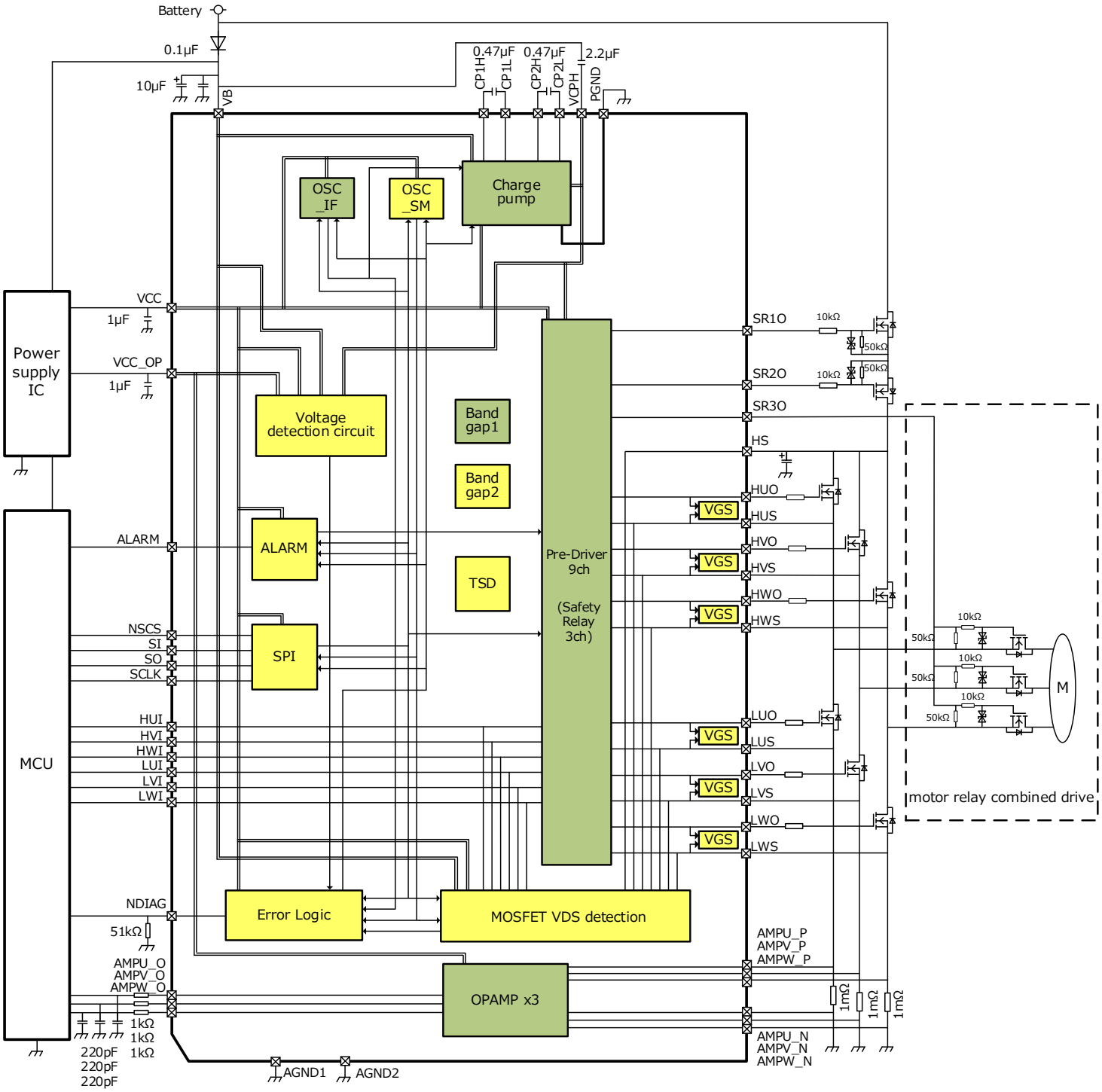
QA timer

Vb=4.5 to 28V, Vcc=3.0 to 5.5V, Tj=-40 to 175°C unless specified otherwise

Parameter	Applied pin	Symbol	Test conditions	Min	Typ.	Max	Unit	Remark
Timeout time	–	Tqa0	–	0.65	1	1.36	ms	–
		Tqa1		1.3	2	2.72	ms	–
		Tqa2		2.6	4	5.44	ms	–
		Tqa3		5.2	8	10.88	ms	–

10. Application circuit example

When driving motor relays collectively



≪Notes for users≫

Note The circuit constants are for the application circuit example, and not guaranteed.

Determine the external circuits after a sufficient evaluation and check on a unit board, assuming the conditions of the operating environment.

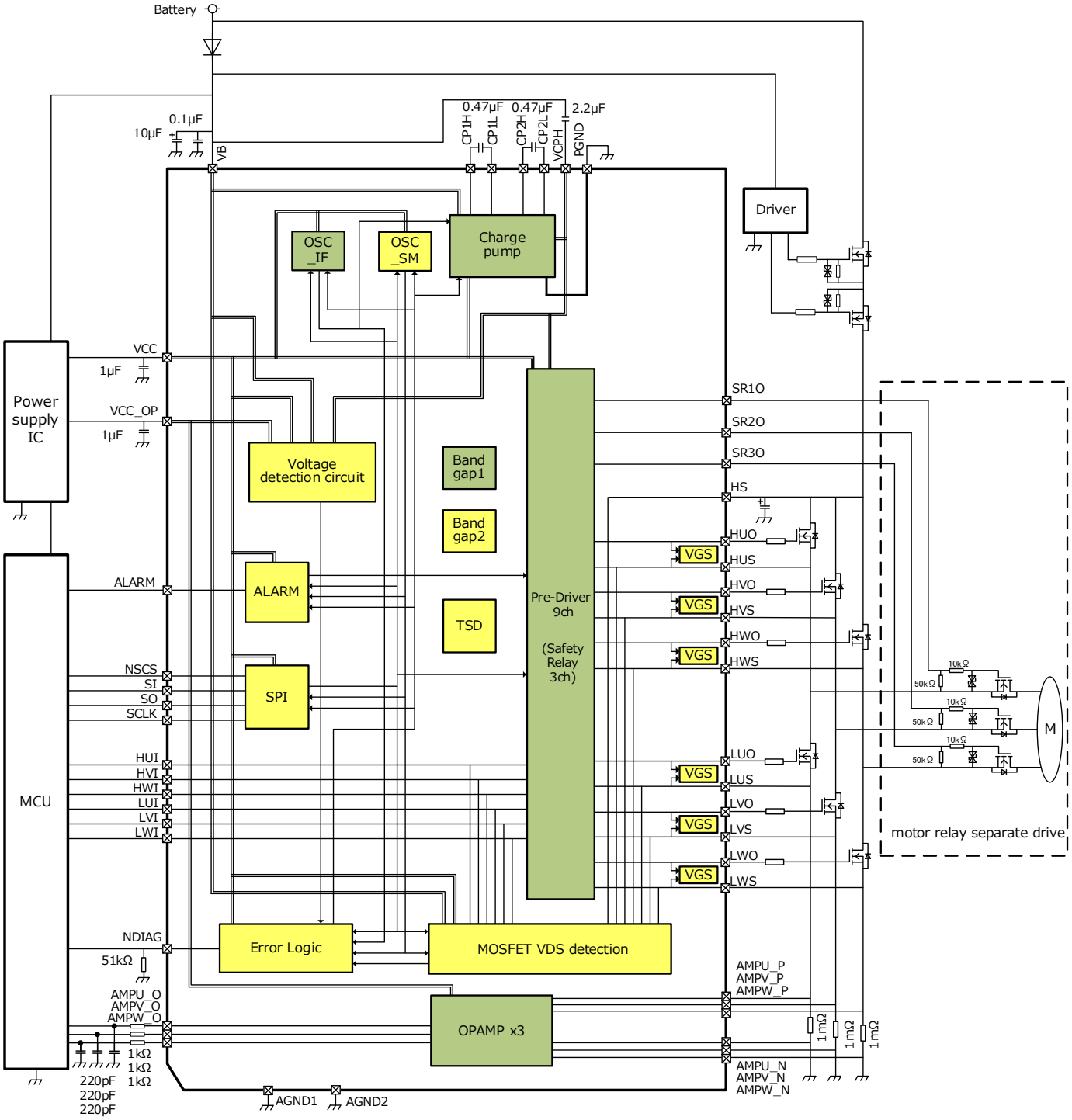
Note The smoothing capacitors externally added to the power supply terminals (VB, VCC, VCC_OP, VCPH) should be located as close to the roots of the IC as possible.

Note AGND1, 2 and PGND should be the solid GND (same potential ±0.3V) on the unit board.

Note When designing a unit, take into consideration the notes of the individual blocks as well.

Note Do not connect the IC incorrectly. It may destroy the IC and/or damage the devices.

When driving motor relays individually



≪Notes for users≫

Note The circuit constants are for the application circuit example, and not guaranteed.

Determine the external circuits after a sufficient evaluation and check on a unit board, assuming the conditions of the operating environment.

Note The smoothing capacitors externally added to the power supply terminals (VB, VCC, VCC_OP, VCPH) should be located as close to the roots of the IC as possible.

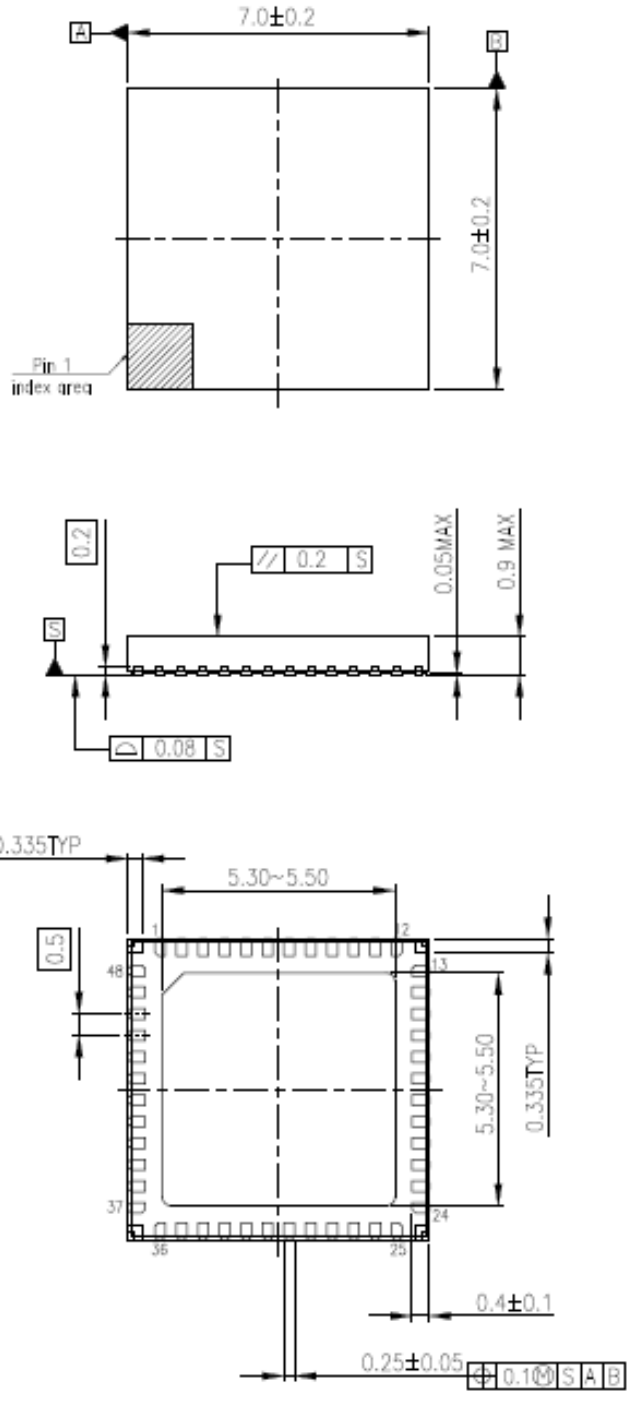
Note AGND1, 2 and PGND should be the solid GND (same potential ±0.3V) on the unit board.

Note When designing a unit, take into consideration the notes of the individual blocks as well.

Note Do not connect the IC incorrectly. It may destroy the IC and/or damage the devices.

11. Outline drawing

Package dimensions
P-VQFN48-0707-0.50-005 "Unit:mm"



Rev01

weight: 137.9mg (typ.)

12. Revision history

Specification Ver.	Specification changes	Dates of creation/changes
0.1	Newly created	2019/8/8
0.2	7.2 Pre-driver circuit Switches of mid-voltage resistors added to the figure. 7.5.8 DS Detection block diagram modified (Switches of mid-voltage resistors added). Detection state table modified. Signal names in the timing chart corrected. 8 Absolute maximum ratings Specifications on the input voltage of HUS, HVS, LWS added. Specifications on the output voltage of HUO, HVO, HWO added.	2019/8/8
0.3	7.5.11, 7.9.2, 7.9.3.18, 7.9.3.19, 7.9.3.20QA timer related items undated.	2019/8/19
0.4	7.3, 7.9.3.15 Electric current related items updated.	2019/8/28
0.5	Fig. 7.9-f Fig. 7.9-i "seq_coutner" value when QA timer start command is received is corrected. Various statuses and error accumulation counter The status bit err_qa is set to "H" for a sequence where answer data has turned out to be invalid, and it is maintained until it is cleared by the err_qa_cl bit. The status bit err_qato is set to "H" for a sequence where answer data has not been obtained within the pre-defined time, and it is maintained until it is cleared by the err_qato_cl bit. The status bit err_qac is set to "H" for a sequence where the error accumulation counter value has reached 4, and it is maintained until it is cleared by the err_qac_cl bit. Table 7.9-a, Fig. 7.9-i Corrected so that "seq_coutner" not cleared by "err_qac_cl." 7.9.3.18: Stated that register setting uses values at a time when a Start command is received.	2019/09/02
0.6	Table 7.7-a, Table 7.7-b Operation of charge pump and pre-drivers related to ABIST updated. Table 7.2-b Truth table regarding the prohibited input updated.。7.9.3.8 Description on registers regarding the prohibited input updated. 7.1,10 Description on the charge pump current limit added. 7.3.2, 7.9.3.15, 7.9.3.16 Description on the current detection amplifier offset calibration updated.	2019/09/03
0.7	Fig. 7.5.8-a Stated that VDS detection is disabled while pre-drivers are disabled. 7.2 Stated that series resistance value is not limited when the relay control output is used for power supply relay.	2019/09/05
0.8	7.8 Description the initial diagnosis circuit for external FETs and relays added. 7.9.3.23 - 7.9.3.26 Registers related to the initial diagnosis for external FETs and relays added. 0 Register map updated.	2019/9/20
0.9	7.9.3.23 Modified typeC description to Type D 7.9.3.23 Added fet_test_manual bit 0 FET manual inspection The explanation was corrected. 7.9.3.9, **エラー! 参照元が見つかりません。** Change the setting range of current value. 9 SPI communication circuit NSCS invalid time is corrected to 2us Fig. 7.8-c, Fig. 7.8-d, Fig. 7.8-e, Fig. 7.8-f Clarified existence of waiting time after turning on the mid-voltage generating resistor.	2019/12/4
0.10	Change motor relay application	2019/12/19
1.0	7.2. Pre-Driver Circuit Deleted the description of constant current drive Deleted the clump circuit of Fig.7.2a and b. Added the gate resistors. 7.9.3 Resister map Deleted HS_ISEL ith_puh/ith_pdh. Deleted LS_ISEL ith_pul/ith_pdl. Changed HS_ISEL to T_ILIM. Added a note about 32 μs and no current limit to the T_ILIM table. 9. Electrical characteristics Consumption current Set Standby current (Vb)/ Supply current (Vb) Supply current (Vcc)/ Supply current (Vccop). Charge pump circuit Changed Vcph1:Vb=4.5 to 7V Output load =TBD(8500pF) to Vb=4.5 to 5.5V Output load =28mA Changed Min:Vb+5.5 to Vb+5.3 Changed Vcph2:Vb=5.5 to 7V Output load =34mA(15000pF) to 28mA Changed Vcph3:Vb=7 to 28V Output load =34mA(15000pF) to 28mA	2020/09/18

Specification Ver.	Specification changes	Dates of creation/changes
	Changed Typ.:Vb+14 to Vb+11 Max.:Vb+16.5 to Vb+12 Deleted current Limitation. Added Operating frequency Pre-driver circuit Changed Output voltage11 Voh1 Test conditions：Voltage between H*O and H*S to Voltage between H*O and AGND Changed min.(Vcph-0.3)/max.Vcph Changed Output voltage 2 min.(6.7)/max.(12) Deleted High side pull-up current1 to 7. Deleted High side pull-down current1 to 7. Deleted Low side pull-up current1 to 7. Deleted Low side pull-down current1 to 7. Added Output resistance1and 2. Changed When turned on, input propagation delay time min:50 to 20n. Changed When turned off, input propagation delay time min:50 to 20n. Set VDS detection input current 1 for external MOSFET min.-850 typ.-650 max. -450μA Set VDS detection input current 2 for external MOSFET min.5 typ.6.8　max.7.6mA に設定 Set External MOSFET VGS overvoltage detection threshold min.15.5V typ.17.5V に設定 Set Threshold for external MOSFET VGS overvoltage detection removal　min. 14.5 typ.16.5 max.18.5V ・10. Application circuit example Added Gate resistors.	
1.1	7.2. Pre-driver circuit Added Clump circuits of Fig.7.2a and b 8. Absolute maximum ratings (Ta = 25℃) Changed Input voltage HS：-0.3 to Vb+0.3　to -18 to Vb+0.3. 9. Electrical characteristics Charge pump circuit Updated Operating frequency Added Pre-charging time and Enable time for pre-driver Updated Fig. Fig. 9 b Charge pump circuit timing chart ・Pre-river circuit Added Output voltage 1 Voh1(Vb=7.0 to 28V) and Voh1_2 Changed Output voltage 1 Voh1 Test conditions ：Voltage between H*O and AGND to Voltage between H*O and H*S Added Output voltage2 Test conditions L*S=0V ・Abnormality detection circuit Added BIST time.	2020/11/9
1.2	7.1 Charge pump Deleteded operating frequency in description 9. Electrical characteristics ・Pre-driver Updated Output resistance1 and 2(Tentative value).	2021/4/26
1.3	7.2 Pre-driver circuit→Corrected description of Current limiter 7.5.8. External MOSFET VDS detection Corrected a typographical error in the filter symbol in the timing chart Updated Fig. 7.5.8 d Timing chart for short-circuit detection (register vdsl_op = vdsh_op "0010") Updated Fig. 7.5.8 f Timing chart for short-circuit detection (register vdsl_op = vdsh_op “0100”) Updated Fig. 7.5.8 h Timing chart for short-circuit detection (register vdsl_op = vdsh_op “0110”) Updated Fig. 7.5.8 j Timing chart for short-circuit detection (register vdsl_op = vdsh_op “1000”) 7.5.9. External MOSFET VGS overvoltage detection Updated Fig. 7.5.9 c　Operational chart for VGS overe detection 7.7 ABIST/LBIST Fig. 7.7 b ABIST timing chart→Updated description of *2 If VB undervoltage detection and VCC_OP undervoltage detection are not released at the start of ABIST, the ABIST result will be abnormal. 7.9.3. Register map 7.9.3.2. OPSEL2 Write Address=04h / Read Address=84h→Added *1 7.9.3.11. FET_OPSEL Write Address=24h / Read Address=A4h→Added *1and*2 7.9.3.15. AMP_CTRL Write Address=40h / Read Address=C0h→gain_amp_u/v/w Updated “101”=x30→x27.5　Added “110”=x27.5 Updated“111”=x1 →x27.5 10. 8. Absolute maximum ratings (Ta = 25°C) Updated Allowable dissipation curve and Thermal resistance 9. Electrical characteristics Current detection circuit	2021/10/06

Specification Ver.	Specification changes	Dates of creation/changes
	GAIN Gain5: updated x30 to x27.5 Slew rate: updated with descriptions for the respective voltages(VCC_OP=5V and 3.3V) Input common mode voltage Updated min:-1.8V to -0.5V and max:2.0V to 0.5V	
1.4	7.3.3 Check output voltage with 1x gain → Delete content 7.9.3 Register map 7.9.3.9. delete note about 32μs in T_ILIM 7.9.3.28. add DUMMY 8. absolute maximum ratings (Ta = 25°C) VCPH -0.3to40(DC),40to60(≤1s) to -0.3to44.5(DC),44.5to60(≤1s) Input voltage: HUS, HVS, HWS -7to Vb+0.3 to -7to Vcph+0.3 LUS, LVS, LWS -7to Vb+0.3 to -7to Vcph+0.3 Input voltage: LUO, LVO, LWO -7to Vcpl+0.3 to -7to Vcph+0.3 Changed from Vout4≤20V to Vout4≤60V Input current : HUS, HVS, HWS Iin1: 1.2A AMPU_P, AMPV_P, AMPW_P, AMPU_N, AMPV_N, AMPW_N Iin2: -0.5 to 2mA Output current: HUO, HVO, HWO, LUO, LVO, LWO Iout1: -10 to 20mA Iout2: -1A AMPU_O, AMPV_O, AMPW_O Iout3: ±5mA NDIAG, SO: Iout4: ±10mA 9. Electrical Characteristics Consumption current Consumption current (Vb) Ib1/ Ib2/ Ib3 → Pre-Driver output load: Rload=0Ω, Cload=15000pF Add Safety Relay output load: Rload=1.5kΩ, Cload=15000pF Pre-Driver Circuit Output Resistor: SR1O/SR2O/SR3O Max changed from 600Ω to 650Ω Output resistor 1: HUO, HVO, HWO Rohh Max 12Ω Output resistor 2: LUO, LVO, LWO Rolh Max 12Ω Fig. 10 d Measurement circuit diagram (High side/Low side) Rload=10Ω Fig. 10 e Measurement circuit diagram Measurement circuit diagram (safety relay) deleted Fig. 10 f Output current switching time, input propagation delay time timing chart → updated to switch control Current detection circuit Settling time Time to converge to Rload=1kΩ, Cload=220pF output voltage ±2% was added to the measurement conditions. Added the input range where amplifier output can secure ±1% gain error when AMP*_P and AMP*_N are short-circuited as a measurement condition and changed max. to 2.0V. PSRR measurement condition was updated to "Input 1KHz to VCC_OP, but exclude the effect of VREF" and "min" was updated to "-". CMRR measurement condition: "Gain=15, Comvin=200mVp-p, 1KHz" was added. min was updated to "-". Abnormality Detection Circuit VDS detection input current of external MOSFET 1 I_vds1_Roff min:-650 typ:-400 max:-250 I_vds1_Ron min:4.5 typ:6.8 max:8.5 VDS detection input current 2 I_vds2_Roff min:-650 typ:-450 max:-250 I_vds2_Ron min:-8.5 typ:-6.8 max:-4.5 Dividing resistor current ratio for midpoint voltage generation → specified as Midpoint voltage divider ratio min. 0.4 typ. 0.5 max. 0.6 10. application circuit example Add external element constants	2022/08/18
1.5	Absolute maximum ratings (Ta = 25℃) Input Voltage HUS, HVS, HWS→Voltage between HUO-HUS, HVO-HVS, HWO-HWS ≤ 40V was added. Input Voltage LUS, LVS, LWS→Voltage between LUO-LUS, LVO-LVS, LWO- LWS ≤ 40V was added. Output Voltage HUO, HVO, HWO→Voltage between HUO-HUS, HVO-HVS, HWO-HWS ≤ 40V was added. Output Voltage LUO, LVO, LWO→Voltage between LUO-LUS, LVO-LVS, LWO- LWS ≤ 40V was added. Input Voltage AMPU_P, AMPV_P, AMPW_P,AMPU_N, AMPV_N, AMPW_N Updated -7 to	2022-10-31

Specification Ver.	Specification changes	Dates of creation/changes
	Vb+0.3(DC) to -7 to 28(DC),28 to 40(≤1s) Deleted Vin5≤28V Electrical characteristics Table Items Updated ratings to Operating voltage range Add " It is not recommended to use this product at Vb<3.6V all the time." outside the operating voltage range column. Charge pump circuit Fig. 9 b Charge pump circuit timing chart NDIAG→Hi timing is changed to D_PRED_EN→Hi timing. Pre-driver circuit Output voltage1 Test conditions of Voh1_2 “HUO(HVO, HWO) and HUS(HVS, HWS), HUS(HVS, HWS)=0V” was added. Output voltage2 Test conditions of Vol2 “LUS(LVS,LWS)=0V” was added. Output resistance1 Test conditions of Rohh Updated Iload = -50 mA Output resistance 2 Test conditions of Rolh Updated Iload = -50 mA Output resistance SR1O/SR2O/SR3O Updated Min. 400Ω to 350Ω and Max 650Ω to 750Ω Deleted reference comments for Fig. 10-e in the measurement circuit Current detection circuit GAIN：Updated Gain5 typ.27.5 to 27.4(Register map AMP_CTRL updated as well) Updated Fig9-i Slew rate timing Output Abnormality detection circuit Filtering time for VCC_OP overvoltage detection Updated min. 13 to 12 VDS detection input current 1 for external MOSFET Added "HUI(HVI,HWI)=Lo" to the measurement conditions VDS detection input current 2 for external MOSFET Added "HUI(HVI,HWI)=Lo" to the measurement conditions Threshold voltage for external MOSFET VDS detection high side→Added Applied pin External MOSFET VDS detection low side voltage threshold→Added Applied pin External MOSFET VGS overvoltage detection threshold→Added Applied pin Threshold for external MOSFET VGS overvoltage detection removal→Added Applied pin Frequency mutual comparison error detection coefficient Added in Remark “OSC_IF[MHz]/OSC_SM[MHz] or OSC_SM[MHz]/OSC_IF[MHz]” Added in outside the table ”A.U. is an abbreviation for Arbitrary Unit.”	
1.6	FEATURES AND BENEFITS AEC-Q100: (TBC) to Qualified ISO 26262 2nd edition Remove (TBC) Register Map DUMMY Corrected address 7ch to 7Ch.	2022-11-22
1.7	Pre-driver circuit Inhibited input changed from “Fig 7.2-b shows” to “Table 7.2-b shows” 8. Absolute maximum ratings Deleted Ta=25℃ Outline drawing Updated weight: 137.9mg (typ.)	2023-01-20
1.8	General Circuit diagram symbols in figures are compatible with new JIS standards. 3. FEATURES AND BENEFITS Functional safety Added Developed according to ISO 26262 2nd Ed. ASIL-D Capable. 7.9.3. Register map 7.9.3.14. AMP_CTRL Write Address=40h / Read Address=C0h Deleted “110”=x27.4 8. Absolute maximum ratings HS Updated -18 to 28(DC),2 to 40(≤1s) Updated Output Current Iout1：±20mA and Iout2：±1A 9.Electrical characteristics Charge pump circuit Output voltage Added maximum voltage 3xVB-1.5 in VB=4.5 to 5.5V and 5.5 to 7.0V Current detection circuit Coorrected Applied pin in Output voltage 1 The following items were corrected that (brackets) are design values	2023-07-24

Specification Ver.	Specification changes	Dates of creation/changes
	Input offset voltage temperature characteristic 1 Input offset voltage temperature characteristic 2 Reference voltage Reference temperature characteristic ALARM input circuit Corrected Fig.9-j Output signal from digital Filter (to be not detected → to be not)	
1.9	7.5.8. External MOSFET VDS detection Fig. 7.5.8 e Timing chart for short-circuit detection (register vdsl_op = vdsh_op “0011”) Fig. 7.5.8 g Timing chart for short-circuit detection (register vdsl_op = vdsh_op “0101”) Fig. 7.5.8 i Timing chart for short-circuit detection (register vdsl_op = vdsh_op “0111”) Fig. 7.5.8 k Timing chart for short-circuit detection (register vdsl_op = vdsh_op “1001”) →Corrected description of fvds*ho and fvds*lo. 9. 9. Electrical characteristics Fig. 9 c Charge pump voltage dependence Corrected description of range of 4.5V to 7.0V.	2024-03-08
2.0	8. Absolute maximum ratings Updated Output voltage Vout2(HUO, HVO, HWO) -7 to Vcph＋0.6(DC).	2024-04-16
2.1	Table 7.5 a Monitoring functions Reg. setting Correct the typo from uvvccop_op to uvccop_op and the typo from ovvccop_op to ovccop_op Fig. 7.8 a Block diagram of the diagnosis circuit for external FETs and relays Correct the typo in the connection destination of the pull-down resistors for HVO and HWO. 10. Electrical characteristics Added HS=4.5 to 28V to Test conditions of High side filtering time for external MOSFET VDS detection, Low side filtering time for external MOSFET VDS detection, Threshold voltage for external MOSFET VDS detection high side and External MOSFET VDS detection low side voltage threshold.	2024-06-25
2.2	Corrected chapter and figure numbers	2024-10-31

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