

**TOSHIBA**

**8 Bit Microcontroller  
TLCS-870/C Series**

**TMP86PM72FG**

Not Recommended  
for New Design

**TOSHIBA CORPORATION**

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For a discussion of how the reliability of microcontrollers can be predicted, please refer to Section 1.3 of the chapter entitled Quality and Reliability Assurance/Handling Precautions. 030619 \_ S

## Revision History

Date	Revision	
2003/6/23	1	First Release
2008/8/29	2	Contents Revised

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## Caution in Setting the UART Noise Rejection Time

When UART is used, settings of RXDNC are limited depending on the transfer clock specified by BRG. The combination "O" is available but please do not select the combination "-".

The transfer clock generated by timer/counter interrupt is calculated by the following equation :

$$\text{Transfer clock [Hz]} = \text{Timer/counter source clock [Hz]} \div \text{TTREG set value}$$

BRG setting	Transfer clock [Hz]	RXDNC setting			
		00 (No noise rejection)	01 (Reject pulses shorter than 31/fc[s] as noise)	10 (Reject pulses shorter than 63/fc[s] as noise)	11 (Reject pulses shorter than 127/fc[s] as noise)
000	fc/13	O	O	O	-
110 (When the transfer clock generated by timer/counter interrupt is the same as the right side column)	fc/8	O	-	-	-
	fc/16	O	O	-	-
	fc/32	O	O	O	-
The setting except the above		O	O	O	O

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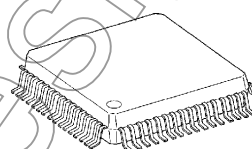
## CMOS 8-Bit Microcontroller

## TMP86PM72FG

The TMP86PM72 is a OTP type MCU which includes 32-Kbyte one-time PROM. It is a pin compatible with a mask ROM product of the TMP86CH72/CM72. Writing the program to built-in PROM, the TMP86PM72 operates as the same way as the TMP86CH72/CM72. Using the Adapter socket, you can write and verify the data for the TMP86PM72 with a general-purpose PROM programmer same as TC571000D/AD.

Product No.	OTP	RAM	Package	Adapter Socket
TMP86PM72FG	32 K × 8 bits	1 K × 8 bits	P-QFP64-1414-0.80C	BM11707

P-QFP64-1414-0.80C



TMP86PM72FG

030619EBP1

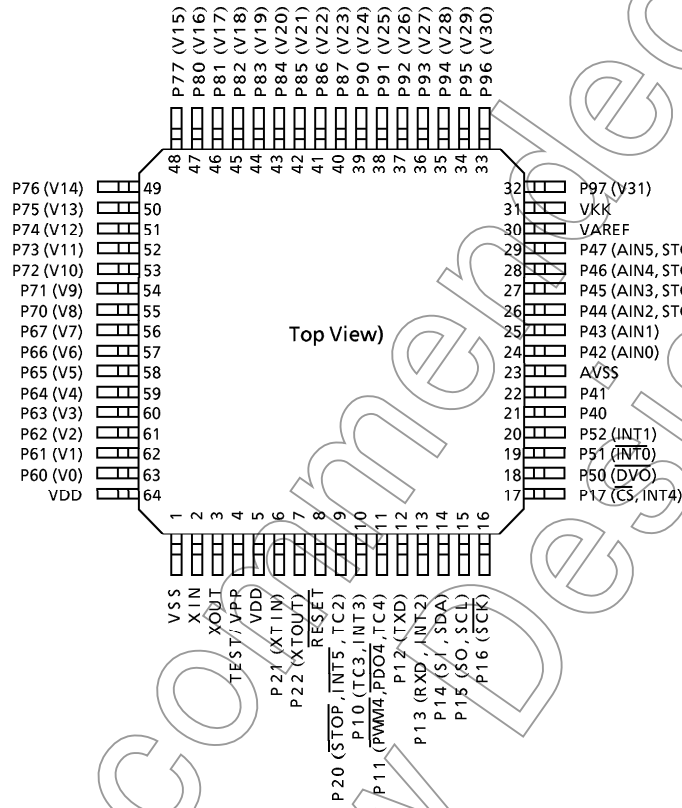
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Purchase of TOSHIBA I<sup>2</sup>C components conveys a license under the Philips I<sup>2</sup>C Patent Rights to use these components in an I<sup>2</sup>C system, provided that the system conforms to the I<sup>2</sup>C Standard Specification as defined by Philips.

Pin Assignments (Top View)

P-QFP64-1414-0.80C



Note: All VDD terminals are connected externally.

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## Pin Function

The TMP86PM72 has MCU mode and PROM mode.

## (1) MCU mode

In the MCU mode, the TMP86PM72 is a pin compatible with the TMP86CH72/CM72 (Make sure to fix the TEST pin to low level).

## (2) PROM mode

Pin name (PROM mode)	Input/Output	Functions	Pin Name (MCU mode)
A16 to A12	Input	Input of Memory address for program	PD4 to PD0
A11 to A8			P53 to P50
A7 to A0			P47 to P40
D7 to D0	I/O	Input/Output of Memory data for program	P17 to P10
CE	Input	Chip enable	P95
OE		Output enable	P94
PGM		Program control	P93
VPP	Power supply	+ 12.75 V/5 V (Power supply of program)	TEST
VDD		+ 6.25 V/5 V	VDD
GND		0 V	VSS
P51, P21	I/O	PROM mode setting pin. Fix to high.	
P50, P20, P22, AVSS, VAREF		PROM mode setting pin. Fix to low.	
RESET			
XIN	Input	Self oscillation with resonator (10 MHz)	
XOUT	Output		

## Operation

This section describes the functions and basic operational blocks of TMP86PM72.

The TMP86PM72 has PROM in place of the mask ROM which is included in the TMP86CH72/CM72.

In addition, TMP86PM72 operates as the single clock mode when releasing reset.

When using the dual clock mode, oscillate a low-frequency clock by [SET (SYSCR2). XTEN] command at the beginning of program.

### 1. Operating Mode

The TMP86PM72 has MCU mode and PROM mode.

#### 1.1 MCU Mode

The MCU mode is set by fixing the TEST/VPP pin to the low level. (TEST/VPP pin cannot be used open because it has no built-in pull-down resistor).

##### 1.1.1 Program Memory

The TMP86PM72 has a 32 Kbyte built-in one time PROM (addresses 8000<sub>H</sub> to FFFF<sub>H</sub> in the MCU mode, addresses 0000<sub>H</sub> to 7FFF<sub>H</sub> in the PROM mode).

When using TMP86PM72 for evaluation of mask ROM products, the program is written in the program storing area shown in Figure 1-1.

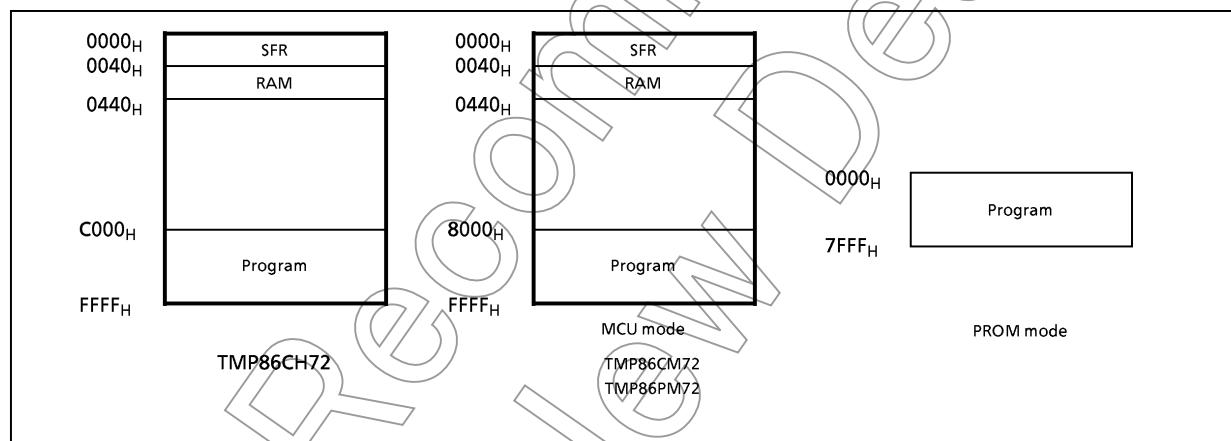


Figure 1-1. Program Memory Area

**Note:** The area that is not in use should be set data to FFH, or a general-purpose PROM programmer should be set only in the program memory area to access.



**1.1.2 Data Memory**

TMP86PM72 has a built-in 1 Kbyte Data memory (static RAM).

**1.1.3 Input/Output Circuitry****(1) Control pins**

The control pins of the TMP86PM72 are the same as those of the TMP86CH72/CM72 except that the TEST pin does not have a built-in pull-down resistor.

**(2) I/O ports**

The I/O circuitries of TMP86PM72 I/O ports are the same as the those of TMP86CH72/CM72.

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1.2 PROM Mode

The PROM mode is set by setting the RESET pin, the ports P51, P50, P22 to P20 and TEST as shown in Figure 1-2. The programming and verification for the internal PROM is achieved by using a general-purpose PROM programmer with the adapter socket.

*Note: The high-speed program mode can be used. The setting is different according to the type of PROM programmer to use, refer to each description of PROM programmer.  
The TMP86PM72 does not support the electric signature mode, apply the ROM type of PROM programmer to TC571000D/AD.*

Always set the switch of adapter socket to the N side when using TOSHIBA's adapter socket.

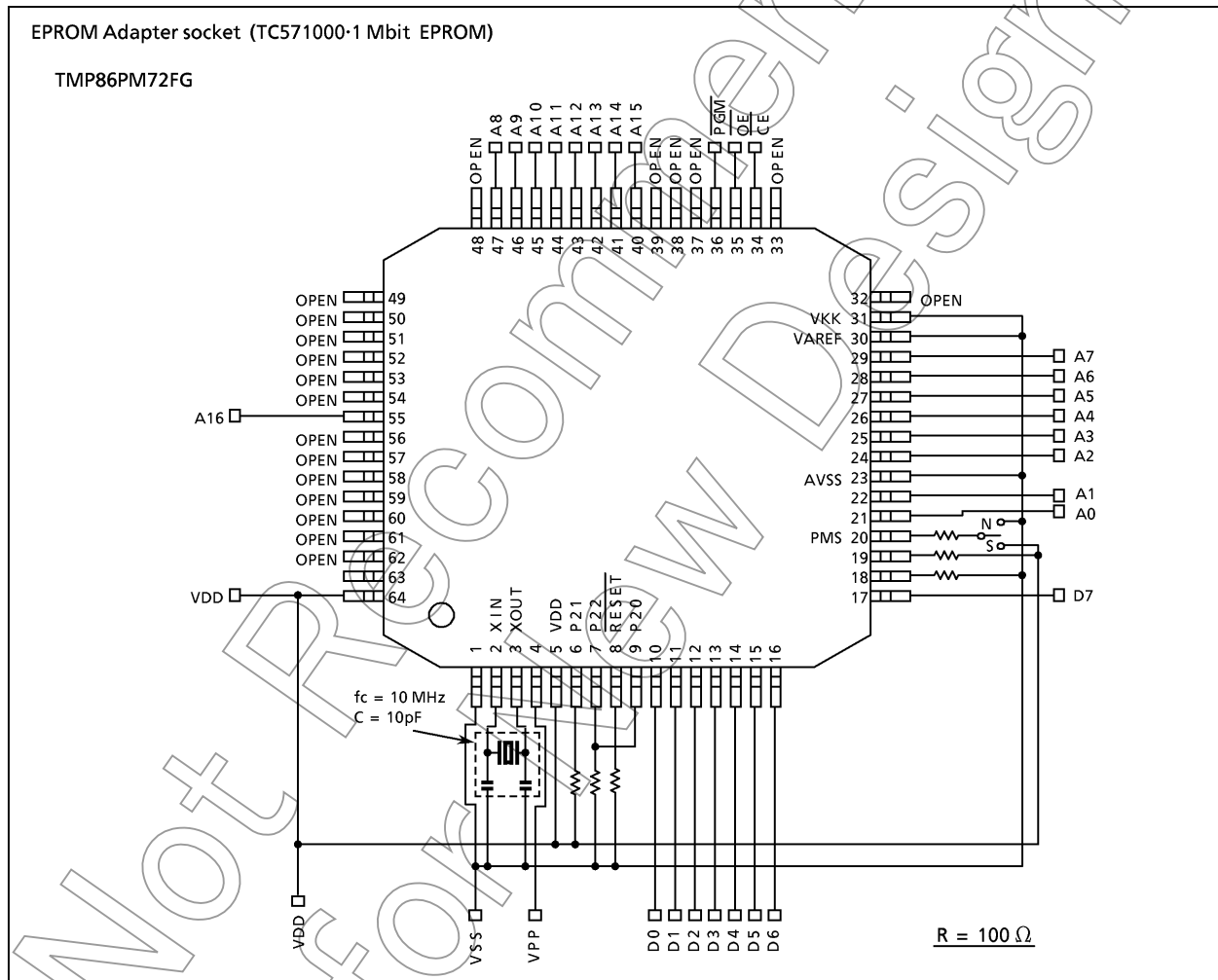


Figure 1-2. PROM Mode Setting

### 1.2.1 Programming Flowchart (High-speed program writing)

The high-speed programming mode is set by applying 12.75 V (programming voltage) to the  $V_{PP}$  pin when the  $V_{DD}$  is 6.25 V. After the address and data are fixed, the data in the address is written by applying 0.1ms of low level program pulse to  $\overline{PGM}$  pin. Then verify if the data is written.

If the programmed data is incorrect, another 0.1 ms pulse is applied to  $\overline{PGM}$  pin.

This programming procedure is repeated until correct data is read from the address (maximum of 25 times).

Subsequently, all data are programmed in all addresses.

When all data were written, verify all address under the condition of  $V_{DD} = V_{PP} = 5$  V.

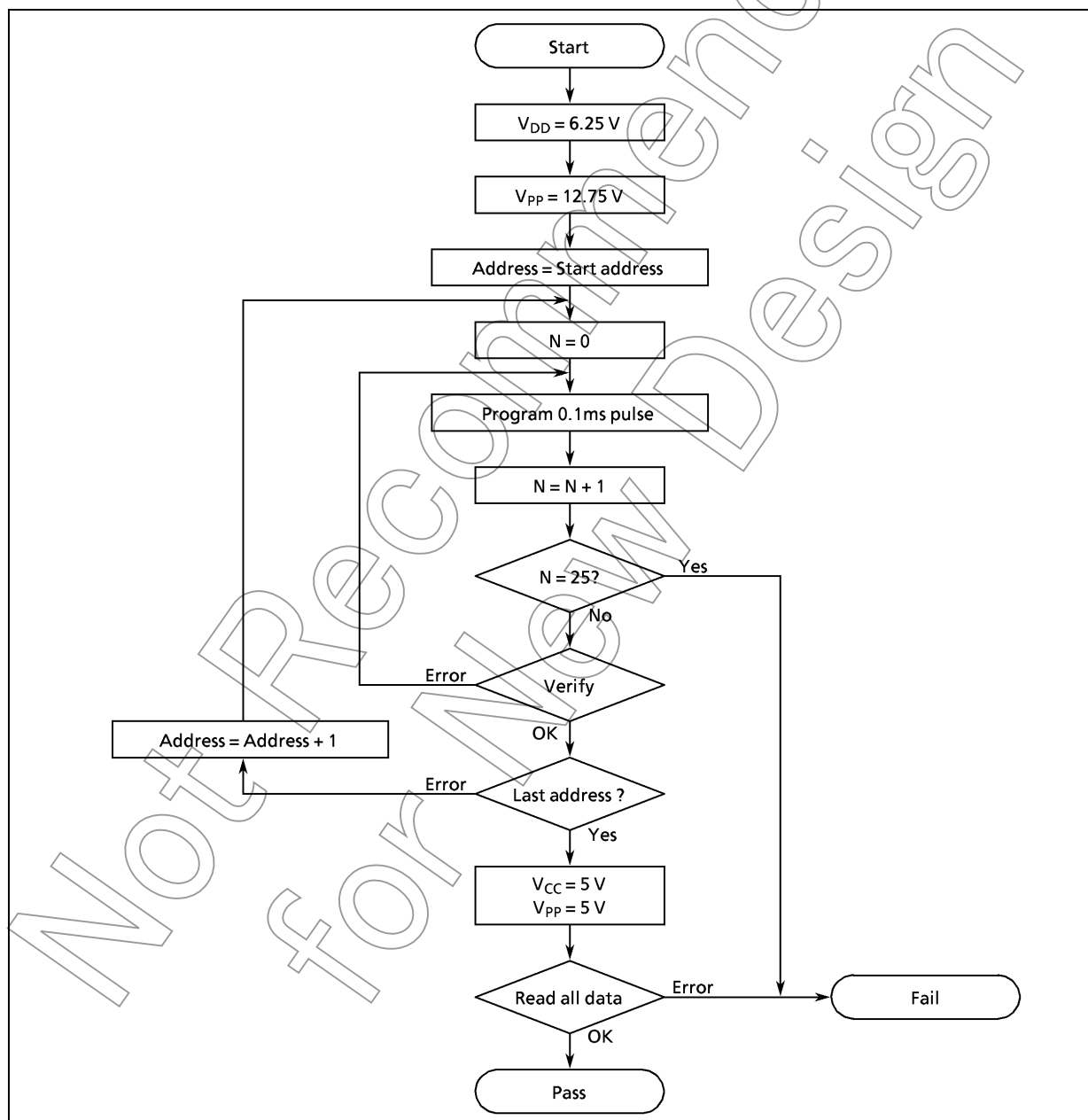


Figure 1-3. Programming Flowchart

### 1.2.2 Program Writing using a General-purpose PROM Programmer

- (1) Recommended OTP adapter  
BM11707: for TMP86PM72FG
- (2) Setting of OTP adapter  
Set the switch (SW1) to N side.
- (3) Setting of PROM programmer
  - i) Set PROM type to TC571000D/AD.  
VPP: 12.75 V (high-speed program writing)

- ii) Data transmission (Note 1)

The PROM of TMP86PM72 is located on different addresses; it depends on operating modes: MCU mode and PROM mode. When you write the data of ROM for mask ROM products, the data should be transferred from the address for MCU mode to that for PROM mode before writing operation is executed. For the applicable program areas of MCU mode and PROM mode are different, refer to Figure 1-1 Program Memory Area.

Example: In the block transfer (copy) mode, executed as below.

ROM capacity of 32 KB: Transferred address 08000<sub>H</sub> to 0FFFF<sub>H</sub> to addresses 00000<sub>H</sub> to 07FFF<sub>H</sub>

- iii) Setting of the program address (Note 1)

Start address: 00000<sub>H</sub>  
End address: 07FFF<sub>H</sub>

- (4) Writing program

Write and verify according to the above mentioned "Setting of PROM programmer."

*Note 1: For the setting method, refer to each description of PROM programmer.*

*Make sure to set the data of address area that is not in used to FF<sub>H</sub>.*

*Note 2: When setting MCU to the adapter or when setting the adapter to the PROM programmer, set the first pin of the adapter and that of PROM programmer socket matched. If the first pin is conversely set, MCU or adapter or programmer would be damaged.*

*Note 3: The TMP86PM72 does not support the electric signature mode.*

*If PROM programmer uses the signature, the device would be damaged because of applying voltage of 12 ± 0.5 V to pin 9 (A9) of the address.*

*Do not use the signature.*

## Electrical Characteristics

Absolute Maximum Ratings	( $V_{SS} = 0\text{ V}$ )
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Parameter	Symbol	Pins	Rating	Unit	
Supply voltage	$V_{DD}$		-0.3 to 6.5	V	
Program voltage	$V_{PP}$	TEST/ $V_{PP}$	-0.3 to 13.0		
Input voltage	$V_{IN}$		-0.3 to $V_{DD} + 0.3$		
Output voltage	$V_{OUT1}$		-0.3 to $V_{DD} + 0.3$		
	$V_{OUT2}$	Source open drain ports	$V_{DD} - 41$ to $V_{DD} + 0.3$		
Output current (per 1 pin)	IOL	$I_{OUT1}$	P0, P1, P2, P4 (P42~P47), P5 ports	5	mA
		$I_{OUT2}$	P4 (P40, P41) port	40	
	IOH	$I_{OUT3}$	P0, P1, P4, P5 ports	-3	
		$I_{OUT4}$	P6, P7 ports	-30	
		$I_{OUT5}$	P8, P9 ports	-20	
Output current (total)	$\Sigma I_{OUT1}$	P0, P1, P2, P4, P5 ports	120		
	$\Sigma I_{OUT2}$	P6, P7, P8, P9 ports	-120		
Power dissipation [ $T_{opr} = 25^\circ\text{C}$ ]	PD		1200	mW	
Soldering temperature (time)	$T_{sld}$		260 (10 $\mu$ )	$^\circ\text{C}$	
Storage temperature	$T_{stg}$		-55 to 125		
Operating temperature	$T_{opr}$		-30 to 70		

**Note:** The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

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Recommended Operating Condition ( $V_{SS} = 0\text{ V}$ ,  $T_{opr} = -30\text{ to }70^{\circ}\text{C}$ )

Parameter	Symbol	Pins	Condition	Min	Max	Unit
Supply voltage	$V_{DD}$		$f_c = 16\text{ MHz}$	NORMAL1/2 modes	4.5	5.5
				IDLE0, 1/2 modes		
			$f_c = 8\text{ MHz}$	NORMAL1/2 modes	2.7	
				IDLE0, 1/2 modes		
			$f_s = 32.768\text{ kHz}$	SLOW mode		
SLEEP mode						
		STOP mode				
Output voltage	$V_{OUT3}$	Source open drain ports		$V_{DD} - 38$	$V_{DD}$	V
Input high level	$V_{IH1}$	Except hysteresis input		$V_{DD} \times 0.70$	$V_{DD}$	
	$V_{IH2}$	Hysteresis input		$V_{DD} \times 0.75$		
	$V_{IH3}$	TTL input	$V_{DD} \leq 4.5\text{ V}$	$V_{DD} \times 0.90$		
Input low level	$V_{IL1}$	Except hysteresis input		0	$V_{DD} \times 0.30$	
	$V_{IL2}$	Hysteresis input			$V_{DD} \times 0.25$	
	$V_{IL3}$	TTL input	$V_{DD} \leq 4.5\text{ V}$	$V_{DD} \times 0.10$	$V_{DD}$	
Clock frequency	$f_c$	XIN, XOUT	$V_{DD} = 2.7\text{ to }5.5\text{ V}$	1.0	8.0	MHz
			$V_{DD} = 4.5\text{ to }5.5\text{ V}$		16.0	
	$f_s$	XTIN, XTOUT		30.0	34.0	kHz

*Note: The recommended operating conditions for a device are operating conditions under which it can be guaranteed that the device will operate as specified. If the device is used under operating conditions other than the recommended operating conditions (Supply voltage, operating temperature range, specified AC/DC values etc.), malfunction may occur. Thus, when designing products which include this device, ensure that the recommended operating conditions for the device are always adhered to.*

## DC Characteristics (1)

 $(V_{DD} = 5\text{ V})$ 

[Condition]  $V_{DD} = 5.0\text{ V} \pm 10\%$ ,  $V_{SS} = A_{VSS} = 0\text{ V}$ ,  $T_{opr} = -30 \sim 70^\circ\text{C}$   
 (Typ.:  $V_{DD} = 5.0\text{ V}$ ,  $T_{opr} = 25^\circ\text{C}$ ,  $V_{in} = 5.0\text{ V}/0\text{ V}$ )

Parameter	Symbol	Pins	Condition	Min	Typ.	Max	Unit		
Hysteresis voltage	$V_{HS}$	Hysteresis input		-	0.9	-	V		
Input current	$I_{IN1}$	TEST	$V_{DD} = 5.5\text{ V}$ , $V_{IN} = 5.5\text{ V}/0\text{ V}$	-	-	$\pm 2$	$\mu\text{A}$		
	$I_{IN2}$	Sink open drain, Tri-st							
	$I_{IN3}$	RESET, STOP							
Input resistance	$R_{IN}$	RESET pull-up		100	220	450	k $\Omega$		
Pull-down resistance (Note 4)	$R_K$	Source open drain, Tri-st	$V_{DD} = 5.5\text{ V}$ , $V_{KK} = -30\text{ V}$	50	80	120			
Output leakage current	$I_{LO1}$	Sink open drain, Tri-st	$V_{DD} = 5.5\text{ V}$ , $V_{OUT} = 5.5\text{ V}/0\text{ V}$	-	-	$\pm 2$	$\mu\text{A}$		
	$I_{LO2}$	Source open drain	$V_{DD} = 5.5\text{ V}$ , $V_{KK} = -32\text{ V}$	-	-	$\pm 2$			
Output high voltage	$V_{OH}$	Tri-st port	$V_{DD} = 4.5\text{ V}$ , $I_{OH} = -0.7\text{ mA}$	4.1	-	-	V		
Output low voltage	$V_{OL1}$	Except XOUT and (P40, P41) Port	$V_{DD} = 4.5\text{ V}$ , $I_{OL} = 1.6\text{ mA}$	-	-	0.4			
Output high current	$I_{OH1}$	P6, P7	$V_{DD} = 4.5\text{ V}$ , $V_{OH} = 2.4\text{ V}$	-18	-28	-	mA		
	$I_{OH2}$	P8, P9, PD	$V_{DD} = 4.5\text{ V}$ , $V_{OH} = 2.4\text{ V}$	-9	-14	-			
Output low current	$I_{OL}$	High current port (P40, P41)	$V_{DD} = 4.5\text{ V}$ , $V_{OL} = 1.0\text{ V}$	-	20	-	mA		
Supply current in NORMAL1/2 modes	$I_{DD}$		$f_c = 16.0\text{ MHz}$ $f_s = 32.768\text{ kHz}$	AD converter disable (IREF off)	-	12		18	
			$f_c = 8.0\text{ MHz}$ $f_s = 32.768\text{ kHz}$		-	6		9	
Supply current in IDLE0/1/2 modes			$f_c = 16.0\text{ MHz}$ $f_s = 32.768\text{ kHz}$		-	6		9	
			$f_c = 8.0\text{ MHz}$ $f_s = 32.768\text{ kHz}$		-	3		4.5	
Supply current in NORMAL1/2 modes			$f_c = 16.0\text{ MHz}$ $f_s = 32.768\text{ kHz}$		AD converter enable	-		13	19
			$f_c = 8.0\text{ MHz}$ $f_s = 32.768\text{ kHz}$			-		7	10
Supply current in STOP mode			$T_{opr} = \text{to } 50^\circ\text{C}$		AD converter disable	-		0.5	5
			$T_{opr} = \text{to } 70^\circ\text{C}$			-	10		

Note 1: Typical values show those at  $T_{opr} = 25^\circ\text{C}$ ,  $V_{DD} = 5\text{ V}$ .

Note 2: Input current ( $I_{IN1}$ ,  $I_{IN3}$ ): The current through pull-up or pull-down resistor is not included.

Note 3:  $I_{DD}$  does not include  $I_{REF}$  current.

Note 4:  $T_{opr} = -10^\circ\text{C}$  to  $70^\circ\text{C}$

## DC Characteristics (2)

 $(V_{DD} = 3\text{ V})$ 

[Condition]  $V_{DD} = 3.0\text{ V} \pm 10\%$ ,  $V_{SS} = A_{VSS} = 0\text{ V}$ ,  $T_{opr} = -30\text{ to }70^\circ\text{C}$   
 (Typ.:  $V_{DD} = 3.0\text{ V}$ ,  $T_{opr} = 25^\circ\text{C}$ ,  $V_{in} = 3.0\text{ V}/0\text{ V}$ )

Parameter	Symbol	Pins	Condition	Min	Typ.	Max	Unit		
Hysteresis voltage	$V_{HS}$	Hysteresis input		-	0.4	-	V		
Input current	$I_{IN1}$	TEST	$V_{DD} = 3.3\text{ V}$ , $V_{IN} = 3.3\text{ V}/0\text{ V}$	-	-	$\pm 2$	$\mu\text{A}$		
	$I_{IN2}$	Sink open drain, Tri-st							
	$I_{IN3}$	RESET, STOP							
Input resistance	$R_{IN}$	RESET pull-up		100	220	450	$\text{k}\Omega$		
Pull-down resistance	$R_K$	Source open drain, tri-st	$V_{DD} = 3.3\text{ V}$ , $V_{KK} = -30\text{ V}$	45	75	115			
Output leakage current	$I_{LO1}$	Sink open drain, tri-st	$V_{DD} = 3.3\text{ V}$ , $V_{OUT} = 3.3\text{ V}/0\text{ V}$	-	-	$\pm 2$	$\mu\text{A}$		
	$I_{LO2}$	Source open drain	$V_{DD} = 3.3\text{ V}$ , $V_{KK} = -32\text{ V}$	-	-	$\pm 2$			
Output high voltage	$V_{OH}$	Tri-st port	$V_{DD} = 2.7\text{ V}$ , $I_{OH} = -0.6\text{ mA}$	2.3	-	-	V		
Output low voltage	$V_{OL1}$	Except XOUT and (P40, P41) Port	$V_{DD} = 2.7\text{ V}$ , $I_{OL} = 0.9\text{ mA}$	-	-	0.4			
Output high current	$I_{OH1}$	P6, P7	$V_{DD} = 2.7\text{ V}$ , $V_{OH} = 1.5\text{ V}$	-5.5	-8	-	mA		
	$I_{OH2}$	P8, P9, PD	$V_{DD} = 2.7\text{ V}$ , $V_{OH} = 1.5\text{ V}$	-3	-4.5	-			
Output low current	$I_{OL}$	High current port (P40, P41) port	$V_{DD} = 2.7\text{ V}$ , $V_{OL} = 1.0\text{ V}$	-	6	-			
Supply current in NORMAL1/2 modes	$I_{DD}$		$f_c = 8.0\text{ MHz}$ $f_s = 32.768\text{ kHz}$	AD converter disable (IREF off)	-	3	4.5	mA	
Supply current in IDLE0/1/2 modes			$f_c = 8.0\text{ MHz}$ $f_s = 32.768\text{ kHz}$	AD converter enable	-	2	2.5		
Supply current in NORMAL1/2 modes			$f_c = 8.0\text{ MHz}$ $f_s = 32.768\text{ kHz}$	AD converter enable	-	3.5	5		
Supply current in SLOW1 mode			$f_s = 32.768\text{ kHz}$	AD converter disable	-	30	60	$\mu\text{A}$	
Supply current in SLEEP0, 1 mode					-	15	30		
Supply current in STOP mode					$T_{opr} = \text{to } 50^\circ\text{C}$	-	0.5		5
					$T_{opr} = \text{to } 70^\circ\text{C}$	-	0.5		10

Note 1: Typical values show those at  $T_{opr} = 25^\circ\text{C}$ ,  $V_{DD} = 3\text{ V}$ .

Note 2: Input current ( $I_{IN1}$ ,  $I_{IN3}$ ): The current through pull-up or pull-down resistor is not included.

Note 3:  $I_{DD}$  does not include IREF current.

Note 4: The supply currents of SLOW2 and SLEEP2 modes are equivalent IDLE0, 1, 2.



## AD Conversion Characteristics

(V<sub>SS</sub> = 0.0 V, 4.5 V ≤ V<sub>DD</sub> ≤ 5.5 V, Topr = -30 to 70°C)

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Analog reference voltage	V <sub>AREF</sub>		V <sub>DD</sub> - 1.5	-	V <sub>DD</sub>	V
Analog reference GND	A <sub>VSS</sub>			V <sub>SS</sub>		
Analog reference voltage range (Note 4)	ΔV <sub>AREF</sub>		3.0	-	-	
Analog input voltage	V <sub>AIN</sub>		V <sub>SS</sub>	-	V <sub>AREF</sub>	
Power supply current of analog reference voltage	I <sub>REF</sub>	V <sub>DD</sub> = V <sub>AREF</sub> = 5.5 V V <sub>SS</sub> = A <sub>VSS</sub> = 0.0 V	-	0.6	1.0	mA
Non linearity error			-	-	± 1	LSB
Zero point error		V <sub>DD</sub> = V <sub>AREF</sub> = 4.5 to 5.0 V, V <sub>SS</sub> = A <sub>VSS</sub> = 0.0 V	-	-	± 1	
Full scale error			-	-	± 1	
Total error			-	-	± 2	

(V<sub>SS</sub> = 0.0 V, 2.7 V ≤ V<sub>DD</sub> < 4.5 V, Topr = -30 to 70°C)

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Analog reference voltage	V <sub>AREF</sub>		V <sub>DD</sub> - 1.5	-	V <sub>DD</sub>	V
Analog reference GND	A <sub>VSS</sub>			V <sub>SS</sub>		
Analog reference voltage range (Note 4)	ΔV <sub>AREF</sub>		2.5	-	-	
Analog input voltage	V <sub>AIN</sub>		V <sub>SS</sub>	-	V <sub>AREF</sub>	
Power supply current of analog reference voltage	I <sub>REF</sub>	V <sub>DD</sub> = V <sub>AREF</sub> = 4.5 V V <sub>SS</sub> = A <sub>VSS</sub> = 0.0 V	-	0.5	0.8	mA
Non linearity error			-	-	± 1	LSB
Zero point error		V <sub>DD</sub> = A <sub>VDD</sub> = 2.7 V to 4.5 V, V <sub>SS</sub> = A <sub>VSS</sub> = 0.0 V	-	-	± 1	
Full scale error			-	-	± 1	
Total error			-	-	± 2	

Note 1: The total error includes all errors except a quantization error, and is defined as a maximum deviation from the ideal conversion line.

Note 2: Conversion time is different in recommended value by power supply voltage. About conversion time, please refer to "2.11.2 Register Configuration".

Note 3: Please use input voltage to AIN input Pin in limit of V<sub>AREF</sub> - V<sub>SS</sub>. When voltage of range outside is input, conversion value becomes unsettled and gives affect to other channel conversion value.

Note 4: Analog Reference Voltage Range: ΔV<sub>AREF</sub> = V<sub>AREF</sub> - V<sub>SS</sub>

## AC Characteristics

 $(V_{SS} = 0\text{ V}, V_{DD} = 4.5\text{ to }5.5\text{ V}, T_{opr} = -30\text{ to }70^{\circ}\text{C})$ 

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Machine cycle time	tcy	NORMAL1/2 modes	0.25	-	4	$\mu\text{s}$
		IDLE1/2 modes				
		SLOW1/2 modes	117.6	-	133.3	
		SLEEP1/2 modes				
High level clock pulse width	twcH	For external clock operation (XIN input)	-	31.25	-	ns
Low level clock pulse width	twcL	fc = 16 MHz	-	15.26	-	$\mu\text{s}$
High level clock pulse width	twcH	For external clock operation (XTIN input)	-	15.26	-	$\mu\text{s}$
Low level clock pulse width	twcL	fc = 32.768 kHz	-	15.26	-	$\mu\text{s}$

 $(V_{SS} = 0\text{ V}, V_{DD} = 2.7\text{ to }4.5\text{ V}, T_{opr} = -30\text{ to }70^{\circ}\text{C})$ 

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Machine cycle time	tcy	NORMAL1/2 modes	0.5	-	8	$\mu\text{s}$
		IDLE1/2 modes				
		SLOW1/2 modes	117.6	-	133.3	
		SLEEP1/2 modes				
High level clock pulse width	twcH	For external clock operation (XIN input)	-	62.5	-	ns
Low level clock pulse width	twcL	fc = 8 MHz	-	15.26	-	$\mu\text{s}$
High level clock pulse width	twcH	For external clock operation (XTIN input)	-	15.26	-	$\mu\text{s}$
Low level clock pulse width	twcL	fc = 32.768 kHz	-	15.26	-	$\mu\text{s}$

Not Recommended for New

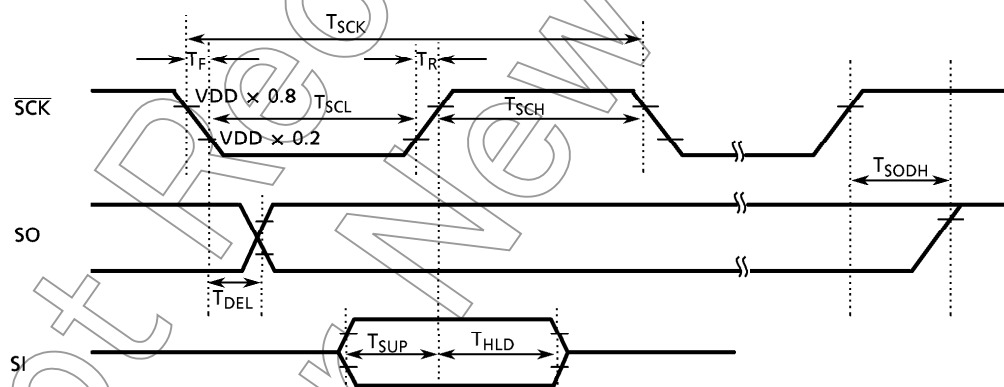
HSIO AC Characteristics

( $V_{SS} = 0\text{ V}$ ,  $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ ,  $T_{opr} = -30\text{ to }70^\circ\text{C}$ )

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit	
$\overline{\text{SCK}}$ output period (Internal clock)	$T_{\text{SCK1}}$	$8\text{ MHz} < f_c \leq 16\text{ MHz}$ $V_{DD} = 4.5\text{ V to }5.5\text{ V}$	$16/f_c$	-	-	s	
$\overline{\text{SCK}}$ output low width (Internal clock)	$T_{\text{SCL1}}$		$8/f_c - 100\text{ ns}$	-	-		
$\overline{\text{SCK}}$ output high width (Internal clock)	$T_{\text{SCH1}}$		$8/f_c - 100\text{ ns}$	-	-		
$\overline{\text{SCK}}$ output period (Internal clock)	$T_{\text{SCK2}}$	$4\text{ MHz} < f_c \leq 8\text{ MHz}$ $V_{DD} = 2.7\text{ V to }5.5\text{ V}$	$8/f_c$	-	-		
$\overline{\text{SCK}}$ output low width (Internal clock)	$T_{\text{SCL2}}$		$4/f_c - 100\text{ ns}$	-	-		
$\overline{\text{SCK}}$ output high width (Internal clock)	$T_{\text{SCH2}}$		$4/f_c - 100\text{ ns}$	-	-		
$\overline{\text{SCK}}$ output period (Internal clock)	$T_{\text{SCK3}}$	$f_c \leq 4\text{ MHz}$ $V_{DD} = 2.7\text{ V to }5.5\text{ V}$	$4/f_c$	-	-		
$\overline{\text{SCK}}$ output low width (Internal clock)	$T_{\text{SCL3}}$		$2/f_c - 100\text{ ns}$	-	-		
$\overline{\text{SCK}}$ output high width (Internal clock)	$T_{\text{SCH3}}$		$2/f_c - 100\text{ ns}$	-	-		
$\overline{\text{SCK}}$ input period (External clock)	$T_{\text{SCK4}}$	$f_c \leq 8\text{ MHz}$ ( $V_{DD} = 2.7\text{ V to }5.5\text{ V}$ )	800	-	-	ns	
$\overline{\text{SCK}}$ input low width (External clock)	$T_{\text{SCL4}}$		$f_c \leq 16\text{ MHz}$	300 (Note 1)	-		-
$\overline{\text{SCK}}$ input low width (External clock)	$T_{\text{SCH4}}$		( $V_{DD} = 4.4\text{ V to }5.5\text{ V}$ )	300 (Note 1)	-		-
SI input setup time	$T_{\text{SUP}}$	$V_{DD} = 3.0\text{ V}$ , $CL = 50\text{ pF}$ (Note 2)	150	-	-	ns	
SI input hold time	$T_{\text{HLD}}$		150	-	-		
SO output delay time	$T_{\text{DEL}}$		-	-	200		
Rising time	$T_{\text{R}}$		-	-	100		
Falling time	$T_{\text{F}}$		-	-	100		
SO last bit hold time	$T_{\text{SODH}}$		$16.5/f_c$	-	$32.5/f_c$		

Note 1:  $T_{\text{SCKL}}, T_{\text{SCKH}} \geq 2.5/f_c$  (High-frequency clock mode),  $T_{\text{SCKL}}, T_{\text{SCKH}} \geq 2.5/f_c$  (Low-frequency clock mode)

Note 2:  $CL$ , external capacitance

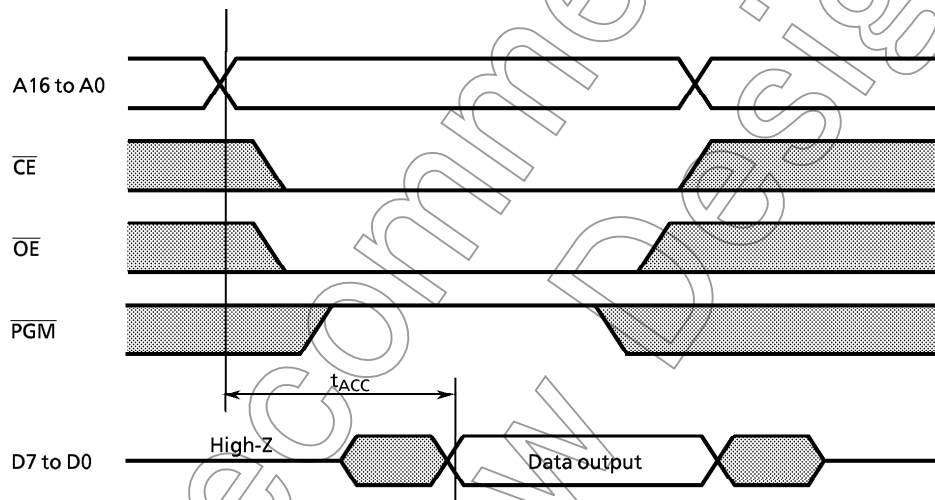


DC Characteristics, AC Characteristics (PROM mode) ( $V_{SS} = 0\text{ V}$ ,  $T_{opr} = 25 \pm 5^\circ\text{C}$ )

(1) Read operation in PROM mode

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
High level input voltage (TTL)	$V_{IH3}$		2.2	-	$V_{DD}$	V
Low level input voltage (TTL)	$V_{IL3}$		0	-	0.8	
Power supply	$V_{DD}$		4.75	5.0	5.25	
Power supply of program	$V_{PP}$					
Address access time	$t_{ACC}$	$V_{DD} = 5.0 \pm 0.25\text{ V}$	-	$1.5t_{cyc} + 300$	-	ns

Note:  $t_{cyc} = 400\text{ ns}$  at 10 MHz

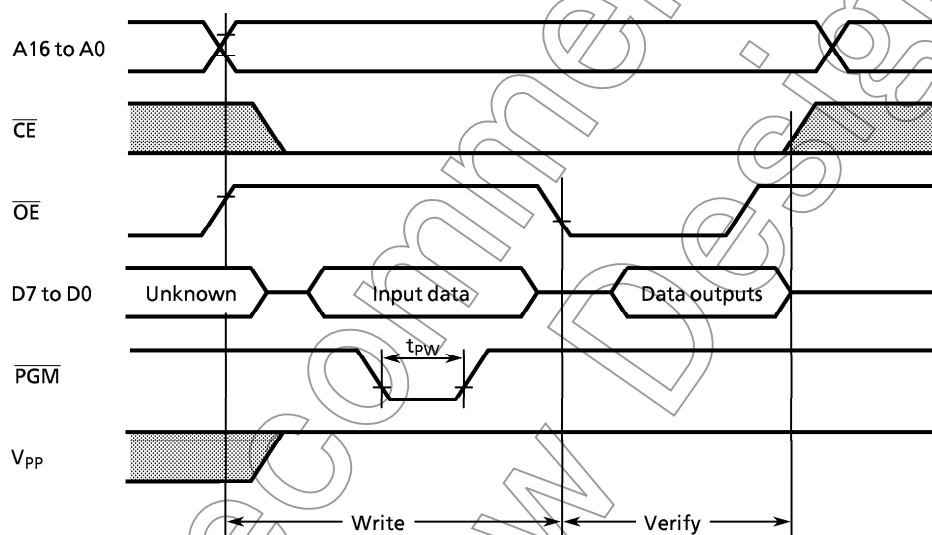


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(2) Program operation (High-speed) ( $T_{opr} = 25 \pm 5^\circ\text{C}$ )

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
High level input voltage (TTL)	$V_{IH3}$		2.2	—	$V_{DD}$	V
Low level input voltage (TTL)	$V_{IL3}$		0	—	0.8	
Power supply	$V_{DD}$		6.0	6.25	6.5	
Power supply of program	$V_{PP}$		12.5	12.75	13.0	
Pulse width of initializing program	$t_{PW}$	$V_{DD} = 6.0\text{ V}$	0.095	0.1	0.105	ms

## High-speed program writing



**Note 1:** The power supply of  $V_{PP}$  (12.75 V) must be set power-on at the same time or the later time for a power supply of  $V_{DD}$  and must be clear power-on at the same time or early time for a power supply of  $V_{DD}$ .

**Note 2:** The pulling up/down device on the condition of  $V_{PP} = 12.75\text{ V} \pm 0.25\text{ V}$  causes a damage for the device. Do not pull up/down at programming.

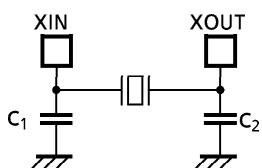
**Note 3:** Use the recommended adapter and mode.

Using other than the above condition may cause the trouble of the writing.

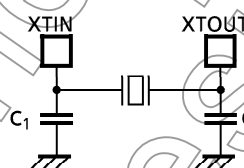
## Recommended Oscillating Conditions

(V<sub>SS</sub> = 0 V, T<sub>opr</sub> = -30 to 70°C)

Parameter	Oscillator	Oscillation Frequency	VDD	Recommended Oscillator	Recommended Constant	
					C <sub>1</sub>	C <sub>2</sub>
High-frequency oscillation	Ceramic resonator	16 MHz	4.5 V to 5.5 V	MURATA CSA16.00MXZ040	10 pF	10 pF
		8 MHz	2.7 V to 5.5 V	MURATA CSA8.00MTZ CST8.00MTW	30 pF 30 pF (built-in)	30 pF 30 pF (built-in)
		4.19 MHz	2.7 V to 5.5 V	MURATA CSA4.19MG CST4.19MGW	30 pF 30 pF (built-in)	30 pF 30 pF (built-in)
Low-frequency oscillation	Crystal oscillator	32.768 kHz	2.7 V to 5.5 V	SII VT-200	6 pF	6 pF



(1) High-frequency Oscillation



(2) Low-frequency Oscillation

**Note 1:** An electrical shield by metal shield plate on the surface of IC package is recommended in order to protect the device from the high electric field stress applied from CRT (Cathodic Ray Tube) for continuous reliable operation.

**Note2:** When using the device (oscillator) in places exposed to high electric fields such as cathode-ray tubes, we recommend electrically shielding the package in order to maintain normal operating condition.

**Note 3:** The product numbers and specifications of the resonators by Murata Manufacturing Co., Ltd. are subject to change.

For up-to-date information, please refer to the following URL:

<http://www.murata.co.jp/search/index.html>