32-bit RISC microcontroller

TXZ+ Family
TMPM4G Group (1)

Reference Manual
Clock Control and Operation Mode
(CG-M4G(1)-C)

Revision 1.4

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Arm® Cortex®-M4 Processor Technical Reference Manual
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Conventions

- Numeric formats follow the rules as shown below:
  Hexadecimal: 0xABC
  Decimal: 123 or 0d123 - Only when it needs to be explicitly shown that they are decimal numbers.
  Binary: 0b111 - It is possible to omit the "0b" when the number of bits can be distinctly understood from a sentence.
- "_N" is added to the end of signal names to indicate low active signals.
- It is called "assert" that a signal moves to its active level, "deassert" to its inactive level.
- When two or more signal names are referred, they are described like as [m:n].
  Example: S[3:0] shows four signal names S3, S2, S1 and S0 together.
- The characters surrounded by ***[ ]*** defines the register.
  Example: ***[ABCD]***
- "N" substitutes suffix number of two or more same kind of registers, fields, and bit names.
  Example: ***[XYZ1]***, ***[XYZ2]***, ***[XYZ3]*** → ***[XYZn]***
- "x" substitutes suffix number or character of units and channels in the register list.
- In case of unit, "x" means A, B, and C, ...
  Example: ***[ADACR0]***, ***[ADBCR0]***, ***[ADCCR0]*** → ***[ADxCR0]***
- In case of channel, "x" means 0, 1, and 2, ...
  Example: ***[T32A0RUNA]***, ***[T32A1RUNA]***, ***[T32A2RUNA]*** → ***[T32AxRUNA]***
- The bit range of a register is written like as [m: n].
  Example: Bit[3: 0] expresses the range of bit 3 to 0.
- The configuration value of a register is expressed by either the hexadecimal number or the binary number.
  Example: ***[ABCD]***<EFG> = 0x01 (hexadecimal), ***[XYZn]***<VW> = 1 (binary)
- Word and byte represent the following bit length.
  Byte: 8 bits
  Half word: 16 bits
  Word: 32 bits
  Double word: 64 bits
- Properties of each bit in a register are expressed as follows:
  R: Read only
  W: Write only
  R/W: Read and write are possible.
- Unless otherwise specified, register access supports only word access.
- The register defined as "Reserved" must not be rewritten. Moreover, do not use the read value.
- The value read from the bit having default value of "-" is unknown.
- When a register containing both of writable bits and read-only bits is written, read-only bits should be written with their default value, In the cases that default is "-", follow the definition of each register.
- Reserved bits of the write-only register should be written with their default value. In the cases that default is "-", follow the definition of each register.
- Do not use read-modified-write processing to the register of a definition which is different by writing and read out.

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Terms and Abbreviations

Some of abbreviations used in this document are as follows:

ADC	Analog to Digital Converter
APB	Advanced Peripheral Bus
A-PMD	Advanced Programmable Motor Control Circuit
CEC	Consumer Electronics Control
CG	Clock Control and Operation Mode
DAC	Digital to Analog Converter
DNF	Digital Noise Filter
ELOSC	External Low-speed Oscillator
EHOSC	External High-speed Oscillator
EI2C	I^2C Interface Version A
FIR	Finite Impulse Response
fsys	Frequency of SYSTEM Clock
HDMAC	High-speed Direct Memory Access Controller
I2C	Inter-integrated Circuit
I2CS	Wake-up Function by Address Matching
I2S	Inter-IC Sound
IHOSC	Internal High-speed Oscillator
IA (INTIF)	Interrupt Control Register A
IB (INTIF)	Interrupt Control Register B
I-Bus	Icode Memory Interface
ISD	Interval Sensing Detector
IMN	Interrupt Monitor
INT	Interrupt
IO	IO Bus (32-bit Peripheral Bus)
LTTMR	Long Term Timer
LVD	Voltage Detection Circuit
MDMAC	Multi-function Direct Memory Access Controller
NBDIF	Non-break Debug Interface
NMI	Non-Maskable Interrupt
OFD	Oscillation Frequency Detector
POR	Power-on Reset Circuit
PORF	Power-on Reset Circuit for FLASH and Debug
RLM	Low-speed Oscillation/Power Supply Control/reset
RMC	Remote Control Signal Preprocessor
RTC	Real Time Clock
S-Bus	System Interface
SCOUT	Source Clock Output
SIWDT	Clock Selective Watchdog Timer
SMIF	Serial Memory Interface
TPIU	Trace Port Interface Unit
TRGSEL	Trigger Selection Circuit
TRM	Trimming Circuit
TSPI	Serial Peripheral Interface
TSSI	Serial Synchronous Interface
T32A	32-Bit Timer Event Counter
UART	Universal Asynchronous Receiver Transmitter

1. Clock Control and Operation Mode

1.1. Outlines

The clock/mode control block can select a clock gear and prescaler clock and set the warming-up of oscillator and so on.

Furthermore, it has NORMAL mode and a low-power consumption mode to reduce power consumption using mode transition.

Functions related to a clock are as follows.

- System clock control
- Prescaler clock control

1.2. Clock Control

1.2.1. Clock Type

This section shows a list of clocks:

EHCLKIN:	High-speed clock input from the external
fosc:	Clock generated in the internal oscillation circuit or input from the X1 and X2 pins
f_{PLL}:	Clock multiplied with PLL0
fc:	Clock selected by ***[CGPLL0SEL]***<PLL0SEL> (High-speed clock)
ELCLKIN:	Low-speed clock input from the external
fs:	Clock output from an external low-speed oscillator
fsysh:	High-speed system clock selected by ***[CGSYSCR]***<GEAR[2:0]>
fsysm:	Middle-speed system clock selected by ***[CGSYSCR]***<GEAR[2:0]><MCKSEL[1:0]>
ΦT0h:	High-speed clock selected by ***[CGSYSCR]***<PRCK[3:0]> (High-speed prescaler clock)
ΦT0m:	Middle-speed clock selected by ***[CGSYSCR]***<PRCK[3:0]><MCKSEL[1:0]> (Middle-speed prescaler clock)
f_{IHOSC1}:	Clock generated with the internal high-speed oscillator 1
f_{IHOSC2}:	Clock generated with the internal high-speed oscillator 2
ADCLK:	Conversion clock for AD converter
TRCLKIN:	Clock for tracing facilities of a debugging circuit (TRACE or SWV)

Note: The high-speed system clock and the middle-speed system clock are collectively called System clock (fsys). And the high-speed prescaler clock and the middle-speed prescaler clock are collectively called prescaler clock (ΦT0).

1.2.2. Initial Value by Reset Operation

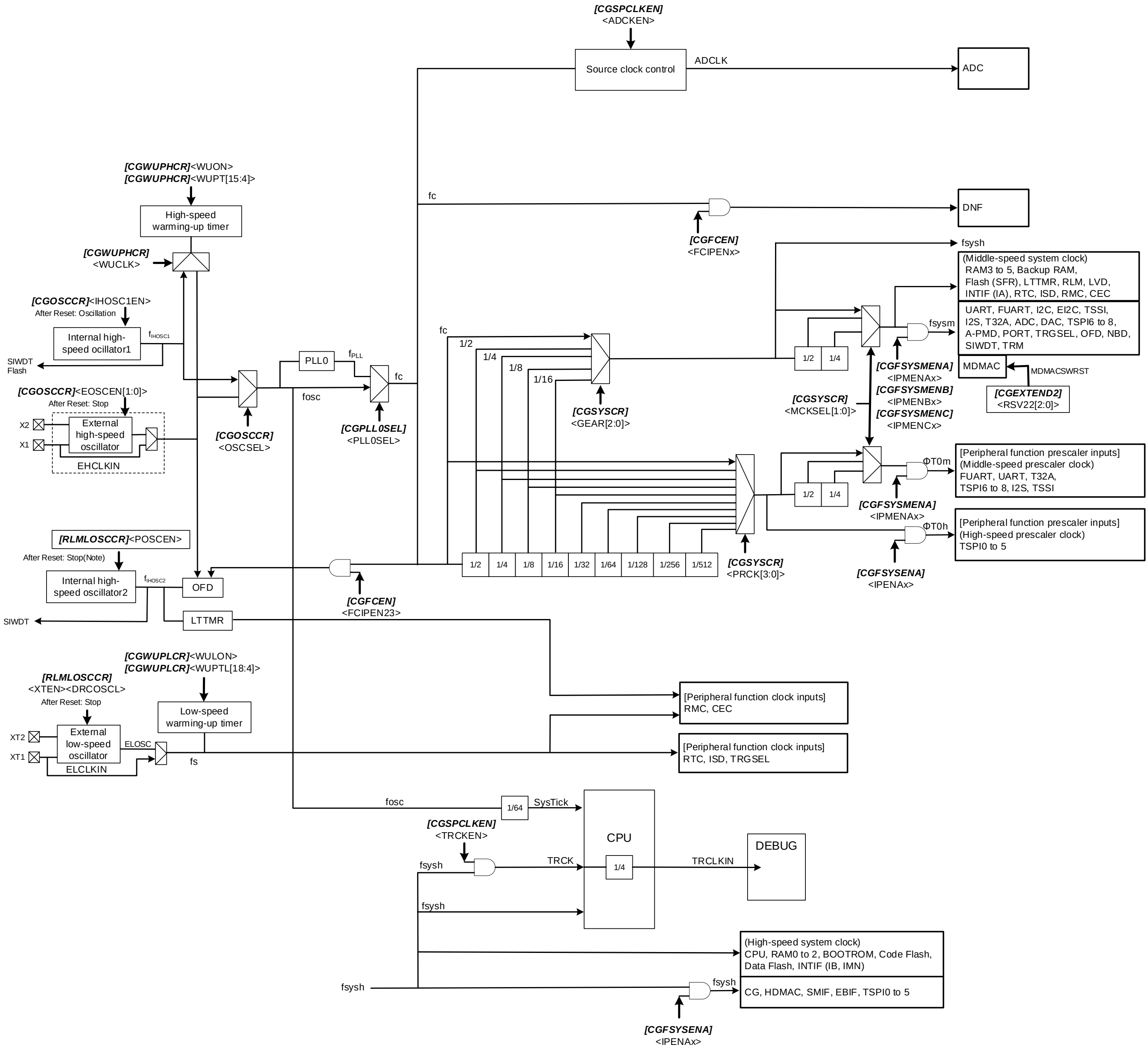
A clock setup is initialized to the following states by a reset action.

External high-speed oscillator:	Stop
Internal high-speed oscillator 1:	Oscillation
Internal high-speed oscillator 2:	Stop (Note)
External low-speed oscillator:	Stop
PLL (multiplying circuit) :	Stop
Gear clock:	fc (no frequency dividing)

Note: The state after the initialization done by RESET_N pin depends on ***[RLMLOSCCR]***<POSCEN> setting.

1.2.3. Clock System Diagram

The figure below shows a clock system diagram.



Note: The state after the initialization done by the reset from the pin depends on ***[RLMLOSCCR]***<POSCEN> setting.

Figure 1.1 Clock System Diagram

1.2.4. Warming-up Function

A warming-up function is used to secure the oscillation stable time at the time of the STOP1 mode release which starts the warming-up timer for high-speed oscillation automatically.

It is available also as a count up timer which uses the exclusive warming-up timer of high-speed clock /each low-speed clock for the waiting for the stability of an external oscillator or an internal oscillator.

This chapter explains the setting method to the register for warming-up timers, and the case where it is used as a count up timer. The detailed explanation at the time of STOP1 mode release, refer to "1.3.3.2. Warming Up at Release of Low-power Consumption Mode".

1.2.4.1. Warming-up Timer for High-speed Oscillation

A 16-bit up-counter is built in as a warming-up timer only for a high-speed oscillation. Also, when setting before changes to the STOP1 mode, the setting value is calculated in the following formula, set ***[CGWUPHCR]***<WUPT[15:4]> to the upper 12 bits of the setting value. Lower 4 bits are ignored.

<Formula>

(When using external high-speed oscillator)

Warming-up timer setting value (16 bits) = (warming-up time (s) / clock period (s)) - 16

(Example) When 5ms of warming-up time is set up with 10 MHz (100 ns of clock periods) of oscillator

Warming-up timer setting value (16 bits) = (5ms / 100ns) - 16
= 50000 - 16
= 49984
= 0xC340

Since upper 12 bits are used, set the register as follows.

[CGWUPHCR]<WUPT[15:4]> = 0xC34

(When using internal high-speed oscillator 1)

Warming-up timer setting value (16 bits) = ((Warming-up time (s) -63.3μs) / clock period (s)) - 41

(Example) When 163.4μs of warming time is set up with 10 MHz (100 ns of clock periods) of oscillator

Warming-up timer setting value (16 bits) = ((163.4μs - 63.3μs) / 100ns) - 41
= (100.1μs / 100ns) - 41
= 960
= 0x03C0

Since upper 12 bits are used, set the register as follows.

[CGWUPHCR]<WUPT[15:4]> = 0x03C

In the case of 10MHz, the setting range is 0x03C ≤ <WUPT[15:4]> ≤ 0xFFF, the warming-up time is set from 163.4μs to 6.6194ms.

1.2.4.2. Warming-up Timer for Low-speed Oscillation

A 19-bit up-timer is built in as a warming-up timer only for a low-speed oscillation. The setting value is calculated in the following formula, set ***[CGWUPLCR]***<WUPT[18:4]> to the upper 15 bits of the setting value. Lower 4 bits are ignored. 16 is subtracted in order to perform the count for 4 bits of low ranks, even when a set point is "0".

<Formula>

Warming-up timer setting value (19 bits)
= (warming-up time (s) / clock period (s)) - 16

(Example) When 50 ms of warming time is set up with 32 kHz (clock period 31.25μs) of oscillator

Warming-up timer setting value (19 bits) = (50ms / 31.25μs) - 16
= 1600 - 16
= 1584
= 0x00630

Since upper 15 bits are used, set the register as follows.

[CGWUPLCR]<WUPTL[18:4]> = 0x0063

In the case of 32 kHz, it setting range is 0x0000 ≤ <WUPTL[18:4]> ≤ 0x7FFF, warming-up time is set from 500μs to 16.384s.

1.2.4.3. Directions for Warming-up Timer

The directions for a warming-up function are explained.

(1) Selection of a clock
In a high-speed oscillation, the clock classification (an internal oscillation/external oscillation) counted with a warming-up timer is selected by ***[CGWUPHCR]*****<**WUCLK>.

(2) Calculation of a warming-up timer setting value
The warming-up time can set any value to the timer for a high-speed oscillation/for a low-speed oscillation. Please compute and set up from each formula.

(3) Start of warming up, and a termination confirmation
When software (instruction) performs the start of warming-up, starting warming-up count is carried out by setting ***[CGWUPHCR]***<WUON> (or ***[CGWUPLCR]*****<**WULON>) to "1".
Termination is confirmed with ***[CGWUPHCR]***<WUEF> (or ***[CGWUPLCR]*****<**WULEF>) that becomes from "1" to "0". "1" indicates under warming up and "0" indicates termination. After a counting end, the timer is reset and returns to an initial state.
It is not forced to terminate, although "0" is written to ***[CGWUPHCR]***<WUON> (or ***[CGWUPLCR]***<WULON>) during timer operation. Writing "0" is ignored.

Note: Since it is operating with the oscillating clock, a warming-up timer includes an error, when oscillation frequency has fluctuation. Therefore, it should be taken as an approximate time.

1.2.5. Clock Multiplying Circuit (PLL) for fsys

The clock multiplying circuit outputs the f_{PLL} clock (up to 200MHz) multiplied by the optimum condition for the frequency (8 MHz to 24 MHz) of the output clock f_{OSC} of the high-speed oscillator.

So, it is possible to make the input frequency to an oscillator low-speed and to make an internal clock high-speed by this circuit.

1.2.5.1. PLL Setup after Reset Release

The PLL is disabled after reset release.

To use the PLL, set ***[CGPLL0SEL]***<PLL0SET[23:0]> to a multiplication value while ***[CGPLL0SEL]***<PLL0ON> is "0". Then wait until approximately 100 µs has elapsed as a PLL initial stabilization time, and set <PLL0ON> to "1" to start PLL operation.

After that, to use f_{PLL} clock, which is multiplied fosc, wait until approximately 400 µs has elapsed as a lock up time. Then set "1" to ***[CGPLL0SEL]***<PLL0SEL>.

Note that a warming-up time is required until PLL operation becomes stable using the warming-up function, etc.

1.2.5.2. Formula and Example of Setting of PLL Multiplication Value

The details of the items of ***[CGPLL0SEL]***<PLL0SET[23:0]> which set up a PLL multiplication value are shown below.

Table 1.1 Details of *[CGPLL0SEL]*<PLL0SET[23:0]> Setup

Items of PLL0SET	Function	
[23:17]	Correction value setting	The quotient of fosc / 450K (integer). For detail, refer to Table 1.2.
[16:14]	fosc setup	000: 6 ≤ fosc ≤ 7 100: 12 < fosc ≤ 15 001: 7 < fosc ≤ 8 101: 15 < fosc ≤ 19 010: 8 < fosc ≤ 10 110: 19 < fosc ≤ 24 011: 10 < fosc ≤ 12 111: Reserved (Unit: MHz)
[13:12]	Dividing setup	00: Reserved 01: Divided by 2 (× 1 / 2) 10: Divided by 4 (× 1 / 4) 11: Divided by 8 (× 1 / 8)
[11:8]	Fractional part of multiplication setting	0000: 0.0000 1000: 0.5000 0001: 0.0625 1001: 0.5625 0010: 0.1250 1010: 0.6250 0011: 0.1875 1011: 0.6875 0100: 0.2500 1100: 0.7500 0101: 0.3125 1101: 0.8125 0110: 0.3750 1110: 0.8750 0111: 0.4375 1111: 0.9375
[7:0]	Integer part of multiplication setup	0x00: 0 0x01: 1 0x02: 2 : 0xFD: 253 0xFE: 254 0xFF: 255

Note: A multiplication value is the total of <PLL0SET[7:0]> (integer part) and <PLL0SET[11:8]>(fractional part).

f_{PLL} is denoted by the following formulas.

f_{PLL} = fosc × (***[CGPLL0SEL]***<PLL0SET[7:0]> + ***[CGPLL0SEL]***<PLL0SET[11:8]>) × (***[CGPLL0SEL]***<PLL0SET[13:12]>)

Note1: Frequency accuracy is not guaranteed.
Note2: There is no Linearity in the frequency by the fractional part of multiplication setting.
Note3: $f_{PLL} \leq$ Maximum operating frequency

Table 1.2 PLL Correction Value (example)

fosc (MHz)	<PLL0SET[23:17]> (decimal, integral value)
8.00	18
10.00	23
12.00	27
16.00	36
20.00	45
24.00	54

A PLL correction value can be calculated below.

When fosc = 10.0 MHz, 10.0 / 0.45 = 22.22 ≈ 23 ; fractional part is rounded up.

The main examples of a setting of ***[CGPLL0SEL]***<PLL0SET[23:0]> are shown below.

(1) It multiplies by PLL, and dividing is carried out and the target clock frequency (f_{PLL}) is generated for input frequency (fosc).
(2) A dividing value is chosen from 1 / 2, 1 / 4, and 1 / 8.
(3) Moreover, set up the frequency after multiplication in the following ranges.
200 MHz ≤ (f_{OSC} × multiplication value) ≤ 400 MHz

Table 1.3 PLL0SET Setting Value (example)

fosc (MHz)	Multiplication value	Dividing value	f_{PLL} (MHz)	<PLL0SET[23:0]>
8.00	50.0000	1/2	200	0x245032
10.00	40.0000	1/2	200	0x2E9028
12.00	33.3150	1/2	199.89	0x36D521
16.00	25.0000	1/2	200	0x495019
16.00	12.5000	1/2	100	0x49580C
20.00	20.0000	1/2	200	0x5B9014
24.00	16.6575	1/2	199.89	0x6D9A10

1.2.5.3. Change of PLL Multiplication Value under Operation

It changes to a setup which sets "0" to ***[CGPLL0SEL]***<PLL0SEL> first, and does not use a PLL multiplication clock during PLL multiplication clock operation when changing a multiplication value. And ***[CGPLL0SEL]*** <PLL0ST> = 0 is read, after checking having changed to a setup which does not use a multiplication clock, ***[CGPLL0SEL]***<PLL0ON> is set to "0", and PLL is stopped.

Then, the multiplication value of ***[CGPLL0SEL]***<PLL0SET> is changed, as reset time of PLL, after about 100μs progress, ***[CGPLL0SEL]***<PLL0ON> is set to "1", and operation of PLL is started.

Then, ***[CGPLL0SEL]***<PLL0SEL> is set to "1" after locking up time (about 400μs) has elapsed.

Finally, ***[CGPLL0SEL]***<PLL0ST> is read and it checks having changed.

1.2.5.4. PLL Operation Start/stop/switching Procedure

(1) fc setup (PLL stop → PLL start)
As an fc setup, the example of switching procedure from the PLL stop state to the PLL operation state is as follows.

<<State before switching>>	
[CGPLL0SEL]<PLL0ON> = 0	Stop the PLL operation for fsys.
[CGPLL0SEL]<PLL0SEL> = 0	Select the setting of the PLL for fsys to "PLL is unused (fosc)".
[CGPLL0SEL]<PLL0ST> = 0	Indicate the status of the PLL for fsys to "PLL is unused (fosc)".
[CGSYSCR]<MCKSEL> = 00	Ratios of "high-speed system clock vs middle-speed system clock" and "high-speed prescaler clock vs middle-speed system clock" are 1:1.

<<Example of switching procedure>>		
1	***[CGSYSCR]***<MCKSEL[1:0]> = 01 or 1*	Ratios of "high-speed system clock vs middle-speed system clock" and "high-speed prescaler clock vs High-speed system clock" are changed.
2	***[CGSYSCR]***<MCKSELGST> and <MCKSELPST> are read.	Wait until they become the values set at Step 1.
3	***[CGPLL0SEL]***<PLL0SET[23:0]> = 0xX	A PLL multiplication value setup is chosen.
4	Wait 100 μs or more.	Latency time after a multiplication setup
5	***[CGPLL0SEL]***<PLL0ON> = 1	PLL operation for fsys is carried out to an oscillation.
6	Wait 400 μs or more.	PLL output clock stable latency time
7	***[CGPLL0SEL]***<PLL0SEL> = 1	PLL selection for fsys is carried out to PLL use (f_{PLL}).
8	***[CGPLL0SEL]***<PLL0ST> is read.	It waits until the PLL selection status for fsys becomes PLL use "(f_{PLL}) (= 1)".

Note1: Step 1 and 2 are executed when the ratio of the system clock should be changed.

Note2: Step 3 to 6 are unnecessary when the state before switching is ***[CGPLL0SEL]***<PLL0ON> = 1.
When changing from the state where the PLL output clock is stable, it can be changed to the PLL operation state by execution of only step 7 and 8.

(2) fc setup (PLL operation → PLL stop)
As an fc setup, the example of switching procedure from the PLL operation state to a PLL stop state is as follows.

<<State before switching>>	
[CGPLL0SEL]<PLL0ON> = 1	Sets the PLL for fsys to oscillate.
[CGPLL0SEL]<PLL0SEL> = 1	Selects the PLL for fsys to "PLL is used (f_{PLL})".
[CGPLL0SEL]<PLL0ST> = 1	Indicates the status of the PLL for fsys to "PLL is used (f_{PLL})".

<<Example of switching sequence>>		
1	***[CGPLL0SEL]***<PLL0SEL> = 0	Select the PLL for fsys to "PLL is unused (fosc)".
2	***[CGPLL0SEL]***<PLL0ST> is read.	Wait until the status of the PLL for fsys becomes "PLL is unused (fosc) (= 0)".
3	***[CGPLL0SEL]***<PLL0ON> =0	Set the PLL operation for fsys to stop.

1.2.6. System Clock

An internal high-speed oscillation clock or external high-speed oscillation clock (connected oscillator or clock input) can be used as a source of system clock.

The system clock consists of "high-speed system clock (fsysh) (up to 200MHz)" for high-speed operation and "middle-speed system clock (fsysm) (up to 100MHz)" which is generated by dividing high-speed system clock. Middle-speed system clock is used by peripheral function to save power dissipation without degrading CPU performance. The clock domains of the peripheral function can be checked in Table 1.4.

High-speed system clock is generated by dividing fc using ***[CGSYSCR]***<GEAR [2:0]> (clock gear). And middle-speed system clock is generated by dividing the high-speed system clock using ***[CGSYSCR]***<MCKSEL[1:0]>. Although a setting can be changed during operation, after register writing before the clock actually changes, a time interval shown in Table 1.5 is required. The completion of the clock change should be checked by ***[CGSYSCR]***<GEARST [2:0]> and <MCKSELGST[1:0]>.

Table 1.4 Clock Domains of CPU and Peripherals

Clock domain	Functions
High-speed system clock	CPU, code Flash, data Flash, HDMAC, EBIF, SMIF, TSPI (ch0 to 5), CG, INTIF, RAM0 to 2, Boot ROM
Middle-speed system clock	MDMAC, NBDIF, I2C, SIWDT, UART, FUART, DAC, TSPI (ch6 to 8), T32A, ADC, Port, PMD, DNF, LTTMR, LVD, RLM, ISD, TRM, Flash (SFR), OFD, EI2C, I2S, FIR, TSSI, TRGSEL, RAM3 to 5, Backup RAM

Table 1.5 Time Interval for Changing System Clock

System clock	High speed (fsysh)	Middle speed (fsysm)
fsys	up to 16 clocks of fc	up to 16 clocks of fc
fsys / 2	-	up to 32 clocks of fc
fsys / 4	-	up to 64 clocks of fc

Note1: The clock gear and the system clock should not be changed while the peripheral function such as the timer/counter is operating.

Note2: An access between high-speed system clock domain and middle-speed system clock domain cannot be done when the system clock is changing.

Table 1.6 shows the example of operating frequency by the clock gear ratio (1/1 to 1/16) to the frequency fc set up with oscillation frequency, a PLL multiplication value, etc.

Table 1.6 Example of Operating Frequency

External oscillation (MHz)	External clock input (MHz)	Internal oscillation IHOSC1 (MHz)	PLL multiplication value (after dividing)	Maximum frequency (fc) (MHz)	Operating frequency by clock gear ratio (MHz) PLL = ON					Operating frequency by clock gear ratio (MHz) PLL = OFF				
					1/1	1/2	1/4	1/8	1/16	1/1	1/2	1/4	1/8	1/16
8	8	-	25	200	200	100	50	25	12.5	8	4	2	1	-
10	10	10	20	200	200	100	50	25	12.5	10	5	2.5	1.25	-
12	12	-	16	192	192	96	48	24	12	12	6	3	1.5	-
16	16	-	12	192	192	96	48	24	12	16	8	4	2	1
20	20	-	10	200	200	100	50	25	12.5	20	10	5	2.5	1.25

Table 1.7 Operating Frequency Examples of High-speed and Middle-speed System Clocks

High-speed system clock fsysh (MHz)	Middle-speed system clock fsysm (MHz)		
	1/1	1/2	1/4
200	-	100	50
160	-	80	40
100	100	50	25
80	80	40	20

Note: The maximum frequency of middle-speed system clock is 100 MHz.

1.2.6.1. Setting Method of System Clock

(1) fosc setup (internal oscillation → external oscillation)
As a fosc setup, the example of switching procedure to the external high-speed oscillator (EHOSC) from an internal high-speed oscillator 1 (IHOSC1) is shown below.

<<State before switching>>	
[CGOSCCR]<IHOSC1EN> = 1	An internal high-speed oscillator 1 oscillates.
[CGOSCCR]<OSCSEL> = 0	The high-speed oscillation selection for fosc is an internal high-speed oscillator 1 (IHOSC1).
[CGOSCCR]<OSCF> = 0	The high-speed oscillation selection status for fosc is an internal high-speed oscillator 1 (IHOSC1).
An oscillator is connected to X1 and X2 pins. (Note)	-

Note: Do not connect any devices except a resonator.

<<Example of switching procedure>>		
1	***[PYPDN]***<bit[1:0]> = 00 ***[PYPUP]***<bit[1:0]> = 00 ***[PYIE]***<bit[1:0]> = 00	Disable the pull-down resistors of X1 and X2 pins. Disable the pull-up resistors of X1 and X2 pins. Disable input control of X1 and X2 pins.
2	***[CGOSCCR]***<EOSCEN[1:0]> = 01	It is an external oscillation (EHOSC) about selection of an external oscillation of operation.
3	***[CGWUPHCR]***<WUCLK> = 1 ***[CGWUPHCR]***<WUPT[15:4]> = arbitrary value	It is the external oscillation (EHOSC) about high-speed oscillation warming-up clock selection. Oscillator stable time is set to a warming-up timer setting value.
4	***[CGWUPHCR]***<WUON> = 1	High-speed oscillation warming up is started.
5	***[CGWUPHCR]***<WUEF> is read.	It waits until it becomes the termination of high-speed oscillation warming up (= 0).
6	***[CGOSCCR]***<OSCSEL> = 1	It is high-speed oscillation selection for fosc to the external high-speed oscillator (EHOSC).
7	***[CGOSCCR]***<OSCF> is read.	It waits until the high-speed oscillation selection status for fosc becomes external high-speed oscillator (EHOSC) (= 1).
8	***[CGOSCCR]***<IHOSC1EN> = 0	An internal high-speed oscillator 1 is stopped.

(2) fosc setup (internal oscillation → external clock input)
As a fosc setup, the example of switching procedure to the external clock input (EHCLKIN) from an internal oscillator 1 (IHOSC1) is shown below.

<<State before switching>>	
[CGOSCCR]<IHOSC1EN> = 1	An internal high-speed oscillator 1 oscillates.
[CGOSCCR]<OSCSEL> = 0	The high-speed oscillation selection for fosc is an internal high-speed oscillator 1 (IHOSC1).
[CGOSCCR]<OSCF> = 0	The high-speed oscillation selection status for fosc is an inside (IHOSC1).
Clock is input to EHCLKIN.	Input in the proper voltage range.

<< Example of switching procedure >>		
1	***[PYPDN]***<bit[0]> = 0 ***[PYPUP]***<bit[0]> = 0 ***[PYIE]***<bit[0]> = 0/1	Disable the pull-down resistor of X1/EHCLKIN pin. Disable the pull-up resistors of X1/EHCLKIN pin. Input control of X1/EHCLKIN pin can be arbitrarily set.
2	***[CGOSCCR]***<EOSCEN[1:0]> = 10	Selection of an external oscillation of operation is carried out to an external high-speed clock input (EHCLKIN).
3	***[CGOSCCR]***<OSCSEL> = 1	It is high-speed oscillation selection for fosc to the external high-speed oscillation.
4	***[CGOSCCR]***<OSCF> is read.	It waits until the high-speed oscillation selection status for fosc becomes external high-speed oscillation (= 1).
5	***[CGOSCCR]***<IHOSC1EN> = 0	An internal high-speed oscillator 1 is stopped.

(3) fosc setup (external oscillation/external clock input → internal oscillation)
As a fosc setup, the example of switching procedure to the internal high-speed oscillator 1 (IHOSC1) from an external high-speed oscillator (EHOSC) or an external clock input (EHCLKIN) is shown below.

<<State before switching>>	
[CGOSCCR]<EOSCEN[1:0]> = 01 or 10	Selection of an external oscillator of operation is an external high-speed oscillator (EHOSC) or external high-speed clock input.
[CGOSCCR]<OSCSEL> = 1	The high-speed oscillation selection for fosc is the external high-speed oscillation (EHOSC).
[CGOSCCR]<OSCF> = 1	The high-speed oscillation selection status for fosc is the external high-speed oscillation (EHOSC).

<<Example of switching procedure>>		
1	[CGWUPHCR]<WUCLK> = 0	Set the warming-up clock selection to internal high-speed oscillator 1 (IHOSC1).
2	***[CGWUPHCR]***<WUPT[15:4]> = 0x03C	Set the high-speed oscillation warming-up timer setting value of 163.4 μs (= 0x3C) or more.
3	***[CGOSCCR]***<IHOSC1EN> = 1	An internal high-speed oscillator 1 oscillates.
4	***[CGWUPHCR]***<WUON> = 1	Start the high-speed oscillation warming-up timer.
5	***[CGWUPHCR]***<WUEF> is read.	Wait until a warming-up timer status flag becomes ends (= 0).
6	***[CGOSCCR]***<OSCSEL> = 0	Set the high-speed oscillation selection for fosc to internal high-speed oscillator1 (IHOSC1).
7	***[CGOSCCR]***<OSCF> is read.	It waits until the internal high-speed oscillation selection status for fosc becomes an internal high-speed oscillation (IHOSC1) (= 0).
8	***[CGOSCCR]***<EOSCEN[1:0]> = 00	Set the selection of an external oscillator operation to unused.

1.2.7. Low-speed Clock

(1) ELOSC setup (not used low-speed clock → external low-speed oscillator used)
An example of setting procedure is shown as follows to use the external low-speed oscillator (ELOSC).

<<State before switching>>	
[RLMLOSCCR]<XTEN> = 0	A low-speed clock is not used.
[RLMLOSCCR]<DRCOSCL> = 0	The external low-speed clock input (ELCLKIN) is selected as the low-speed clock.

<<Example of switching procedure>>		
1	***[PYPDN]***<bit[3:2]> = 00 ***[PYPUP]***<bit[3:2]> = 00 ***[PYIE]***<bit[3:2]> = 00	The pull-down resistors on XT1/XT2 pins are disabled. The pull-up resistors on XT1/XT2 pins are disabled. Disable input control of XT1/XT2 pins.
2	***[RLMLOSCCR]***<DRCOSCL> = 1	The low-speed clock source is set to the external low-speed oscillator (ELOSC).
3	***[RLMLOSCCR]***<XTEN> = 1	The low-speed clock is used.
4	***[RLMLOSCCR]***<XTEN> is read.	It waits until using a low-speed clock status becomes "used (= 1)".
5	***[CGWUPLCR]***<WUPTL> = arbitrary value	Set the low-speed oscillation warming-up timer setting value.
6	***[CGWUPLCR]***<WULON> = 1	Start the low-speed oscillation warming-up timer.
7	***[CGWUPLCR]***<WULEF> is read.	It waits until it becomes the termination of low-speed oscillation warming up (= 0).

(2) ELCLKIN setup (No Operation of External Low-speed Oscillator → Operation)
An example of setting procedure is shown as follows to use the external low-speed clock input (ELCLKIN).

<<State before switching>>	
[RLMLOSCCR]<XTEN> = 0	A low-speed clock is not used.
[RLMLOSCCR]<DRCOSCL> = 0	The external low-speed clock input (ELCLKIN) is selected as the low-speed clock.

<<Example of switching procedure>>		
1	***[PYPDN]***<bit[2]> = 0 ***[PYPUP]***<bit[2]> = 0 ***[PYIE]***<bit[2]> = 1	Disable the pull-down resistor on XT1/ELCLKIN pin. Disable the pull-up resistor on XT1/ELCLKIN pin. Enable input control of XT1/ELCLKIN pin.
2	***[RLMLOSCCR]***<DRCOSCL> = 0	The external low-speed clock source is set to the external low-speed clock input (ELCLKIN).
3	***[RLMLOSCCR]***<XTEN> = 1	The low-speed clock is used.
4	***[RLMLOSCCR]***<XTEN> is read.	It waits until using a low-speed clock status becomes "used (= 1)".

1.2.8. Clock Supply Setting Function

TMPM4G Group (1) has the clock on/off function for the peripheral circuits. To reduce the power consumption, TMPM4G Group (1) can stop supplying the clock to the peripheral functions that are not used.

Except some peripheral functions, clocks are not supplied after reset.

To supply the clock of the function to be used, set the bit of relevance of ***[CGFSYSENA]***, ***[CGFSYSMENA]***, ***[CGFSYSMENB]***, ***[CGFSYSMENC]***, ***[CGSPCLKEN]*** and ***[RLMLOSCCR]*** to "1".

For details, refer to "1.4. Registers".

1.2.9. Prescaler Clock

Each peripheral function has a prescaler circuit to divide the ΦT0 clock. ΦT0h or ΦT0m of prescaler clock is input to them. For which clock is input for each peripheral function, refer to "Figure 1.1 Clock System Diagram".

The clock which the divider divides fc by ***[CGSYSCR]***<PRCK[3:0]> is ΦT0h.

The clock which the divider divides ΦT0h by ***[CGSYSCR]***<MCKSEL[1:0]> is ΦT0m.

For ΦT0 clock after reset, fc is chosen.

After each register writing before a clock actually changes, a time interval shown in Table 1.8 is required.

To confirm the completion of the clock change, check the status of ***[CGSYSCR]***<PRCKST[3:0]> or <MCKSELPST[1:0]>.

Table 1.8 Time Interval for Changing Prescaler Clock

Prescaler clock	High speed (ΦT0h)	Middle speed (ΦT0m)
ΦT0	512 fc cycles at maximum	Up to 512 fc cycles
ΦT0/2	-	Up to 1024 fc cycles
ΦT0/4	-	UP to 2048 fc cycles

Note1: Do not change a prescaler clock during operation of peripheral functions, such as a timer counter.

Note2: An access between high-speed system clock domain and middle-speed system clock domain cannot be done when the prescaler clock is changing.

1.3. Operation Mode

There are NORMAL mode and a low-power consumption mode (IDLE, STOP1, and STOP2) in TMPM4G Group (1) as an operation mode, and it can reduce power consumption by performing mode transition according to directions for use.

1.3.1. Details of Operation Mode

1.3.1.1. Feature in Each Mode

The feature in NORMAL, low-power consumption modes is as follows.

- NORMAL mode
  It is a mode to operate a CPU core and peripheral circuits by a high-speed oscillation clock. After the reset release, operation mode is NORMAL mode.

- Low-power consumption mode
  Low-power consumption modes are as following.

  - IDLE mode
    It is the mode which CPU stops.
    The peripheral function should perform operation/stop by the register of each peripheral function, a clock supply setting function, etc.

Note: CPU cannot clear the watchdog timer in IDLE mode.

  - STOP1 mode
    It is the mode which all the internal circuits also including an internal oscillator stop.
    However, when an external low-speed oscillator is oscillating and it shifts to STOP1 mode, the RTC, CEC, RMC and ISD operate.
    If it shifts to STOP1 mode when the internal high-speed oscillator 2 (IHOSC2) is oscillating and LTTMR is selected as a sample clock, the CEC and RMC operate.
    If the STOP1 mode is released, an internal high-speed oscillator1 (IHOSC1) will start, and operation mode will return to NORMAL mode.
    Please disable interrupt which is not used for STOP1 release before shifting to the STOP1 mode.

  - STOP2 mode
    It is the mode which holds a part of functions and cut off internal electrical power source. STOP1 consumption of electric power larger than the STOP2 mode can be held down. If the STOP2 mode is released, power supply will be switched on to the main power domain, a reset sequence will be performed, and it will return to NORMAL mode.
    As for the main power domain, it is a function which does not supply a power supply in STOP2 mode.

Before shifting to the STOP2 mode, disable an interrupt which is not made into a release STOP2, please be sure to set up ***[RLMSHTDNOP]***<PTKEEP> = 1 and to hold the state of each port.

An output/pull-up holds, and input permission hold a state when it sets as a port keeping function. In addition, external interrupt continues an input.

This product will be cut off the power except for the following circuit in STOP2 mode.

- External low-speed oscillator (ELOSC)
- RTC
- Backup RAM
- Port pin status
- LVD
- RMC
- ISD
- CEC
- LTTMR
- RLM
- IA
- Internal high-speed oscillator 2 (IHOSC2)

Regarding a power supply cut off in the low-power consumption mode, for details, refer to "1.3.1.4. Peripheral Function State in Low-power Consumption Mode".

1.3.1.2. Transition to and Return from Low-power Consumption Mode

To shift to each low-power consumption mode, the IDLE/STOP1/STOP2 mode is chosen by standby control register ***[CGSTBYCR]***<STBY[1:0]>, and a WFI instruction is executed. When the transition to the low-power consumption mode has been done by WFI instruction, the return from a low-power consumption mode is performed by reset or interrupt generating. To return by an interrupt, it is necessary to set up. Please refer to "interrupt" chapter of a reference manual "Exception" for details.

Note1: TMPM4G Group (1) does not support a return by events; therefore, do not make a transition to low-power consumption mode triggered by WFE (Wait For Event).

Note2: TMPM4G Group (1) does not support low-power consumption mode by SLEEPDEEP of the Cortex-M4 processor with FPU core. Do not use the <SLEEPDEEP> bit of the system control register.

1.3.1.3. Selection of Low-power Consumption Mode

Low-power consumption mode selection is chosen by setup of ***[CGSTBYCR]***<STBY[1:0]>.

Following table shows the mode chosen from a setup of <STBY[1:0]>.

Table 1.9 Low-power Consumption Mode Selection

Mode	*[CGSTBYCR]*<STBY[1:0]>
IDLE	00
STOP1	01
STOP2	10

Note: Do not use the settings other than the above.

1.3.1.4. Peripheral Function State in Low-power Consumption Mode

The following Table 1.10 shows the operation state of the peripheral function (block) in each low-power consumption mode.

In addition, after reset release, it will be in the state where a clock is not supplied except for some blocks.

If needed, set up ***[CGFSYSENA]***, ***[CGFSYSMENA]***, ***[CGFSYSMENB]***, ***[CGFSYSMENC]***, ***[CGFCEN]***, ***[CGSPCLKEN]*** and enable clock supply.

Table 1.10 Block Operation Status in Each Low-power Consumption Mode

Block		NORMAL	IDLE	STOP1		STOP2 (Note1)	
				ELOSC On	ELOSC Off	ELOSC On	ELOSC Off
Processor core (debug included)		✓	-	-	-	x	x
HDMAC		✓	✓	-	-	x	x
MDMAC		✓	✓	-	-	x	x
I/O port	Pin status	✓	✓	✓	✓	✓ (Note3)	✓ (Note3)
	Register	✓	✓	-	-	x	x
EBIF, ADC, DAC, UART, FUART, I2C, EI2C, TSPI, SMIF, I2S, FIR, A-PMD, T32A, TRGSEL		✓	✓	-	-	x	x
LTTMR		✓ (Note5)	✓ (Note5)	✓ (Note5)	✓ (Note5)	✓ (Note5)	✓ (Note5)
RTC		✓	✓	✓	-	✓	-
RMC		✓	✓	✓	-	✓	✓ (Note4)
CEC		✓	✓	✓	-	✓	✓ (Note4)
ISD		✓	✓	✓	-	✓	-
SIWDT		✓	✓ (Note2)	✓ (Note2)	✓ (Note2)	x	x
LVD		✓	✓	✓	✓	✓	✓
OFD		✓	✓	-	-	x	x
TRM		✓	Unavailable	-	-	x	x
CG		✓	✓	✓	✓	x	x
PLL		✓	✓	-	-	x	x
External high-speed oscillator (EHOSC)		✓	✓	-	-	x	x
Internal high-speed oscillator 1 (IHOSC1)		✓	✓	-	-	x	x
Internal high-speed oscillator 2 (IHOSC2)		✓ (Note5)	✓ (Note5)	✓ (Note5)	✓ (Note5)	✓ (Note5)	✓ (Note5)
External low-speed oscillator (ELOSC)		✓	✓	✓	-	✓	-
RLM (Note7)		✓	✓	✓	✓	✓	✓
Code Flash		Access Possible	Access Possible (Note6)	Data hold	Data hold	Data hold	Data hold
Data Flash							
RAM						x	x
Backup RAM						Data hold	Data hold

✓: Operation is possible.

-: If it shifts to the object mode, the clock to peripheral circuits stops automatically.

×: If it shifts to the object mode, the power supply to the module is cut-off automatically. When returning, initialized by the reset.

Note1: Check that the peripheral function is not operating and change to STOP 2 mode.

Note2: Stop SIWDT before shifting to the IDLE/STOP1 mode except protection A mode.

Note3: A port state when the ***[RLMSHTDNOP]***<PTKEEP> is set to "1" is held.

Note4: This peripheral circuit can operate by using LTTMR as a sampling clock.

Note5: This peripheral circuit can operate when ***[RLMLOSCCR]***<POSCEN> is set to "1".

Note6: It becomes a data hold when peripheral functions (DMA etc.) which carry out data access (R/W), except CPU, are not connected on the bus matrix.

Note7: RLM means the registers to control the power, the low-speed oscillator, and others in the region where the power is not cut off.

1.3.2. Mode State Transition

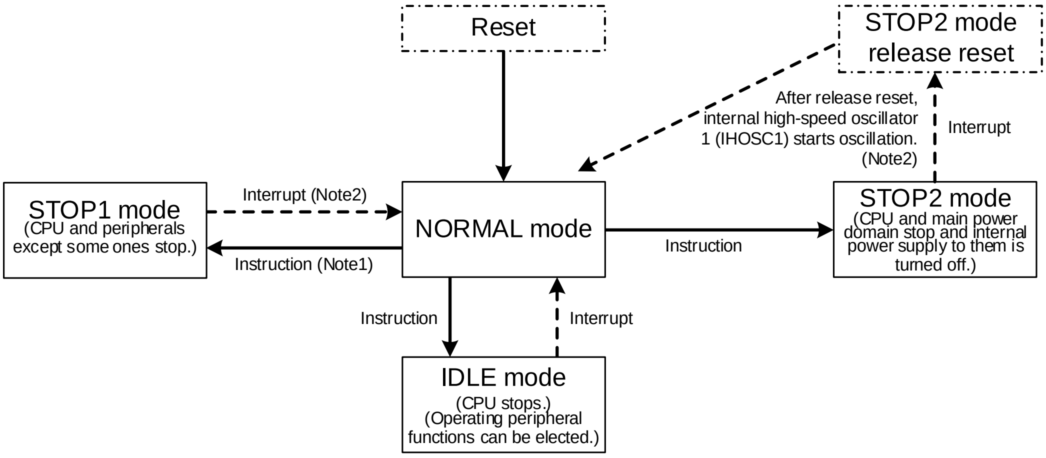


Figure 1.2 Change State Transition

Note1: Warm-up is required at returning. A warming-up time must be set in the previous mode (NORMAL mode) before entering to STOP1 mode.

Note2: When the TMPM4G Group (1) returns from STOP2 mode, the TMPM4G Group (1) branches to the interrupt service routine triggered by reset. When the TMPM4G Group (1) returns from STOP1 mode, the TMPM4G Group (1) branches to the interrupt service routine triggered by interrupt events.

1.3.2.1. IDLE Mode Transition Flow

Set up the following procedure at transition to IDLE mode.

Because IDLE mode is released by an interrupt, set the interrupt before transition to IDLE mode. For the interrupts that can be used to release the IDLE mode, refer to "1.3.3.1. Release Source of Low-power Consumption Mode". Disables unused interrupts and unavailable interrupts for release.

Transition procedure (from NORMAL mode)		
1	***[SIWDxEN]***<WDTE> = 0	Disable SIWDT.
2	***[SIWDxCR]***<WDCR[7:0]> = 0xB1	Disable SIWDT.
3	***[FCSR0]***<RDYBSY> is read.	It waits until Flash will be in a Ready state (= 1).
4	***[CGSTBYCR]***<STBY[1:0]> = 00	Low-power consumption mode selection is set to IDLE mode.
5	***[CGSTBYCR]***<STBY[1:0]> is read.	Confirm "00" is written to the register at the step 4.
6	WFI command execution	Transit to IDLE mode

Note: When using the protection A mode of SIWDT, step 1 and 2 are not required.

1.3.2.2. STOP1 Mode Transition Flow

Set up the following procedure at transition to STOP1 mode.

Because STOP1 mode is released by an interrupt, set the interrupt before transition to STOP1 mode. For the interrupts that can be used to release the STOP1 mode, refer to "1.3.3.1. Release Source of Low-power Consumption Mode". Disables unused interrupts and unavailable interrupts for release STOP1 mode.

Transition procedure (from NORMAL mode)		
1	***[SIWDxEN]***<WDTE> = 0	Disable SIWDT.
2	***[SIWDxCR]***<WDCR[7:0]> = 0xB1	Disable SIWDT.
3	***[FCSR0]***<RDYBSY> is read	Wait until Flash becomes the Ready state (= 1).
4	***[CGWUPHCR]***<WUEF> is read	Wait until the high-speed oscillation warming-up ends (= 0).
5	***[CGWUPHCR]***<WUCLK> = 0	Set the warming-up clock selection to internal high-speed oscillator 1 (IHOSC1).
	[CGWUPHCR]<WUPT[15:4]> = 0x3C	Set the high-speed oscillation warming-up timer setting value of 163.4 μs (= 0x03C) or more.
6	***[CGSTBYCR]***<STBY[1:0]> = 01	Low-power consumption mode selection is set to STOP1 mode.
7	***[CGPLL0SEL]***<PLL0SEL> = 0	Select the PLL for fsys to "PLL is unused (fosc)".
8	***[CGPLL0SEL]***<PLL0ST> is read	Wait until the status of the PLL for fsys becomes "PLL is unused (fosc) (= 0)".
9	***[CGPLL0SEL]***<PLL0ON> = 0	Stop PLL for fsys.
10	***[CGOSCCR]***<IHOSC1EN> = 1	Enable the internal high-speed oscillator 1 (IHOSC1).
11	***[CGWUPHCR]***<WUON> = 1	Start the high-speed oscillation warming-up timer.
12	***[CGWUPHCR]***<WUEF> is read.	Wait until a warming-up timer status flag becomes ends (= 0).
13	***[CGOSCCR]***<OSCSEL> = 0	Set the high-speed oscillation selection for fosc to internal high-speed oscillator1 (IHOSC1).
14	***[CGOSCCR]***<OSCF> is read	Wait until the high-speed oscillation selection status for fosc becomes internal high-speed oscillator1 (IHOSC1). (= 0).
15	***[CGOSCCR]***<EOSCEN[1:0]> = 00	Set the selection of an external oscillator operation to unused.
16	***[RLMLOSCCR]***<POSCEN> = 0 or 1	Setting for the internal high-speed oscillator 2 (IHOSC2). 0: Except following condition 1: When the LTTMR operates in STOP1 mode
17	***[CGOSCCR]***<EOSCEN[1:0]> is read	The register writing in step 15 is checked (= 00).
18	***[RLMLOSCCR]***<POSCF> is read	Wait until the status of the internal high-speed oscillator 2 (IHOSC2) becomes the value set at step16.
19	WFI command execution	Transit STOP1 mode.

Note: When using the protection A mode of SIWDT, step 1, 2, 16 and 18 are not required.

1.3.2.3. STOP2 Mode Transition Flow

Set up the following procedure at transition to STOP2 mode.

Because STOP2 mode is released by an interrupt, set the interrupt before transition to STOP2 mode. For the interrupts that can be used to release the STOP2 mode, refer to "1.3.3.1. Release Source of Low-power Consumption Mode". Disables unused interrupts and unavailable interrupts for release STOP2 mode.

Transition procedure		
1	***[SIWDxEN]***<WDTE> = 0	Disable SIWDT.
2	***[SIWDxCR]***<WDCR[7:0]> = 0xB1	Disable SIWDT.
3	***[FCSR0]***<RDYBSY> is read.	Wait until Flash becomes the ready state (= 1).
4	***[RLMSHTDNOP]***<PTKEEP> = 1	I/O control signal is made to hold.
5	***[CGSTBYCR]***<STBY[1:0]> = 10	Low-power consumption mode selection is set to STOP2 mode.
6	***[CGPLL0SEL]***<PLL0SEL> = 0	Select the PLL for fsys to "PLL is unused (fosc)".
7	***[CGPLL0SEL]***<PLL0ST> is read.	Wait until PLL status of fsys becomes off state (= 0).
8	***[CGPLL0SEL]***<PLL0ON> = 0	Stop PLL for fsys.
9	***[CGWUPHCR]***<WUCLK> = 0 ***[CGWUPHCR]***<WUPT[15:4]> = 0x03C	Set the warming-up clock selection to internal high-speed oscillator 1 (IHOSC1). Set the high-speed oscillation warming-up timer to 163.4 μs (= 0x03C) or more.
10	***[CGOSCCR]***<IHOSC1EN> = 1	Enable the internal high-speed oscillator 1 (IHOSC1).
11	***[CGWUPHCR]***<WUON> = 1	Start the high-speed oscillation warming-up timer
12	***[CGWUPHCR]***<WUEF> is read.	Wait until the warming-up timer status flag becomes ends (= 0).
13	***[CGOSCCR]***<OSCSEL> = 0	Set the high-speed oscillation selection for fosc to internal high-speed oscillator1 (IHOSC1).
14	***[CGOSCCR]***<OSCF> is read	Wait until the high-speed oscillation selection status for fosc becomes internal high-speed oscillator1 (IHOSC1) (= 0).
15	***[CGOSCCR]***<EOSCEN[1:0]> = 00	Set the selection of an external oscillator operation to unused.
16	***[RLMLOSCCR]***<POSCEN> = 0 or 1	Setting for the internal high-speed oscillator 2 (IHOSC2). 0: Except following condition 1: When the LTTMR operates in STOP2 mode
17	***[CGOSCCR]***<EOSCEN[1:0]> is read.	The register writing in step 15 is checked (= 00).
18	***[RLMLOSCCR]***<POSCF> is read.	Wait until the status of internal high-speed oscillator 2 (IHOSC2) becomes the value set at step16.
19	***[RLMRSTFLG0]***<STOP2RSTF> = 0 ***[RLMRSTFLG0]***<PINRSTF> = 0	STOP2 reset flag and reset pin flag are cleared (Note).
20	WFI command execution	Transit to STOP2 mode.
21	Jump instruction	Return to step 20.

Note: Refer to the reference manual "Exception" for a reset flag register ***[RLMRSTFLG0]***.

1.3.3. Return Operation from Low-power Consumption Mode

1.3.3.1. Release Source of Low-power Consumption Mode

Interrupt, Non-Maskable Interrupt, and reset can perform release from a low-power consumption mode. The low-power consumption mode release source which can be used is decided by a low-power consumption mode.

It shows the following table about details.

Table 1.11 Release Source List

Low-power consumption mode			IDLE	STOP1	STOP2
Release Source	Interrupt	INT00 to INT15 (Note)	✓	✓	✓
		INTRTC	✓	✓	✓
		INTCECxRX, INTCECxTX	✓	✓	✓
		INTISDx	✓	✓	✓
		INTRMCx	✓	✓	✓
		INTLTTMRx	✓	✓	✓
		INTHDMAxTC, INTHDMAxERR	✓	-	x
		INTMDMAxTC, INTMDMAxBERR, INTMDMAxDERR	✓	-	x
		INT32Ax_A_CT, INT32Ax_B_Cx_CPC	✓	-	x
		INTADxCP0, INTADxCP1, INTADxTRG, INTADxSGL, INTADxCNT, INTADxHP	✓	-	x
		INTEMGx, INTOVVx, INTPWMx	✓	-	x
		INTTxRX, INTTxTX, INTTxERR	✓	-	x
		INTSMIx	✓	-	x
		INTUARTxRX, INTUARTxTX, INTUARTxERR	✓	-	x
		INTFUARTx	✓	-	x
		INTFLCRDY, INTFLDRDY	✓	-	x
		INTI2CxNST, INTI2CxATX, INTI2CxBX, INTI2CxNA	✓	-	x
		INTI2SxSI, INTI2SxSIERR, INTI2SxSO, INTI2SxSOERR	✓	-	x
		INTFIR	✓	-	x
		INTISSIxRX, INTSSIxTX, INTSSIxERR	✓	-	x
	SysTick interrupt		✓	-	-
	Non-Maskable Interrupt (INTWDT0)		✓	✓	-
	Non-Maskable Interrupt (INTLVD)		✓	✓	✓
	Reset (SIWDT)		✓	✓	-
	Reset (LVD)		✓	✓	✓
	Reset (OFD)		✓	-	-
	Reset (RESET_N pin)		✓	✓	✓

✓: It can be used for release. After release, the interrupt procedure will start.

-: It cannot be used for release.

Note: INT00 to INT15 (External Interrupt 00 to 15) can select one of falling edge, rising edge and level. For details, please refer to the reference manual "Exception".

- Released by an interrupt request
  When interrupt releases a low-power consumption mode, it is necessary to prepare so that interrupt may be detected by CPU. The interrupt used for release in STOP1 and STOP2 modes needs to set for detecting the interrupt by INTIF other than a setting of CPU.

- Released by Non-Maskable interrupt (NMI)
  The factor of NMIs is SIWDT interrupt (INTWDT0, protection mode A only) and LVD interrupt (INTLVD).

- Released by reset
  The reset can perform release from all the low-power consumption modes.
  When released by reset, all registers will be initialized in NORMAL mode after release. For detail, refer to "3.2.8.1. Reset Factor and Reset Range".

- Released by SysTick interrupt
  SysTick interrupt is available only in IDLE mode.

Refer to "Interrupt" chapter of a reference manual of "Exception" about the details of interrupt.

1.3.3.2. Warming Up at Release of Low-power Consumption Mode

Warming up may be required because of stability of an internal oscillator at the time of mode transition.

When the transition from STOP1 mode to NORMAL mode is done, an internal oscillator 1 (IHOSC1) is selected automatically and the warming-up timer is started. The output of a system clock is started after warming-up time elapsed.

For this reason, before executing the instruction which transit to the STOP1 mode, set up warming-up time by ***[CGWUPHCR]***<WUPT[15:4]>. For the setting method, refer to "1.2.4.1. Warming-up Timer for High-speed Oscillation".

The following table shows the necessity of warming-up setup at the time of each operation mode transition.

Table 1.12 Warming Up

Operation mode transition	Warming-up setup
NORMAL → IDLE	Not required
NORMAL → STOP1	Not required
NORMAL → STOP2	Not required
IDLE → NORMAL	Not required
STOP1 → NORMAL	Required
STOP2 → RESET → NORMAL	Not required

1.3.3.3. Restart Operation from STOP2 Mode

The restart operation flow from STOP2 mode release factor interrupt generating is as follows.

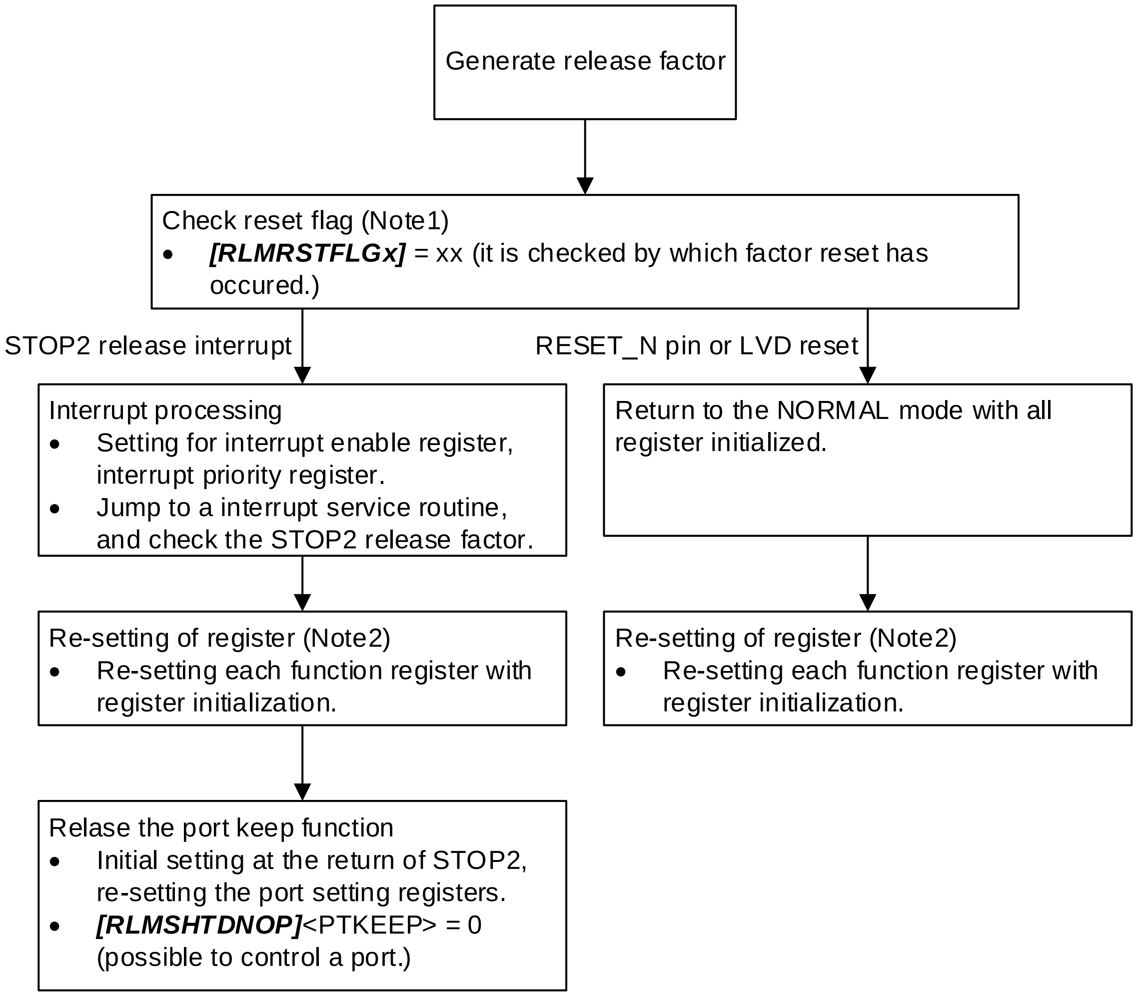


Figure 1.3 STOP2 Mode Restart Operation Flow

Note1: When STOP2 released by a RESET_N pin, as for a reset flag, both "STOP2 reset flag" and "reset pin flag" are set.

Note2: When STOP2 mode is released by LVD reset, as for a reset flag, both "STOP2 reset flag" and "reset pin flag" are materialized.

Note3: The reset range of registers is differ depending on the releasing STOP2 mode by an interrupt and by the reset of RESET_N pin or one of LVD. Refer to "3.2.8.1. Reset Factor and Reset Range" for detail.

1.3.4. Clock Operation by Mode Transition

The clock operation in case of mode transition is shown below.

1.3.4.1. NORMAL → IDLE → NORMAL Operation Mode Transition

CPU stops at IDLE mode. The clock supply to a peripheral function holds a setting state. Please perform operation/stop by the register of each peripheral function, a clock supply setting function, etc. if needed. Execution of warming-up operation is not performed at the time of the restart operation in NORMAL mode from IDLE mode.

After the transition instruction (WFI) execution which switch to IDLE mode, a program counter will indicate the next instruction and CPU stops. With a release source, it becomes a CPU start. In the case of an enable interrupt, the next instruction of the transition one (WFI) will be executed after the interrupt processing of release source.

1.3.4.2. NORMAL → STOP1 → NORMAL Operation Mode Transition

When returning to NORMAL mode from the STOP1 mode, warming up is started automatically.

Please set ***[CGWUPHCR]***<WUPT[15:4]> to warming-up time (163.4μs or more) before transition to the STOP1 mode.

Note: When releasing factor is RESET_N pin or LVD reset, CPU operation is started after the internal processing time for reset and the waiting time till CPU running, not the warming-up time elapse.
When reset factor is not released after the internal processing time for reset elapses, starts measuring elapsed time after releasing reset factor. CPU operation is started after the waiting time till CPU running elapse.

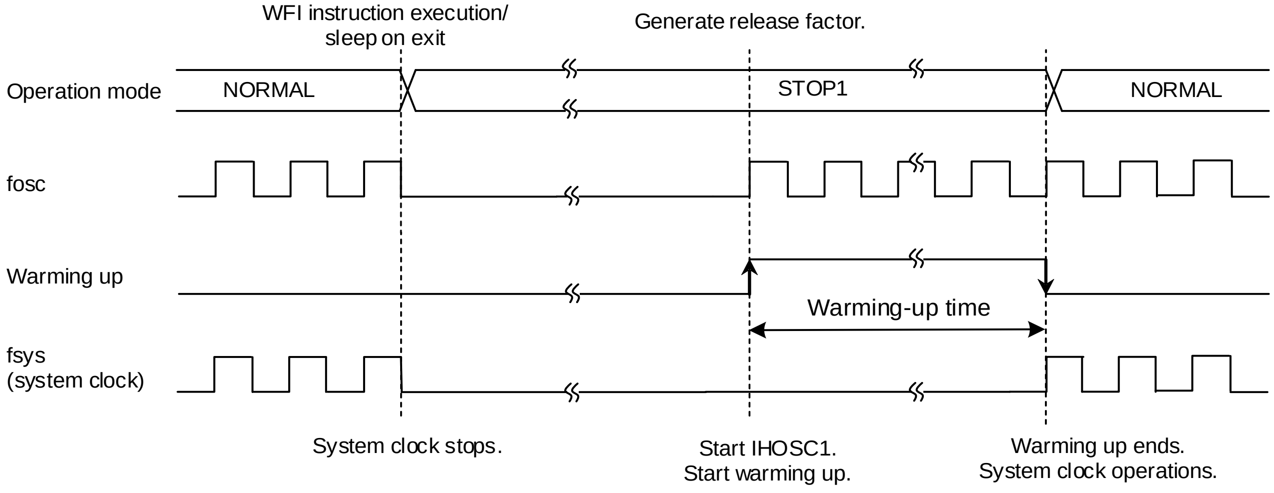


Figure 1.4 NORMAL → STOP1 → NORMAL Operation Mode Transition

1.3.4.3. NORMAL → STOP2 → RESET → NORMAL Operation Mode Transition

Warming up is not performed when returning to NORMAL mode.

Even when returning to NORMAL mode by no reset, the CPU branches to the interrupt routine of reset.

A reset operation is performed to an internal main power domain after STOP2 mode released. However, a reset operation is not performed to a backup power domain.

Note: When releasing factor is RESET_N pin or LVD reset, CPU operation is started after the internal processing time for reset and the waiting time till CPU running, not the warming-up time elapse.
When reset factor is not released after the internal processing time for reset elapses, starts measuring elapsed time after releasing reset factor. CPU operation is started after the waiting time till CPU running elapse.

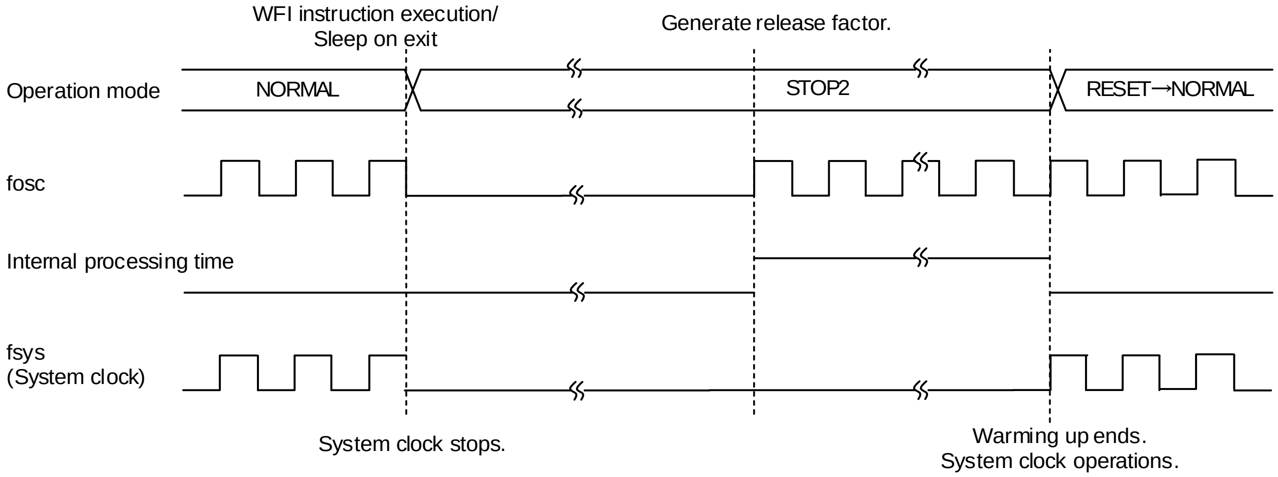


Figure 1.5 NORMAL → STOP2 → RESET → NORMAL Operation Mode Transition

1.4. Registers

1.4.1. List of Registers

The register related to CG and its address information are shown below.

Peripheral function		Channel/unit	Base address
Clock Control and Operation Mode	CG	-	0x40083000
Low-speed oscillation/ power control	RLM	-	0x4003E400

1.4.1.1. Clock Control and Operation Mode

Register name		Address (Base+)
CG Write Protection Register	*[CGPROTECT]*	0x0000
Oscillation Control Register	*[CGOSCCR]*	0x0004
System Clock Control Register	*[CGSYSCR]*	0x0008
Standby Control Register	*[CGSTBYCR]*	0x000C
PLL Selection Register for fsys	*[CGPLL0SEL]*	0x0020
High-Speed Oscillation Warming Up Register	*[CGWUPHCR]*	0x0030
Low-speed Oscillation Warming Up Register	*[CGWUPLCR]*	0x0034
Middle-speed Clock Supply and Stop Register C for fsysm	*[CGFSYSMENC]*	0x0044
Middle-speed Clock Supply and Stop Register A for fsysm	*[CGFSYSMENA]*	0x0048
Middle-speed Clock Supply and Stop Register B for fsysm	*[CGFSYSMENB]*	0x004C
High-speed Clock Supply and Stop Register A for fsysh	*[CGFSYSENA]*	0x0050
Clock Supply and Stop Register for fc	*[CGFCEN]*	0x0058
Clock Supply for ADC and Debug Circuit Register	*[CGSPCLKEN]*	0x005C
Function Extension Register 2	*[CGEXTEND2]*	0x0068

1.4.1.2. Low-speed Oscillation/power Control (Note1, Note2)

Register name		Address (Base+)
Low-speed Oscillation and Internal High-speed Oscillation 2 Clock Control Register	*[RLMLOSCCR]*	0x0000
Power Supply Cut Off Control Register	*[RLMSHTDNOP]*	0x0001
RLM Write Protection Register	*[RLMPROTECT]*	0x000F

Note1: Byte accessible registers. Bit band access cannot be performed.

Note2: When a register is rewritten, read the register to check rewriting.

In addition, when the reserved area is written, the initial value should be set.

1.4.2. Details of Register

1.4.2.1. *[CGPROTECT]* (CG Write Protection Register)

Bit	Bit symbol	After reset	Type	Function
31:8	-	0	R	Read as "0".
7:0	PROTECT[7:0]	0xC1	R/W	Control write protection for the CG registers (all registers except this register). 0xC1: Write protection for CG registers is disabled. Other than 0xC1: Write protection for CG registers is enabled.

1.4.2.2. *[CGOSCCR]* (Oscillation Control Register)

Bit	Bit symbol	After reset	Type	Function
31:17	-	0	R	Read as "0".
16	IHOSC1F	1	R	Indicate the stability flag of an internal oscillation for IHOSC1. (Note3) 0: Stopping or being in warming up 1: Stable oscillation
15:13	-	0	R	Read as "0".
12	-	0	R/W	Write as "0".
11:10	-	0	R	Read as "0".
9	OSCF	0	R	Indicate the selection status of a high-speed oscillator for fosc. 0: Internal high-speed oscillator 1 (IHOSC1) 1: External high-speed oscillator (EHOSC)
8	OSCSEL	0	R/W	Select a high-speed oscillation for fosc. (Note1) 0: Internal high-speed oscillator 1 (IHOSC1) 1: External high-speed oscillator (EHOSC)
7:4	-	0	R	Read as "0".
3	-	0	R/W	Write as "0".
2:1	EOSCEN[1:0]	00	R/W	Select the operation of the external high-speed oscillation. (Note2) 00: External oscillation is not used. 01: Use an external high-speed oscillator (EHOSC). 10: Use an external high-speed clock input (EHCLKIN). 11: Reserved
0	IHOSC1EN	1	R/W	Internal high-speed oscillator 1 (IHOSC1) 0: Stop 1: Oscillation

Note1: When the setting is modified, confirm whether the written value has been reflected to the ***[CGOSCCR]***<OSCF> bit before executing the next operation.

Note2: When using the oscillator connection, set "01" to these bits (use an external high-speed oscillator.).

Note3: To wait stabilizing oscillation of an internal high-speed oscillator 1 (IHOSC1), use a warming-up timer and confirm ***[CGWUPHCR]***<WUEF> instead of <IHOSCF1>.

1.4.2.3. *[CGSYSCR]* (System Clock Control Register)

Bit	Bit symbol	After reset	Type	Function
31:30	MCKSELPST[1:0]	00	R	Middle-speed prescaler clock (ΦT0m) selection status 00: <PRCK[3:0]> setting value (no division) 01: <PRCK[3:0]> setting value is divided by 2 Others: <PRCK[3:0]> setting value is divided by 4
29:28	-	0	R	Read as "0".
27:24	PRCKST[3:0]	0000	R	High-speed prescaler clock (ΦT0h) selection status 0000: fc 0100: fc / 16 1000: fc / 256 0001: fc / 2 0101: fc / 32 1001: fc / 512 0010: fc / 4 0110: fc / 64 0011: fc / 8 0111: fc / 128 Others: Reserved
23:22	MCKSELGST[1:0]	00	R	Middle-speed system clock (fsysm) selection status 00: <GEAR[2:0]> setting value (no division) 01: <GEAR[2:0]> setting value is divided by 2 Others: <GEAR[2:0]> setting value is divided by 4
21:19	-	0	R	Read as "0".
18:16	GEARST[2:0]	000	R	High-speed system clock (fsysh) gear selection status 000: fc 100: fc / 16 001: fc / 2 010: fc / 4 011: fc / 8 Others: Reserved
15:12	-	0	R	Read as "0".
11:8	PRCK[3:0]	0000	R/W	High-speed prescaler clock (ΦT0h) selection 0000: fc 0100: fc / 16 1000: fc / 256 0001: fc / 2 0101: fc / 32 1001: fc / 512 0010: fc / 4 0110: fc / 64 0011: fc / 8 0111: fc / 128 Others: Reserved Select a prescaler clock for the peripheral functions.
7:6	MCKSEL[1:0]	00	R/W	Middle-speed system clock (fsysm) and middle-speed prescaler clock (ΦT0m) selection 00: <GEAR[2:0]>, <PRCK[3:0]> setting values (no division) 01: <GEAR[2:0]>, <PRCK[3:0]> setting values are divided by 2. Others: <GEAR[2:0]>, <PRCK[3:0]> setting values are divided by 4. Maximum operating frequency of middle-speed system clock is 100 MHz.
5:3	-	0	R	Read as "0".
2:0	GEAR[2:0]	000	R/W	High-speed system clock (fsysh) gear selection 000: fc 100: fc / 16 001: fc / 2 010: fc / 4 011: fc / 8 Others: Reserved

1.4.2.4. *[CGSTBYCR]* (Standby Control Register)

Bit	Bit symbol	After reset	Type	Function
31:2	-	0	R	Read as "0".
1:0	STBY[1:0]	00	R/W	Select a low-power consumption mode. 00: IDLE 01: STOP1 10: STOP2 11: Reserved

1.4.2.5. *[CGPLL0SEL]* (PLL Selection Register for fsys)

Bit	Bit symbol	After reset	Type	Function
31:8	PLL0SET[23:0]	0x000000	R/W	PLL multiplication setup About a multiplication setup, refer to "1.2.5.2. Formula and Example of Setting of PLL Multiplication Value".
7:3	-	0	R	Read as "0".
2	PLL0ST	0	R	Indicate selection status of the clock for fsys. 0: fosc 1: f_{PLL}
1	PLL0SEL	0	R/W	Select clock selection for fsys 0: fosc 1: f_{PLL}
0	PLL0ON	0	R/W	Select PLL operation for fsys 0: Stop 1: Oscillation

1.4.2.6. *[CGWUPHCR]* (High-speed Oscillation Warming-up Register)

Bit	Bit symbol	After reset	Type	Function
31:20	WUPT[15:4]	0x800	R/W	Set the upper 12 bits of the 16 bits of calculation values of the warming-up timer. About a setup of a warming-up timer, refer to "1.2.4.1. Warming-up Timer for High-speed Oscillation".
19:16	WUPT[3:0]	0x0	R	Set the lower 4 bits of the 16 bits of calculation values of the warming-up timer. It is fixed to "0x0".
15:9	-	0	R	Read as "0".
8	WUCLK	0	R/W	Warming-up clock selection (Note1) 0: Internal high-speed oscillator 1 (IHOSC1) 1: External high-speed oscillator (EHOSC)
7:2	-	0	R	Read as "0".
1	WUEF	0	R	Indicate a status of the warming-up timer. (Note2) 0: The end of warming up 1: In warming-up operation
0	WUON	0	W	Control the warming-up timer. 0: Don't care 1: Warming-up operation starts.

Note1: Use the internal high-speed oscillator 1 (IHOSC1) for warming up when returning from STOP1 mode. Do not use an external high-speed oscillator (EHOSC).

Note2: Do not modify the registers during the warming up (<WUEF> = 1). Set the registers when <WUEF> = 0.

1.4.2.7. *[CGWUPLCR]* (Low-speed Oscillation Warming-up Register)

Bit	Bit symbol	After reset	Type	Function
31:27	-	0	R	Read as "0".
26:12	WUPTL[18:4]	0x4000	R/W	Set the upper 15 bits of 19 bits of calculation values of the warming-up timer. About a setup of a warming-up timer, refer to "1.2.4.2. Warming-up Timer for Low-speed Oscillation".
11:8	WUPTL[3:0]	0x0	R	Sets the lower 4 bits of the 19 bits of calculation values of the warming-up timer. It is fixed to "0x0".
7:2	-	0	R	Read as "0".
1	WULEF	0	R	Indicate a status of the warming-up timer (Note) 0: The end of warming up 1: In warming-up operation
0	WULON	0	W	Control the warming-up timer 0: Don't care 1: Warming-up operation starts.

Note: Do not modify the registers during the warming up (<WULEF> = 1). Set the registers when <WULEF> = 0.

1.4.2.8. *[CGFSYSMENC]* (Middle-speed Clock Supply and Stop Register C for fsysm)

Bit	Bit symbol	After reset	Type	Function
31:17	-	0	R	Read as "0".
16	IPMENC16	0	R/W	Clock enable of T32A ch15 0: Clock stop 1: Clock supply
15	IPMENC15	0	R/W	Clock enable of T32A ch14 0: Clock stop 1: Clock supply
14:10	-	00000	R/W	Write as "00000"
9	IPMENC09	0	R/W	Clock enable of EI2C ch4 0: Clock stop 1: Clock supply
8	IPMENC08	0	R/W	Clock enable of EI2C ch3 0: Clock stop 1: Clock supply
7	IPMENC07	0	R/W	Clock enable of EI2C ch2 0: Clock stop 1: Clock supply
6	IPMENC06	0	R/W	Clock enable of EI2C ch1 0: Clock stop 1: Clock supply
5	IPMENC05	0	R/W	Clock enable of EI2C ch0 0: Clock stop 1: Clock supply
4	IPMENC04	0	R/W	Clock enable of TSSI ch1 0: Clock stop 1: Clock supply
3	IPMENC03	0	R/W	Clock enable of TSSI ch0 0: Clock stop 1: Clock supply
2	IPMENC02	0	R/W	Clock enable of FIR 0: Clock stop 1: Clock supply
1	IPMENC01	0	R/W	Clock enable of I2S ch1 0: Clock stop 1: Clock supply
0	IPMENC00	0	R/W	Clock enable of I2S ch0 0: Clock stop 1: Clock supply

Note1: Even if the initial value of the register is set to stop of the clock, the clock is supplied during the reset.

Note2: Write "0" for bit of function that does not exist in TMPM4GQ and TMPM4GN. For detail, refer to "1.5. Information for Each Product".

1.4.2.9. *[CGFSYSMENA]* (Middle-speed Clock Supply and Stop Register A for fsysm)

Bit	Bit symbol	After reset	Type	Function
31	IPMENA31	0	R/W	Clock enable of I2C ch2 0: Clock stop 1: Clock supply
30	IPMENA30	0	R/W	Clock enable of I2C ch1 0: Clock stop 1: Clock supply
29	IPMENA29	0	R/W	Clock enable of I2C ch0 0: Clock stop 1: Clock supply
28	IPMENA28	0	R/W	Clock enable of UART ch5 0: Clock stop 1: Clock supply
27	IPMENA27	0	R/W	Clock enable of UART ch4 0: Clock stop 1: Clock supply
26	IPMENA26	0	R/W	Clock enable of UART ch3 0: Clock stop 1: Clock supply
25	IPMENA25	0	R/W	Clock enable of UART ch2 0: Clock stop 1: Clock supply
24	IPMENA24	0	R/W	Clock enable of UART ch1 0: Clock stop 1: Clock supply
23	IPMENA23	1	R/W	Clock enable of UART ch0 0: Clock stop 1: Clock supply
22	IPMENA22	0	R/W	Clock enable of TSPI ch8 0: Clock stop 1: Clock supply
21	IPMENA21	0	R/W	Clock enable of TSPI ch7 0: Clock stop 1: Clock supply
20	IPMENA20	0	R/W	Clock enable of TSPI ch6 0: Clock stop 1: Clock supply
19	IPMENA19	0	R/W	Clock enable of T32A ch13 0: Clock stop 1: Clock supply
18	IPMENA18	0	R/W	Clock enable of T32A ch12 0: Clock stop 1: Clock supply
17	IPMENA17	0	R/W	Clock enable of T32A ch11 0: Clock stop 1: Clock supply
16	IPMENA16	0	R/W	Clock enable of T32A ch10 0: Clock stop 1: Clock supply
15	IPMENA15	0	R/W	Clock enable of T32A ch09 0: Clock stop 1: Clock supply
14	IPMENA14	0	R/W	Clock enable of T32A ch08 0: Clock stop 1: Clock supply
13	IPMENA13	0	R/W	Clock enable of T32A ch07 0: Clock stop 1: Clock supply
12	IPMENA12	0	R/W	Clock enable of T32A ch06 0: Clock stop 1: Clock supply

Bit	Bit symbol	After reset	Type	Function
11	IPMENA11	0	R/W	Clock enable of T32A ch05 0: Clock stop 1: Clock supply
10	IPMENA10	0	R/W	Clock enable of T32A ch04 0: Clock stop 1: Clock supply
9	IPMENA09	0	R/W	Clock enable of T32A ch03 0: Clock stop 1: Clock supply
8	IPMENA08	0	R/W	Clock enable of T32A ch02 0: Clock stop 1: Clock supply
7	IPMENA07	0	R/W	Clock enable of T32A ch01 0: Clock stop 1: Clock supply
6	IPMENA06	1	R/W	Clock enable of T32A ch00 0: Clock stop 1: Clock supply
5	IPMENA05	0	R/W	Clock enable of DAC ch1 0: Clock stop 1: Clock supply
4	IPMENA04	0	R/W	Clock enable of DAC ch0 0: Clock stop 1: Clock supply
3	IPMENA03	0	R/W	Clock enable of ADC Unit A 0: Clock stop 1: Clock supply
2	IPMENA02	0	R/W	Clock enable of FUART ch1 0: Clock stop 1: Clock supply
1	IPMENA01	0	R/W	Clock enable of FUART ch0 0: Clock stop 1: Clock supply
0	IPMENA00	0	R/W	Clock enable of MDMAC unit A 0: Clock stop 1: Clock supply

Note1: Even if the initial value of the register is set to stop of the clock, the clock is supplied during the reset.

Note2: Write "0" for bit of function that does not exist in TMPM4GQ and TMPM4GN. For detail, refer to "1.5. Information for Each Product".

1.4.2.10. *[CGFSYSMENB]* (Middle-speed Clock Supply and Stop Register B for fsysm)

Bit	Bit symbol	After reset	Type	Function
31	IPMENB31	1	R/W	Clock enable of SIWDT 0: Clock stop 1: Clock supply
30	IPMENB30	1	R/W	Clock enable of NBDIF 0: Clock stop 1: Clock supply
29	IPMENB29	1	R/W	Write as "1"
28	IPMENB28	0	R/W	Clock enable of TRGSEL 0: Clock stop 1: Clock supply
27:25	-	0	R	Read as "0"
24	IPMENB24	0	R/W	Clock enable of A-PMD 0: Clock stop 1: Clock supply
23	IPMENB23	0	R/W	Clock enable of OFD 0: Clock stop 1: Clock supply
22	IPMENB22	0	R/W	Clock enable of TRM 0: Clock stop 1: Clock supply
21	IPMENB21	0	R/W	Clock enable of PORT Y 0: Clock stop 1: Clock supply
20	IPMENB20	0	R/W	Clock enable of PORT W 0: Clock stop 1: Clock supply
19	IPMENB19	0	R/W	Clock enable of PORT V 0: Clock stop 1: Clock supply
18	IPMENB18	0	R/W	Clock enable of PORT U 0: Clock stop 1: Clock supply
17	IPMENB17	0	R/W	Clock enable of PORT T 0: Clock stop 1: Clock supply
16	IPMENB16	0	R/W	Clock enable of PORT R 0: Clock stop 1: Clock supply
15	IPMENB15	0	R/W	Clock enable of PORT P 0: Clock stop 1: Clock supply
14	IPMENB14	0	R/W	Clock enable of PORT N 0: Clock stop 1: Clock supply
13	IPMENB13	0	R/W	Clock enable of PORT M 0: Clock stop 1: Clock supply
12	IPMENB12	0	R/W	Clock enable of PORT L 0: Clock stop 1: Clock supply
11	IPMENB11	0	R/W	Clock enable of PORT K 0: Clock stop 1: Clock supply
10	IPMENB10	0	R/W	Clock enable of PORT J 0: Clock stop 1: Clock supply
9	IPMENB09	1	R/W	Clock enable of PORT H 0: Clock stop 1: Clock supply

Bit	Bit symbol	After reset	Type	Function
8	IPMENB08	0	R/W	Clock enable of PORT G 0: Clock stop 1: Clock supply
7	IPMENB07	0	R/W	Clock enable of PORT F 0: Clock stop 1: Clock supply
6	IPMENB06	0	R/W	Clock enable of PORT E 0: Clock stop 1: Clock supply
5	IPMENB05	0	R/W	Clock enable of PORT D 0: Clock stop 1: Clock supply
4	IPMENB04	0	R/W	Clock enable of PORT C 0: Clock stop 1: Clock supply
3	IPMENB03	0	R/W	Clock enable of PORT B 0: Clock stop 1: Clock supply
2	IPMENB02	0	R/W	Clock enable of PORT A 0: Clock stop 1: Clock supply
1	IPMENB01	0	R/W	Clock enable of I2C ch4 0: Clock stop 1: Clock supply
0	IPMENB00	0	R/W	Clock enable of I2C ch3 0: Clock stop 1: Clock supply

Note1: Even if the initial value of the register is set to stop of the clock, the clock is supplied during the reset.

Note2: Write "0" for bit of function that does not exist in TMPM4GQ and TMPM4GN. For detail, refer to "1.5. Information for Each Product".

1.4.2.11. *[CGFSYSENA]* (High-speed Clock Supply and Stop Register A for fsysh)

Bit	Bit symbol	After reset	Type	Function
31:10	-	0	R	Read as "0".
9	IPENA09	0	R/W	Clock enable of TSPI ch5 0: Clock stop 1: Clock supply
8	IPENA08	0	R/W	Clock enable of TSPI ch4 0: Clock stop 1: Clock supply
7	IPENA07	0	R/W	Clock enable of TSPI ch3 0: Clock stop 1: Clock supply
6	IPENA06	0	R/W	Clock enable of TSPI ch2 0: Clock stop 1: Clock supply
5	IPENA05	0	R/W	Clock enable of TSPI ch1 0: Clock stop 1: Clock supply
4	IPENA04	0	R/W	Clock enable of TSPI ch0 0: Clock stop 1: Clock supply
3	IPENA03	0	R/W	Clock enable of EBIF 0: Clock stop 1: Clock supply
2	IPENA02	0	R/W	Clock enable of SMIF ch0 0: Clock stop 1: Clock supply
1	IPENA01	0	R/W	Clock enable of HDMAC unit B 0: Clock stop 1: Clock supply
0	IPENA00	0	R/W	Clock enable of HDMAC unit A 0: Clock stop 1: Clock supply

Note1: Even if the initial value of the register is set to stop of the clock, the clock is supplied during the reset.

Note2: Write "0" for bit of function that does not exist in TMPM4GQ and TMPM4GN. For detail, refer to "1.5. Information for Each Product".

1.4.2.12. *[CGFCEN]* (Clock Supply and Stop Register for fc)

Bit	Bit symbol	After reset	Type	Function
31:28	-	0	R	Read as "0"
27	FCIPEN27	0	R/W	Clock enable of DNF unit B 0: Clock stop 1: Clock supply
26	FCIPEN26	0	R/W	Clock enable of DNF unit A 0: Clock stop 1: Clock supply
25:24	-	0	R	Read as "0"
23	FCIPEN23	0	R/W	Clock enable of OFD (Note1) 0: Clock stop 1: Clock supply
22:0	-	0	R	Read as "0"

Note1: When use the monitor clock of fc, ***[CGFSYSMENB]***<IPMENB23> and ***[CGFCEN]***<FCIPEN23> should be enabled.

Note2: Even if the initial value of the register is set to stop of the clock, the clock is supplied during the reset.

Note3: Write "0" for bit of function that does not exist in TMPM4GQ and TMPM4GN. For detail, refer to "1.5. Information for Each Product".

1.4.2.13. *[CGSPCLKEN]* (Clock Supply for ADC and Debug Circuit Register)

Bit	Bit symbol	After reset	Type	Function
31:17	-	0	R	Read as "0".
16	ADCKEN	0	R/W	Clock enable of ADC. 0: Clock stop 1: Clock supply
15:1	-	0	R	Read as "0".
0	TRCKEN	0	R/W	Clock enable of the trace function of debug circuit (TRACE and SWV). 0: Clock stop 1: Clock supply

Note1: Even if the initial value of the register is set to stop of the clock, the clock is supplied during the reset.

Note2: When setting this bit to "0" (clock stop), please make sure that AD conversion is stopped.

1.4.2.14. *[CGEXTEND2]* (Function Extension Register 2)

Bit	Bit symbol	After reset	Type	Function
31:3	-	0	R	Read as "0".
2	RSV22	0	R/W	MDMAC software reset It is generated with the continuous writes of "0", "1" and "0" in order. When this bit is written continuously in the order of "0", "1" and "0", MDMAC software reset is generated. After "1" is set, 4 cycles of middle-speed system clock (fsysm) or more should elapse before "0" is set.
1	RSV21	0	R/W	MDMAC descriptor error clear (Note) It is generated with the continuous writes of "0", "1" and "0" in order. MDMAC descriptor error is cleared by the sequential writes of "0", "1" and "0" in order. After "1" is set, 4 cycles of middle-speed system clock (fsysm) or more should elapse before "0" is set.
0	RSV20	0	R/W	MDMAC bus error clear (Note) It is generated with the continuous writes of "0", "1" and "0" in order. MDMAC bus error is cleared by the sequential writes of "0", "1" and "0" in order. After "1" is set, 4 cycles of middle-speed system clock (fsysm) or more should elapse before "0" is set.

Note: When an error flag should be cleared, it is necessary to assert the software reset <RSV22>, too.

1.4.2.15. *[RLMLOSCCR]* (Low-speed Oscillation and Internal High-speed Oscillation 2 Clock Control Register)

Bit	Bit symbol	After reset	Type	Function
7:6	-	0	R	Read as "0".
5	POSCF	0	R	Indicate the stability flag of internal oscillation for IHOSC2. 0: Stopping or being in warming up 1: Stable oscillation
4	POSCEN	0	R/W	Internal high-speed oscillator 2 (IHOSC2) (Note3), (Note5) 0: Stop 1: Oscillation
3	-	0	R	Read as "0".
2	DRCOSCL	0	R/W	Selection of a low-speed clock. 0: External low-speed clock input (ELCLKIN) 1: External low-speed oscillator (ELOSC)
1	-	0	R/W	Write as "0"
0	XTEN	0	R/W	Selection of using a low-speed clock (Note4) 0: Not used 1: Used

Note1: It is initialized only by a power-on reset.

Note2: It is a register accessed per byte. Bit band access is not allowed.

Note3: After changing the setting, make sure that ***[RLMLOSCCR]***<POSCF> becomes "1" and then perform the next operation.

Note4: When <XTEN> is rewritten, read it to confirm rewriting result.

Note5: Even if <POSCEN> is write enabled by ***[RLMPROTECT]***, it cannot be written when ***[SIWDxOSCCR]*** <OSCPRO> = 1.

1.4.2.16. *[RLMSHTDNOP]* (Power Supply Cut Off Control Register)

Bit	Bit symbol	After reset	Type	Function
7	-	0	R/W	Write "0".
6:1	-	0	R	Read as "0".
0	PTKEEP	0	R/W	The I/O control signal in the STOP2 mode is held. 0: Control by Port. 1: Hold the state when it changes into "1" from "0". It is necessary to set this bit prior to the transition to STOP2 mode.

Note1: It is a register accessed per byte. Bit band access is not allowed.

Note2: When <PTKEEP> is rewritten, read it to confirm rewriting result.

1.4.2.17. *[RLMPROTECT]* (RLM Write Protection Register)

Bit	Bit symbol	After reset	Type	Function
7:0	PROTECT[7:0]	0xC1	R/W	Control write protection for RLM registers (all registers except this register). 0xC1: Write protection for RLM registers is disabled. Other than 0xC1: Write protection for RLM registers is enabled.

Note1: It is a register accessed per byte. Bit band access is not allowed.

Note2: When <PROTECT[7:0]> is rewritten, read it to confirm rewriting result.

1.5. Information for Each Product

The information about ***[CGFSYSENA]***, ***[CGFSYSMENA]***, ***[CGFSYSMENB]***, ***[CGFSYSMENC]*** and ***[CGFCEN]*** which are different according to each product is shown below.

1.5.1. *[CGFSYSENA]*

Table 1.13 Allocation of *[CGFSYSENA]* by Each Product

Bit	Bit symbol	Destination	Channel number/ unit name/ port name	M4GR	M4GQ	M4GN
31	IPENA31	-	-	-	-	-
30	IPENA30	-	-	-	-	-
29	IPENA29	-	-	-	-	-
28	IPENA28	-	-	-	-	-
27	IPENA27	-	-	-	-	-
26	IPENA26	-	-	-	-	-
25	IPENA25	-	-	-	-	-
24	IPENA24	-	-	-	-	-
23	IPENA23	-	-	-	-	-
22	IPENA22	-	-	-	-	-
21	IPENA21	-	-	-	-	-
20	IPENA20	-	-	-	-	-
19	IPENA19	-	-	-	-	-
18	IPENA18	-	-	-	-	-
17	IPENA17	-	-	-	-	-
16	IPENA16	-	-	-	-	-
15	IPENA15	-	-	-	-	-
14	IPENA14	-	-	-	-	-
13	IPENA13	-	-	-	-	-
12	IPENA12	-	-	-	-	-
11	IPENA11	-	-	-	-	-
10	IPENA10	-	-	-	-	-
9	IPENA09	TSPI	5	✓	✓	-
8	IPENA08		4	✓	✓	✓
7	IPENA07		3	✓	✓	✓
6	IPENA06		2	✓	✓	✓
5	IPENA05		1	✓	✓	✓
4	IPENA04		0	✓	✓	✓
3	IPENA03	EBIF	-	✓	✓	✓
2	IPENA02	SMIF	0	✓	✓	✓
1	IPENA01	HDMAC	B	✓	✓	✓
0	IPENA00		A	✓	✓	✓

✓: Available, -: Not available

1.5.2. *[CGFSYSMENA]*

Table 1.14 Allocation of *[CGFSYSMENA]* by Each Product

Bit	Bit symbol	Destination	Channel number/ unit name/ port name	M4GR	M4GQ	M4GN
31	IPMENA31	I2C	2	✓	✓	✓
30	IPMENA30		1	✓	✓	✓
29	IPMENA29		0	✓	✓	✓
28	IPMENA28	UART	5	✓	-	-
27	IPMENA27		4	✓	✓	-
26	IPMENA26		3	✓	✓	-
25	IPMENA25		2	✓	✓	✓
24	IPMENA24		1	✓	✓	✓
23	IPMENA23		0	✓	✓	✓
22	IPMENA22	TSPI	8	✓	-	-
21	IPMENA21		7	✓	✓	-
20	IPMENA20		6	✓	✓	-
19	IPMENA19	T32A	13	✓	✓	✓
18	IPMENA18		12	✓	✓	✓
17	IPMENA17		11	✓	✓	✓
16	IPMENA16		10	✓	✓	✓
15	IPMENA15		9	✓	✓	✓
14	IPMENA14		8	✓	✓	✓
13	IPMENA13		7	✓	✓	✓
12	IPMENA12		6	✓	✓	✓
11	IPMENA11		5	✓	✓	✓
10	IPMENA10		4	✓	✓	✓
9	IPMENA09		3	✓	✓	✓
8	IPMENA08		2	✓	✓	✓
7	IPMENA07		1	✓	✓	✓
6	IPMENA06		0	✓	✓	✓
5	IPMENA05	DAC	1	✓	✓	✓
4	IPMENA04		0	✓	✓	✓
3	IPMENA03	ADC	A	✓	✓	✓
2	IPMENA02	FUART	1	✓	✓	-
1	IPMENA01		0	✓	✓	✓
0	IPMENA00	MDMAC	A	✓	✓	✓

✓: Available, -: Not available

1.5.3. *[CGFSYSENB]*

Table 1.15 Allocation of *[CGFSYSMENB]* by Each Product

Bit	Bit symbol	Destination	Channel number/ unit name/ port name	M4GR	M4GQ	M4GN
31	IPMENB31	SIWDT	0	✓	✓	✓
30	IPMENB30	NBDIF	-	✓	✓	✓
29	IPMENB29	- (Note)	-	-	-	-
28	IPMENB28	TRGSEL	0	✓	✓	✓
27	IPMENB27	-	-	-	-	-
26	IPMENB26	-	-	-	-	-
25	IPMENB25	-	-	-	-	-
24	IPMENB24	A-PMD	0	✓	✓	✓
23	IPMENB23	OFD	-	✓	✓	✓
22	IPMENB22	TRM	-	✓	✓	✓
21	IPMENB21	PORT	Y	✓	✓	✓
20	IPMENB20		W	✓	-	-
19	IPMENB19		V	✓	✓	-
18	IPMENB18		U	✓	-	-
17	IPMENB17		T	✓	✓	✓
16	IPMENB16		R	✓	✓	-
15	IPMENB15		P	✓	✓	✓
14	IPMENB14		N	✓	✓	✓
13	IPMENB13		M	✓	✓	-
12	IPMENB12		L	✓	✓	✓
11	IPMENB11		K	✓	✓	✓
10	IPMENB10		J	✓	-	-
9	IPMENB09		H	✓	✓	✓
8	IPMENB08		G	✓	✓	✓
7	IPMENB07		F	✓	✓	✓
6	IPMENB06		E	✓	✓	✓
5	IPMENB05		D	✓	✓	✓
4	IPMENB04		C	✓	✓	-
3	IPMENB03		B	✓	✓	✓
2	IPMENB02		A	✓	✓	✓
1	IPMENB01	I2C	4	✓	✓	-
0	IPMENB00		3	✓	✓	-

✓: Available, -: Not available

Note: Write as "1" (Clock supply).

1.5.4. *[CGFSYSENC]*

Table 1.16 Allocation of *[CGFSYSMENC]* by Each Product

Bit	Bit symbol	Destination	Channel number/ unit name/ port name	M4GR	M4GQ	M4GN
31	IPMENC31	-	-	-	-	-
30	IPMENC30	-	-	-	-	-
29	IPMENC29	-	-	-	-	-
28	IPMENC28	-	-	-	-	-
27	IPMENC27	-	-	-	-	-
26	IPMENC26	-	-	-	-	-
25	IPMENC25	-	-	-	-	-
24	IPMENC24	-	-	-	-	-
23	IPMENC23	-	-	-	-	-
22	IPMENC22	-	-	-	-	-
21	IPMENC21	-	-	-	-	-
20	IPMENC20	-	-	-	-	-
19	IPMENC19	-	-	-	-	-
18	IPMENC18	-	-	-	-	-
17	IPMENC17	-	-	-	-	-
16	IPMENC16	T32A	15	✓	✓	✓
15	IPMENC15		14	✓	✓	✓
14	IPMENC14	-	-	-	-	-
13	IPMENC13	-	-	-	-	-
12	IPMENC12	-	-	-	-	-
11	IPMENC11	-	-	-	-	-
10	IPMENC10	-	-	-	-	-
9	IPMENC09	EI2C	4	✓	✓	-
8	IPMENC08		3	✓	✓	-
7	IPMENC07		2	✓	✓	✓
6	IPMENC06		1	✓	✓	✓
5	IPMENC05		0	✓	✓	✓
4	IPMENC04	TSSI	1	✓	-	-
3	IPMENC03		0	✓	✓	✓
2	IPMENC02	FIR	0	✓	✓	✓
1	IPMENC01	I2S	1	✓	✓	✓
0	IPMENC00		0	✓	✓	✓

✓: Available, -: Not available

1.5.5. *[CGFCEN]*

Table 1.17 Allocation of *[CGFCEN]* by Each Product

Bit	Bit symbol	Destination	Channel number/ unit name/ port name	M4GR	M4GQ	M4GN
31	FCIPEN31	-	-	-	-	-
30	FCIPEN30	-	-	-	-	-
29	FCIPEN29	-	-	-	-	-
28	FCIPEN28	-	-	-	-	-
27	FCIPEN27	DNF	B	✓	✓	✓
26	FCIPEN26		A	✓	✓	✓
25	FCIPEN25	-	-	-	-	-
24	FCIPEN24	-	-	-	-	-
23	FCIPEN23	OFD	-	✓	✓	✓
22	FCIPEN22	-	-	-	-	-
21	FCIPEN21	-	-	-	-	-
20	FCIPEN20	-	-	-	-	-
19	FCIPEN19	-	-	-	-	-
18	FCIPEN18	-	-	-	-	-
17	FCIPEN17	-	-	-	-	-
16	FCIPEN16	-	-	-	-	-
15	FCIPEN15	-	-	-	-	-
14	FCIPEN14	-	-	-	-	-
13	FCIPEN13	-	-	-	-	-
12	FCIPEN12	-	-	-	-	-
11	FCIPEN11	-	-	-	-	-
10	FCIPEN10	-	-	-	-	-
9	FCIPEN09	-	-	-	-	-
8	FCIPEN08	-	-	-	-	-
7	FCIPEN07	-	-	-	-	-
6	FCIPEN06	-	-	-	-	-
5	FCIPEN05	-	-	-	-	-
4	FCIPEN04	-	-	-	-	-
3	FCIPEN03	-	-	-	-	-
2	FCIPEN02	-	-	-	-	-
1	FCIPEN01	-	-	-	-	-
0	FCIPEN00	-	-	-	-	-

✓: Available, -: Not available

2. Memory Map

2.1. Outline

The memory maps for TMPM4G Group (1) are based on the Cortex-M4 (with FPU) processor core memory map.

The internal ROM, internal RAM, and special function registers (SFR) of TMPM4G Group (1) are mapped to the Code, SRAM, and peripheral regions of the Cortex-M4 (with FPU) respectively. The special function register (SFR) means the control registers of all input/output ports and peripheral functions.

The CPU register region is the processor core's internal register region.

For more information on each region, see the "Arm Cortex-M4 Processor Technical Reference Manual".

Note that access to regions indicated as "Fault" causes a bus fault if bus faults are enabled, or causes a hard fault if bus faults are disabled. Also, do not access the vendor-specific region.

2.1.1. TMPM4GxF20

- Code Flash: 2048KB
- RAM: 256KB+2KB (Backup RAM)
- Data Flash: 32KB
- Target products: TMPM4GRF20FG, TMPM4GRF20XBG, TMPM4GQF20FG, TMPM4GQF20XBG, TMPM4GNF20FG

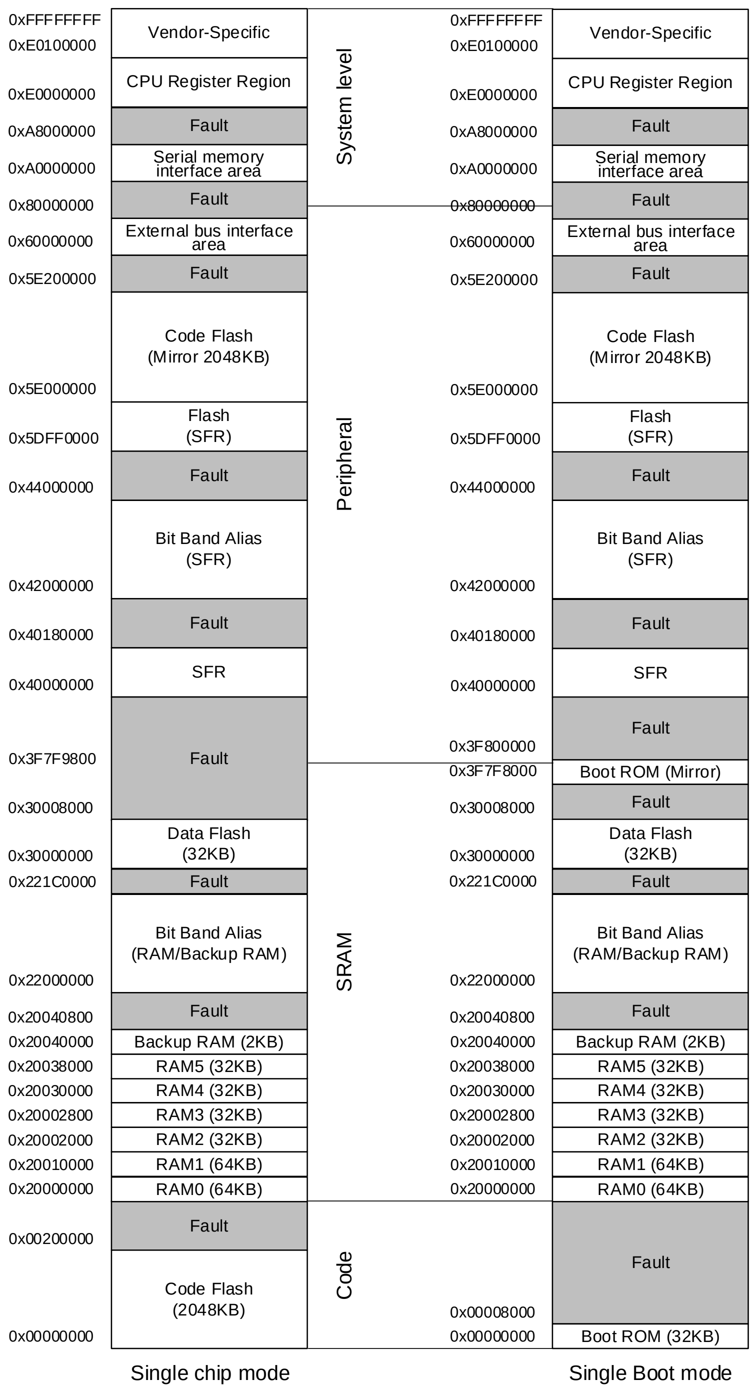


Figure 2.1 TMPM4GxF20

2.1.2. TMPM4GxF15

- Code Flash: 1536KB
- RAM: 256KB+2KB (Backup RAM)
- Data Flash: 32KB
- Target products: TMPM4GRF15FG, TMPM4GRF15XBG, TMPM4GQF15FG, TMPM4GQF15XBG, TMPM4GNF15FG

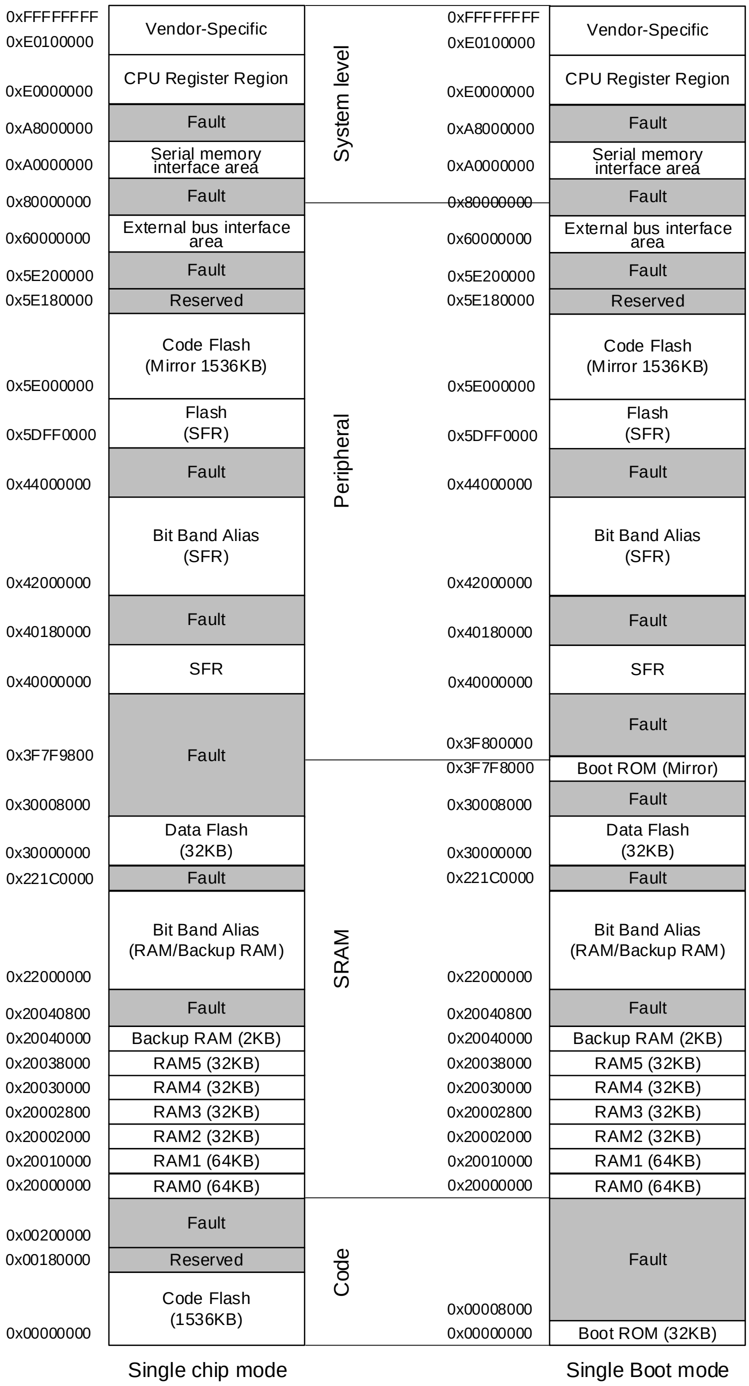


Figure 2.2 TMPM4GxF15

2.1.3. TMPM4GxF10

- Code Flash: 1024KB
- RAM: 256KB+2KB (Backup RAM)
- Data Flash: 32KB
- Target products: TMPM4GRF10FG, TMPM4GRF10XBG, TMPM4GQF10FG, TMPM4GQF10XBG, TMPM4GNF10FG

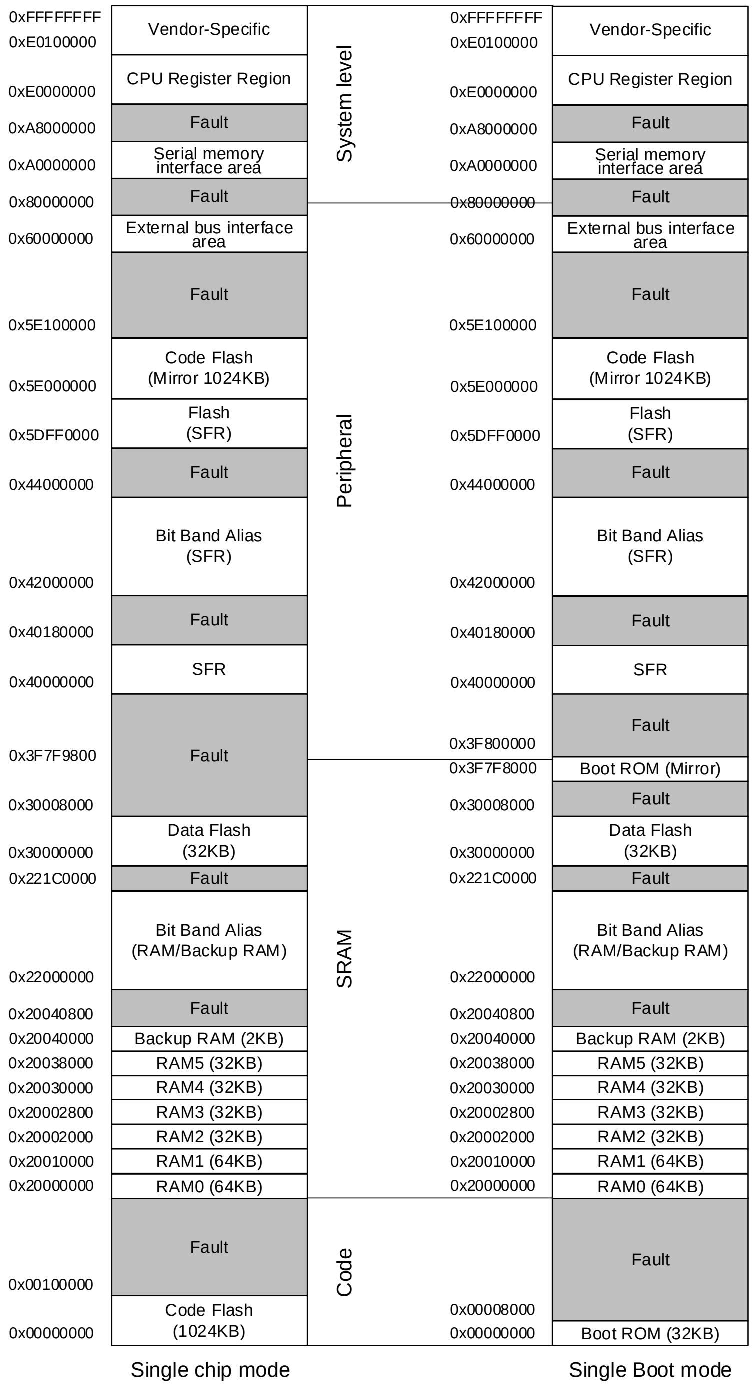


Figure 2.3 TMPM4GxF10

2.1.4. TMPM4GxFD

- Code Flash: 512KB
- RAM: 192KB+2KB (Backup RAM)
- Data Flash: 32KB
- Target products: MPM4GRFDFG, TMPM4GRFDXBG, TMPM4GQFDFG, TMPM4GQFDXBG, TMPM4GNFDFG

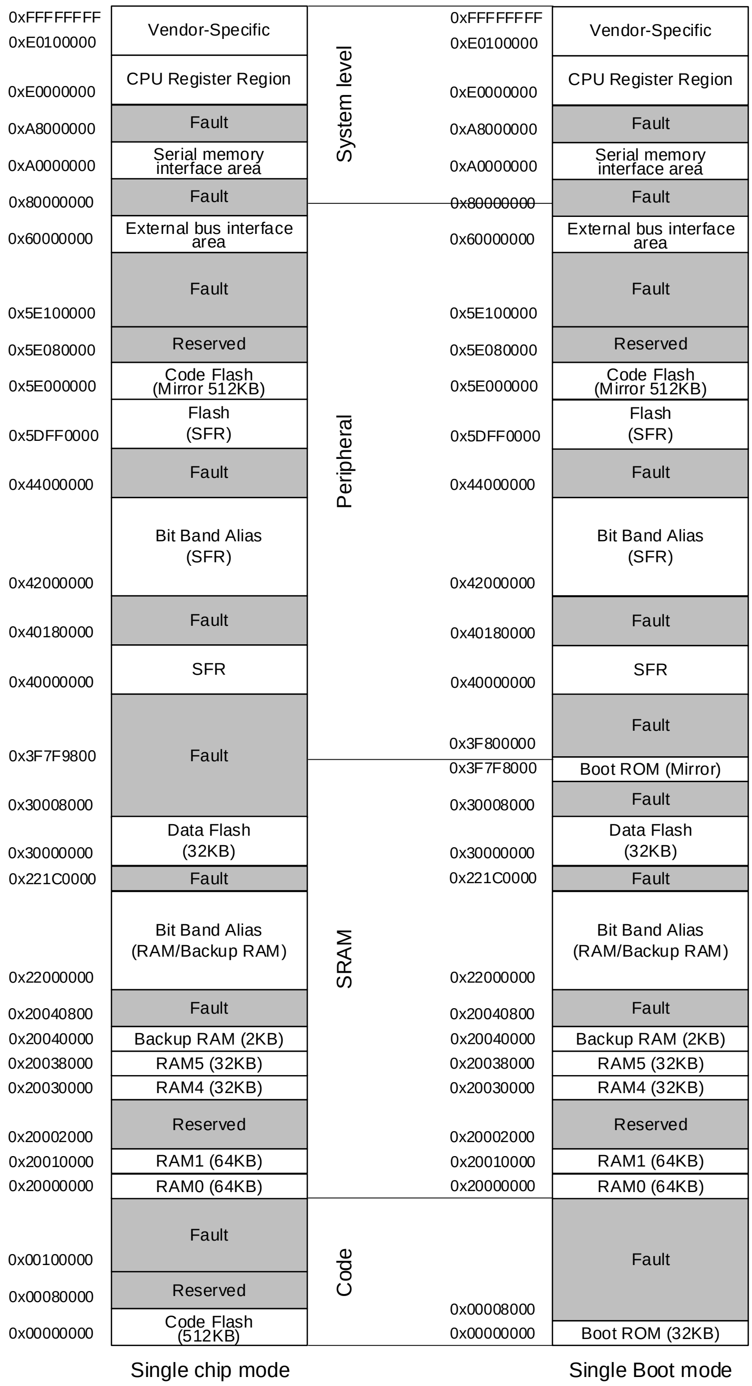


Figure 2.4 TMPM4GxFD

2.2. Bus Matrix

TMPM4G Group (1) have the main masters consisted of the CPU core and high-speed DMA controllers (HDMAC) and sub master consisted of a multi-function DMA controller (MDMAC) and NBDIF.

The main masters are connected to the slave ports (S1 to S5) of the bus matrix. They are connected to the peripheral functions and middle-speed clock domain via master ports (M0 to M15) through the symbol "○" and "●" which mean the connection in a bus matrix.

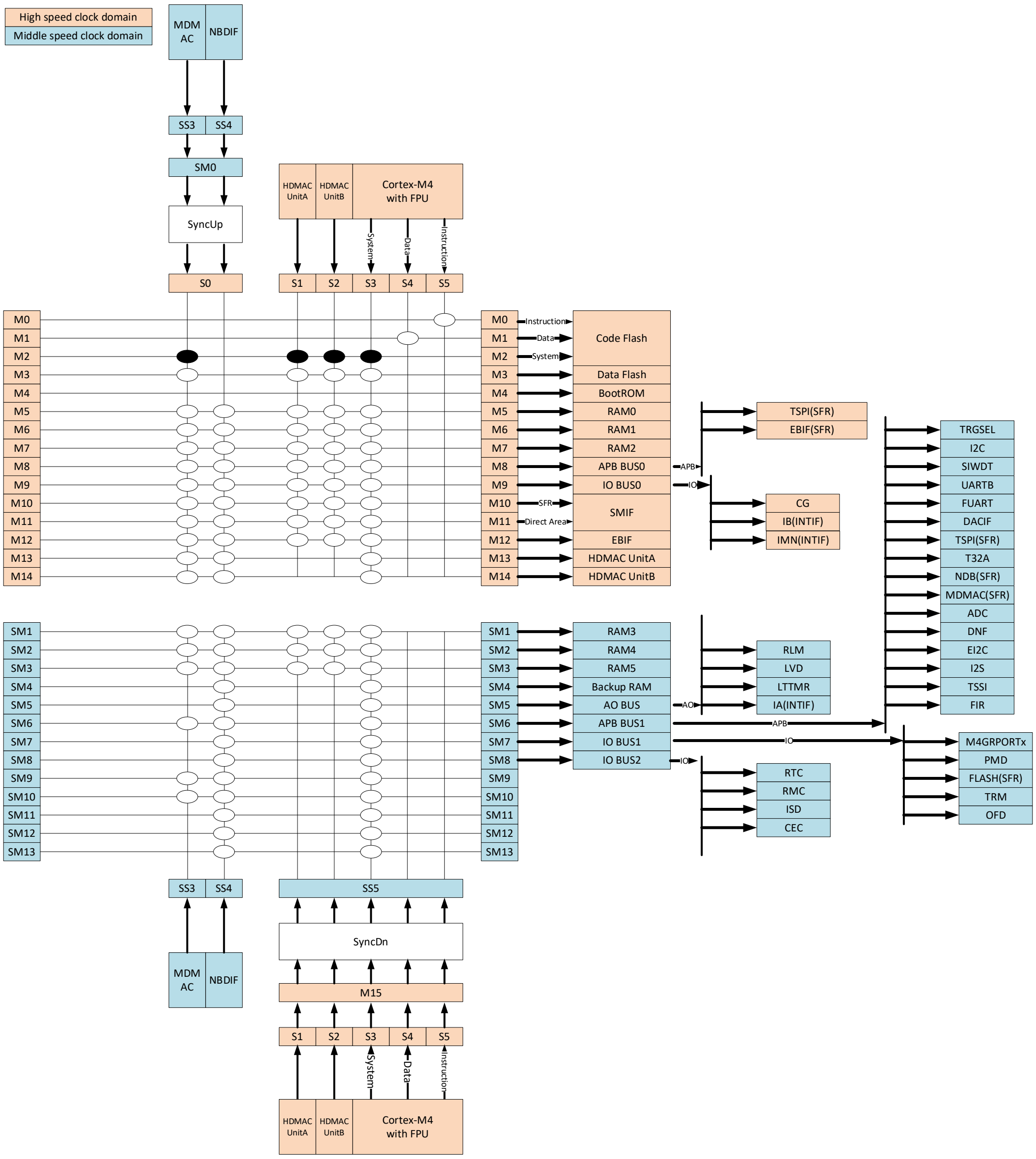
The sub masters are connected to the slave ports (SS3 and SS4) of the bus matrix. They are connected to the peripheral functions and high-speed clock domain via master ports (SM0 to SM8) through the symbol "○" and "●" which mean the connection in a bus matrix.

"●" shows a connection to a mirror area.

When multiple slaves are connected to the same master line in the bus matrix and multiple slaves are accessed at the same time, the access to the slave from the master with the smallest slave number is prioritized.

2.2.1. Configuration

2.2.1.1. Single Chip Mode

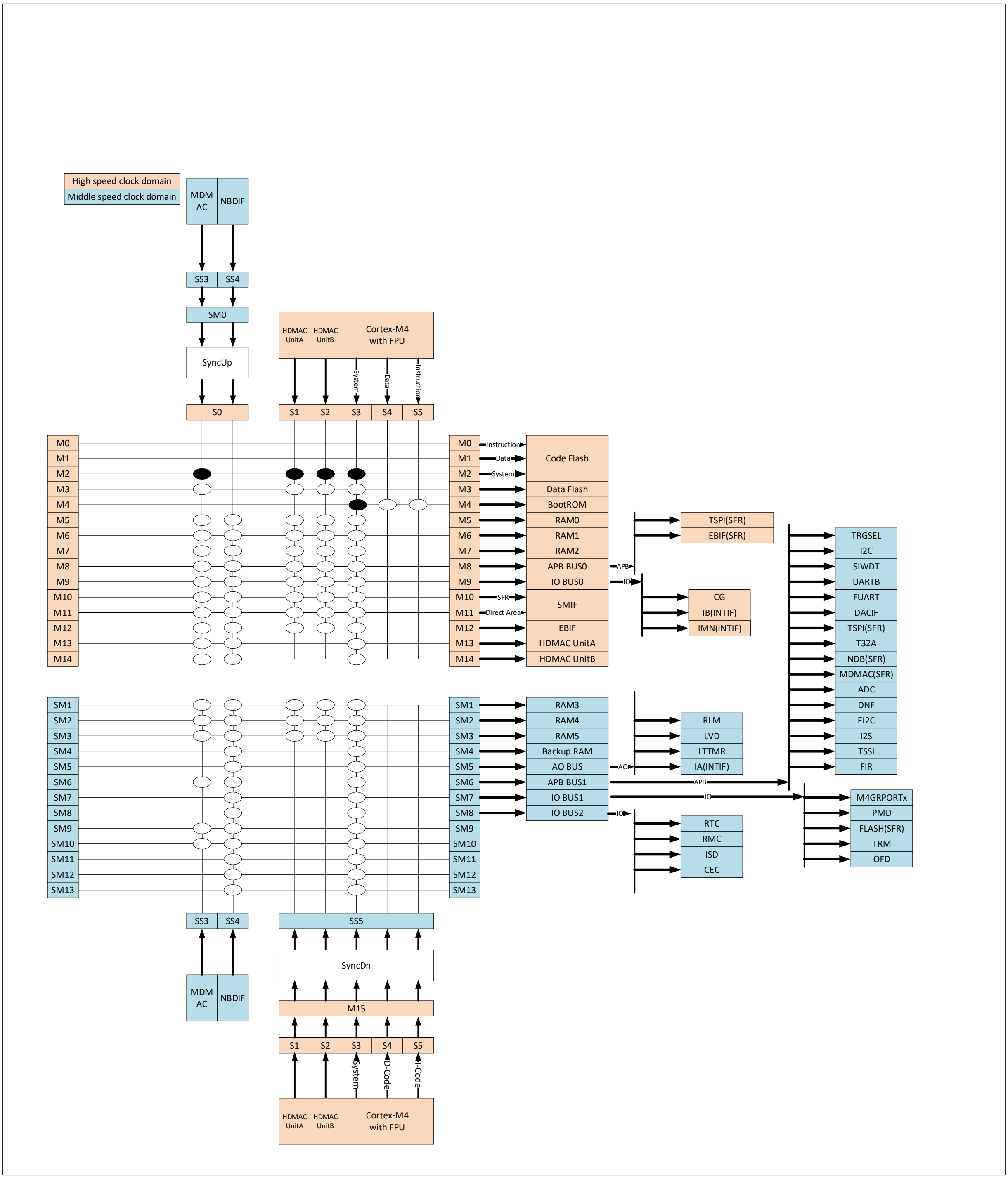


Note1: NBDIF is not connected to M2, M3.

Note2: Access between the high-speed domain and the middle-speed domain requires synchronization time between domains.

Figure 2.5 Single Chip Mode

2.2.1.2. Single Boot Mode



Note1: NBDIF is not connected to M2, M3.

Note2: Access between the high-speed domain and the middle-speed domain requires synchronization time between domains.

Figure 2.6 Single Boot Mode

2.2.2. Connection Table

2.2.2.1. Code Area/SRAM Area/SMIF Area/External Bus Area

(1) TMPM4GxF20

● Single chip mode

Table 2.1 TMPM4GxF20 Single Chip Mode

Start address	Slave		Sub master		Main master				
			MDMAC unit A	NBDIF	HDMAC unit A	HDMAC unit B	Core S-Bus	Core D-Bus	Core I-Bus
			SS3	SS4	S1	S2	S3	S4	S5
0x00000000	Code Flash	M0	Fault	Fault	Fault	Fault	-	Fault	✓
		M1	Fault	Fault	Fault	Fault	-	✓	Fault
0x00200000	Fault	-	Fault	Fault	Fault	Fault	-	-	-
0x20000000	RAM0	M5	✓	✓	✓	✓	✓	-	-
0x20010000	RAM1	M6	✓	✓	✓	✓	✓	-	-
0x20020000	RAM2	M7	✓	✓	✓	✓	✓	-	-
0x20028000	RAM3	SM1	✓	✓	Fault	Fault	✓	-	-
0x20030000	RAM4	SM2	✓	✓	Fault	Fault	✓	-	-
0x20038000	RAM5	SM3	✓	✓	Fault	Fault	✓	-	-
0x20040000	Backup RAM	SM4	Fault	✓	Fault	Fault	✓	-	-
0x20040800	Fault	-	Fault	Fault	Fault	Fault	Fault	-	-
0x22000000	Bit band alias	-	✓	✓	✓	✓	✓	-	-
0x221C0000	Fault	-	Fault	Fault	Fault	Fault	Fault	-	-
0x30000000	Data Flash	M3	✓	Fault	✓	✓	✓	-	-
0x30008000	Fault	-	Fault	Fault	Fault	Fault	Fault	-	-
For the address of this area, refer to "Table 2.9 Peripheral Area".									
0x5E000000	Code Flash (Mirror)	M2	✓	Fault	✓	✓	✓	-	-
0x5E200000	Fault	-	Fault	Fault	Fault	Fault	Fault	-	-
0x60000000	External Bus Interface area (EBIF)	M12	✓	✓	✓	✓	✓	-	-
0x80000000	Fault	-	Fault	Fault	Fault	Fault	Fault	-	-
0xA0000000	Serial memory interface area (SMIF)	M11	✓	✓	✓	✓	✓	-	-

✓: Accessible, - : No access, Fault: Fault occurred

● Single Boot mode

Table 2.2 TMPM4GxF20 Single Boot Mode

Start address	Slave		Sub master		Main master				
			MDMAC unit A	NBDIF	HDMAC unit A	HDMAC unit B	Core S-Bus	Core D-Bus	Core I-Bus
			SS3	SS4	S1	S2	S3	S4	S5
0x00000000	Boot ROM	M4	Fault	Fault	Fault	Fault	✓	✓	✓
0x00008000	Fault	-	Fault	Fault	Fault	Fault	-	Fault	Fault
0x20000000	RAM0	M5	✓	✓	✓	✓	✓	-	-
0x20010000	RAM1	M6	✓	✓	✓	✓	✓	-	-
0x20020000	RAM2	M7	✓	✓	✓	✓	✓	-	-
0x20028000	RAM3	SM1	✓	✓	Fault	Fault	✓	-	-
0x20030000	RAM4	SM2	✓	✓	Fault	Fault	✓	-	-
0x20038000	RAM5	SM3	✓	✓	Fault	Fault	✓	-	-
0x20040000	Backup RAM	SM4	Fault	✓	Fault	Fault	✓	-	-
0x20040800	Fault	-	Fault	Fault	Fault	Fault	Fault	-	-
0x22000000	Bit band alias	-	Fault	Fault	Fault	Fault	Fault	-	-
0x221C0000	Fault	-	Fault	Fault	Fault	Fault	Fault	-	-
0x30000000	Data Flash	M3	✓	Fault	✓	✓	✓	-	-
0x30008000	Fault	-	Fault	Fault	Fault	Fault	Fault	Fault	Fault
0x3F7F8000	Boot ROM (Mirror)	M4	✓	✓	✓	Fault	Fault	Fault	Fault
0x3F800000	Fault	-	Fault	Fault	Fault	Fault	Fault	Fault	Fault
For the address of this area, refer to "Table 2.9 Peripheral Area".									
0x5E000000	Code Flash (Mirror)	M2	✓	Fault	✓	✓	✓	-	-
0x5E200000	Fault	-	Fault	Fault	Fault	Fault	Fault	-	-
0x60000000	External Bus Interface area (EBIF)	M11	✓	✓	✓	✓	✓	-	-
0x80000000	Fault	-	Fault	Fault	Fault	Fault	Fault	-	-
0xA0000000	Serial memory interface area (SMIF)	M11	✓	✓	✓	✓	✓	-	-

✓: Accessible, - : No access, Fault: Fault occurred

(2) TMPM4GxF15

● Single chip mode

Table 2.3 TMPM4GxF15 Single Chip Mode

Start address	Slave		Sub master		Main master				
			MDMAC unit A	NBDIF	HDMAC unit A	HDMAC unit B	Core S-Bus	Core D-Bus	Core I-Bus
			SS3	SS4	S1	S2	S3	S4	S5
0x00000000	Code Flash (Area0)	M0	Fault	Fault	Fault	Fault	-	Fault	✓
		M1	Fault	Fault	Fault	Fault	-	✓	Fault
0x00180000	Reserved	-	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
0x00200000	Fault	-	Fault	Fault	Fault	Fault	-	-	-
0x20000000	RAM0	M5	✓	✓	✓	✓	✓	-	-
0x20010000	RAM1	M6	✓	✓	✓	✓	✓	-	-
0x20020000	RAM2	M7	✓	✓	✓	✓	✓	-	-
0x20028000	RAM3	SM1	✓	✓	Fault	Fault	✓	-	-
0x20030000	RAM4	SM2	✓	✓	Fault	Fault	✓	-	-
0x20038000	RAM5	SM3	✓	✓	Fault	Fault	✓	-	-
0x20040000	Backup RAM	SM4	Fault	✓	Fault	Fault	✓	-	-
0x20040800	Fault	-	Fault	Fault	Fault	Fault	Fault	-	-
0x22000000	Bit band alias	-	✓	✓	✓	✓	✓	-	-
0x221C0000	Fault	-	Fault	Fault	Fault	Fault	Fault	-	-
0x30000000	Data Flash	M3	✓	Fault	✓	✓	✓	-	-
0x30008000	Fault	-	Fault	Fault	Fault	Fault	Fault	-	-
For the address of this area, refer to "Table 2.9 Peripheral Area".									
0x5E000000	Code Flash (Mirror)	M2	✓	Fault	✓	✓	✓	-	-
0x5E180000	Reserved	-	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
0x5E200000	Fault	-	Fault	Fault	Fault	Fault	Fault	-	-
0x60000000	External Bus Interface area (EBIF)	M12	✓	✓	✓	✓	✓	-	-
0x80000000	Fault	-	Fault	Fault	Fault	Fault	Fault	-	-
0xA0000000	Serial memory interface area (SMIF)	M11	✓	✓	✓	✓	✓	-	-

✓: Accessible, - : No access, Fault: Fault occurred

● Single Boot mode

Table 2.4 TMPM4GxF15 Single Boot Mode

Start Address	Slave		Sub master		Main master				
			MDMAC unit A	NBDIF	HDMAC unit A	HDMAC unit B	Core S-Bus	Core D-Bus	Core I-Bus
			SS3	SS4	S1	S2	S3	S4	S5
0x00000000	Boot ROM	M4	Fault	Fault	Fault	Fault	✓	✓	✓
0x00008000	Fault	-	Fault	Fault	Fault	Fault	-	Fault	Fault
0x20000000	RAM0	M5	✓	✓	✓	✓	✓	-	-
0x20010000	RAM1	M6	✓	✓	✓	✓	✓	-	-
0x20020000	RAM2	M7	✓	✓	✓	✓	✓	-	-
0x20028000	RAM3	SM1	✓	✓	Fault	Fault	✓	-	-
0x20030000	RAM4	SM2	✓	✓	Fault	Fault	✓	-	-
0x20038000	RAM5	SM3	✓	✓	Fault	Fault	✓	-	-
0x20040000	Backup RAM	SM4	Fault	✓	Fault	Fault	✓	-	-
0x20040800	Fault	-	Fault	Fault	Fault	Fault	Fault	-	-
0x22000000	Bit band alias	-	Fault	Fault	Fault	Fault	Fault	-	-
0x221C0000	Fault	-	Fault	Fault	Fault	Fault	Fault	-	-
0x30000000	Data Flash	M3	✓	Fault	✓	✓	✓	-	-
0x30008000	Fault	-	Fault	Fault	Fault	Fault	Fault	Fault	Fault
0x3F7F8000	Boot ROM (Mirror)	M4	✓	✓	✓	Fault	Fault	Fault	Fault
0x3F800000	Fault	-	Fault	Fault	Fault	Fault	Fault	Fault	Fault
For the address of this area, refer to "Table 2.9 Peripheral Area".									
0x5E000000	Code Flash (Mirror)	M2	✓	Fault	✓	✓	✓	-	-
0x5E180000	Reserved	-	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
0x5E200000	Fault	-	Fault	Fault	Fault	Fault	Fault	-	-
0x60000000	External Bus Interface area (EBIF)	M11	✓	✓	✓	✓	✓	-	-
0x80000000	Fault	-	Fault	Fault	Fault	Fault	Fault	-	-
0xA0000000	Serial memory interface area (SMIF)	M11	✓	✓	✓	✓	✓	-	-

✓: Accessible, - : No access, Fault: Fault occurred

(3) TMPM4GxF10

● Single chip mode

Table 2.5 TMPM4GxF10 Single Chip Mode

Start address	Slave		Sub master		Main master				
			MDMAC unit A	NBDIF	HDMAC unit A	HDMAC unit B	Core S-Bus	Core D-Bus	Core I-Bus
			SS3	SS4	S1	S2	S3	S4	S5
0x00000000	Code Flash	M0	Fault	Fault	Fault	Fault	-	Fault	✓
		M1	Fault	Fault	Fault	Fault	-	✓	Fault
0x00100000	Fault	-	Fault	Fault	Fault	Fault	-	-	-
0x20000000	RAM0	M5	✓	✓	✓	✓	✓	-	-
0x20010000	RAM1	M6	✓	✓	✓	✓	✓	-	-
0x20020000	RAM2	M7	✓	✓	✓	✓	✓	-	-
0x20028000	RAM3	SM1	✓	✓	Fault	Fault	✓	-	-
0x20030000	RAM4	SM2	✓	✓	Fault	Fault	✓	-	-
0x20038000	RAM5	SM3	✓	✓	Fault	Fault	✓	-	-
0x20040000	Backup RAM	SM4	Fault	✓	Fault	Fault	✓	-	-
0x20040800	Fault	-	Fault	Fault	Fault	Fault	Fault	-	-
0x22000000	Bit band alias	-	✓	✓	✓	✓	✓	-	-
0x221C0000	Fault	-	Fault	Fault	Fault	Fault	Fault	-	-
0x30000000	Data Flash	M3	✓	Fault	✓	✓	✓	-	-
0x30008000	Fault	-	Fault	Fault	Fault	Fault	Fault	-	-
For the address of this area, refer to "Table 2.9 Peripheral Area".									
0x5E000000	Code Flash (Area0) (Mirror)	M2	✓	Fault	✓	✓	✓	-	-
0x5E100000	Fault	-	Fault	Fault	Fault	Fault	Fault	-	-
0x60000000	External Bus Interface area (EBIF)	M12	✓	✓	✓	✓	✓	-	-
0x80000000	Fault	-	Fault	Fault	Fault	Fault	Fault	-	-
0xA0000000	Serial memory interface area (SMIF)	M11	✓	✓	✓	✓	✓	-	-

✓: Accessible, - : No access, Fault: Fault occurred

● Single Boot mode

Table 2.6 TMPM4GxF10 Single Boot Mode

Start address	Slave		Sub master		Main master				
			MDMAC unit A	NBDIF	HDMAC unit A	HDMAC unit B	Core S-Bus	Core D-Bus	Core I-Bus
			SS3	SS4	S1	S2	S3	S4	S5
0x00000000	Boot ROM	M4	Fault	Fault	Fault	Fault	✓	✓	✓
0x00008000	Fault	-	Fault	Fault	Fault	Fault	-	Fault	Fault
0x20000000	RAM0	M5	✓	✓	✓	✓	✓	-	-
0x20010000	RAM1	M6	✓	✓	✓	✓	✓	-	-
0x20020000	RAM2	M7	✓	✓	✓	✓	✓	-	-
0x20028000	RAM3	SM1	✓	✓	Fault	Fault	✓	-	-
0x20030000	RAM4	SM2	✓	✓	Fault	Fault	✓	-	-
0x20038000	RAM5	SM3	✓	✓	Fault	Fault	✓	-	-
0x20040000	Backup RAM	SM4	Fault	✓	Fault	Fault	✓	-	-
0x20040800	Fault	-	Fault	Fault	Fault	Fault	Fault	-	-
0x22000000	Bit band alias	-	Fault	Fault	Fault	Fault	Fault	-	-
0x221C0000	Fault	-	Fault	Fault	Fault	Fault	Fault	-	-
0x30000000	Data Flash	M3	✓	Fault	✓	✓	✓	-	-
0x30008000	Fault	-	Fault	Fault	Fault	Fault	Fault	Fault	Fault
0x3F7F8000	Boot ROM (Mirror)	M4	✓	✓	✓	Fault	Fault	Fault	Fault
0x3F800000	Fault	-	Fault	Fault	Fault	Fault	Fault	Fault	Fault
For the address of this area, refer to "Table 2.9 Peripheral Area".									
0x5E000000	Code Flash (Mirror)	M2	✓	Fault	✓	✓	✓	-	-
0x5E100000	Fault	-	Fault	Fault	Fault	Fault	Fault	-	-
0x60000000	External Bus Interface area (EBIF)	M11	✓	✓	✓	✓	✓	-	-
0x80000000	Fault	-	Fault	Fault	Fault	Fault	Fault	-	-
0xA0000000	Serial memory interface area (SMIF)	M11	✓	✓	✓	✓	✓	-	-

✓: Accessible, - : No access, Fault: Fault occurred

(4) TMPM4GxFD

● Single chip mode

Table 2.7 TMPM4GxFD Single Chip Mode

Start address	Slave		Sub master		Main master				
			MDMAC unit A	NBDIF	HDMAC unit A	HDMAC unit B	Core S-Bus	Core D-Bus	Core I-Bus
			SS3	SS4	S1	S2	S3	S4	S5
0x00000000	Code Flash	M0	Fault	Fault	Fault	Fault	-	Fault	✓
		M1	Fault	Fault	Fault	Fault	-	✓	Fault
0x00080000	Reserved	-	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
0x00100000	Fault	-	Fault	Fault	Fault	Fault	-	-	-
0x20000000	RAM0	M5	✓	✓	✓	✓	✓	-	-
0x20010000	RAM1	M6	✓	✓	✓	✓	✓	-	-
0x20020000	Reserved	-	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
0x20030000	RAM4	SM2	✓	✓	Fault	Fault	✓	-	-
0x20038000	RAM5	SM3	✓	✓	Fault	Fault	✓	-	-
0x20040000	Backup RAM	SM4	Fault	✓	Fault	Fault	✓	-	-
0x20040800	Fault	-	Fault	Fault	Fault	Fault	Fault	-	-
0x22000000	Bit band alias	-	✓	✓	✓	✓	✓	-	-
0x221C0000	Fault	-	Fault	Fault	Fault	Fault	Fault	-	-
0x30000000	Data Flash	M3	✓	Fault	✓	✓	✓	-	-
0x30008000	Fault	-	Fault	Fault	Fault	Fault	Fault	-	-
For the address of this area, refer to "Table 2.9 Peripheral Area".									
0x5E000000	Code Flash (Mirror)	M2	✓	Fault	✓	✓	✓	-	-
0x5E080000	Reserved	-	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
0x5E100000	Fault	-	Fault	Fault	Fault	Fault	Fault	-	-
0x60000000	External Bus Interface area (EBIF)	M12	✓	✓	✓	✓	✓	-	-
0x80000000	Fault	-	Fault	Fault	Fault	Fault	Fault	-	-
0xA0000000	Serial memory interface area (SMIF)	M11	✓	✓	✓	✓	✓	-	-

✓: Accessible, - : No access, Fault: Fault occurred

●Single Boot mode

Table 2.8 TMPM4GxFD Single Boot Mode

Start Address	Slave		Sub master		Main master				
			MDMAC unit A	NBDIF	HDMAC unit A	HDMAC unit B	Core S-Bus	Core D-Bus	Core I-Bus
			SS3	SS4	S1	S2	S3	S4	S5
0x00000000	Boot ROM	M4	Fault	Fault	Fault	Fault	✓	✓	✓
0x00001800	Fault	-	Fault	Fault	Fault	Fault	-	Fault	Fault
0x20000000	RAM0	M5	✓	✓	✓	✓	✓	-	-
0x20010000	RAM1	M6	✓	✓	✓	✓	✓	-	-
0x20020000	Reserved	-	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
0x20030000	RAM4	SM2	✓	✓	Fault	Fault	✓	-	-
0x20038000	RAM5	SM3	✓	✓	Fault	Fault	✓	-	-
0x20040000	Backup RAM	SM4	Fault	✓	Fault	Fault	✓	-	-
0x20040800	Fault	-	Fault	Fault	Fault	Fault	Fault	-	-
0x22000000	Bit band alias	-	Fault	Fault	Fault	Fault	Fault	-	-
0x221C0000	Fault	-	Fault	Fault	Fault	Fault	Fault	-	-
0x30000000	Data Flash	M3	✓	Fault	✓	✓	✓	-	-
0x30008000	Fault	-	Fault	Fault	Fault	Fault	Fault	Fault	Fault
0x3F7F8000	Boot ROM (Mirror)	M4	✓	✓	✓	Fault	Fault	Fault	Fault
0x3F800000	Fault	-	Fault	Fault	Fault	Fault	Fault	Fault	Fault
For the address of this area, refer to "Table 2.9 Peripheral Area".									
0x5E000000	Code Flash (Area0) (Mirror)	M2	✓	Fault	✓	✓	✓	-	-
0x5E080000	Reserved	-	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
0x5E100000	Fault	-	Fault	Fault	Fault	Fault	Fault	-	-
0x60000000	External Bus Interface area (EBIF)	M11	✓	✓	✓	✓	✓	-	-
0x80000000	Fault	-	Fault	Fault	Fault	Fault	Fault	-	-
0xA0000000	Serial memory interface area (SMIF)	M11	✓	✓	✓	✓	✓	-	-

✓: Accessible, - : No access, Fault: Fault occurred

2.2.2.2. Peripheral Area

Table 2.9 Peripheral Area

Start address	Slave		Sub master		Main master				
			MDMAC unit A	NBDIF	HDMAC unit A	HDMAC unit B	Core S-Bus	Core D-Bus	Core I-Bus
			SS3	SS4	S1	S2	S3	S4	S5
0x40000000	HDMAC (Unit A)	M13	✓	✓	Fault	Fault	✓	-	-
0x40001000	HDMAC (Unit B)	M14	✓	✓	Fault	Fault	✓	-	-
0x40002000	Fault	-	Fault	Fault	Fault	Fault	Fault	-	-
0x40005000	Reserved	-	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
0x40007000	Fault	-	Fault	Fault	Fault	Fault	Fault	-	-
0x4000A000	Reserved	-	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
0x4000C000	SMIF (SFR)	M10	✓	✓	✓	✓	✓	-	-
0x4000D000	Fault	-	Fault	Fault	Fault	Fault	Fault	-	-
0x4003E000	IA (INTIF)	SM5	Fault	✓	Fault	Fault	✓	-	-
0x4003E400	RLM	SM5	Fault	✓	Fault	Fault	✓	-	-
0x4003EC00	LVD	SM5	Fault	✓	Fault	Fault	✓	-	-
0x4003FF00	LTTMR	SM5	Fault	✓	Fault	Fault	✓	-	-
0x4006A000	TSPI (ch0-5)	M8	✓	✓	✓	✓	✓	-	-
0x40076000	EBIF (SFR)	M8	✓	✓	✓	✓	✓	-	-
0x40083000	CG	M9	✓	✓	✓	✓	✓	-	-
0x40083200	IB (INTIF)	M9	✓	✓	✓	✓	✓	-	-
0x40083300	IMN	M9	✓	✓	✓	✓	✓	-	-
0x400A0200	DNF (ch0, 1)	SM6	✓	✓	Fault	Fault	✓	-	-
0x400A0400	TRGSEL	SM6	✓	✓	Fault	Fault	✓	-	-
0x400A0600	SIWDT	SM6	✓	✓	Fault	Fault	✓	-	-
0x400A2000	NBDIF	SM6	✓	✓	Fault	Fault	✓	-	-
0x400A4000	MDMAC	SM6	✓	✓	Fault	Fault	✓	-	-
0x400A8000	FUART (ch0, 1)	SM6	✓	✓	Fault	Fault	✓	-	-
0x400BA000	ADC	SM6	✓	✓	Fault	Fault	✓	-	-
0x400BC800	DAC (ch0, 1)	SM6	✓	✓	Fault	Fault	✓	-	-
0x400C1000	T32A (ch0 to 15)	SM6	✓	✓	Fault	Fault	✓	-	-
0x400CB800	TSPI (ch6 to 8)	SM6	✓	✓	Fault	Fault	✓	-	-
0x400CD000	TSSI (ch0, 1)	SM6	✓	✓	Fault	Fault	✓	-	-
0x400CE000	UART (ch0 to 5)	SM6	✓	✓	Fault	Fault	✓	-	-
0x400D0000	I2S (ch0, 1)	SM6	✓	✓	Fault	Fault	✓	-	-
0x400D1000	I2C (ch0 to 4)	SM6	✓	✓	Fault	Fault	✓	-	-
0x400D8000	EI2C (ch0 to 4)	SM6	✓	✓	Fault	Fault	✓	-	-
0x400DD000	FIR	SM6	✓	✓	Fault	Fault	✓	-	-
0x400E0000	PORT	SM7	Fault	✓	Fault	Fault	✓	-	-
0x400E3100	TRM	SM7	Fault	✓	Fault	Fault	✓	-	-
0x400E4000	OFD	SM7	Fault	✓	Fault	Fault	✓	-	-
0x400E4800	RTC	SM8	Fault	✓	Fault	Fault	✓	-	-
0x400E8000	CEC	SM8	Fault	✓	Fault	Fault	✓	-	-
0x400E8100	RMC (ch0, 1)	SM8	Fault	✓	Fault	Fault	✓	-	-
0x400E9000	A-PMD	SM7	Fault	✓	Fault	Fault	✓	-	-
0x400F0000	ISD	SM8	Fault	✓	Fault	Fault	✓	-	-
0x40100000	Reserved	-	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
0x40180000	Fault	-	Fault	Fault	Fault	Fault	Fault	-	-
0x42000000	Bit Band Alias	-	Fault	Fault	Fault	Fault	✓	-	-
0x44000000	Fault	-	Fault	Fault	Fault	Fault	Fault	-	-
0x5DFF0000	Flash (SFR)	SM7	Fault	✓	Fault	Fault	✓	-	-

✓: Accessible, - : No access, Fault: Fault occurred

2.2.3. RAM Access

The number of clocks required to access the internal RAM is shown in the table below.

Table 2.10 Number of Clocks to Access Each RAM

RAM	fsys	No. of clocks	Description
RAM0	fsysh	1	-
RAM1	fsysh	1 or 2	Refer to "2.2.3.1. List of Registers".
RAM2	fsysh	1 or 2	
RAM3	fsysm	1	Access between the high-speed domain and the middle-speed domain requires synchronization time between domains.
RAM4	fsysm	1	
RAM5	fsysm	1	
Backup RAM	fsysm	5	

2.2.3.1. List of Registers

Change the setting according to the fsysh frequency.
The register and address of FC are shown below.

Peripheral function		Channel/unit	Base address
			TYPE1
Flash memory	FC	-	0x5DFF0000

Register Name		Address (Base+)
Flash Key Code Register (Note)	***[FCKCR]***	0x0018
RAM Access Control Register	***[FCRACCR]***	0x1218

Note: These registers are same as registers of the reference manual "Flash memory".

2.2.3.2. Details of Register

(1) ***[FCKCR]*** (Flash Key Code Register)

Bit	Bit symbol	After reset	Type	Function
31:0	KEYCODE	0x00000000	W	Locked register release key code When ***[FCRACCR]*** is rewritten, write the specific code (0xA74A9D23) to this register. And then rewrite the value of the register within 16 clocks after the previous action. If valid data is written to this register within 16 clocks, released status is reset.

(2) ***[FCRACCR]*** (RAM Access Control Register)

Bit	Bit symbol	After reset	Type	Function
31:14	-	0	R	Read as "0".
13:12	-	00	R/W	Write as "00".
11:10	-	0	R	Read as "0".
9:8	-	00	R/W	Write as "00".
7:6	-	0	R	Read as "0".
5:4	RAMLC1[1:0]	00	R/W	Access control to RAM1, RAM2 00: 1clock (fsysh ≤ 160MHz) 01: 2clocks (fsysh > 160MHz) Others: Reserved
3:2	-	0	R	Read as "0"
1:0	-	00	R/W	Write as "00"

Note1: Rewrite the contents of this register on the program code in the Flash memory.

Note2: To rewrite this register, follow the procedure below:

(a) Write the specific code (0xA74A9D23) to ***[FCKCR]***.
(b) Rewrite data of ***[FCRACCR]***<RAMLC1[1:0]> within 16 clocks after Procedure 1.
(c) After wrote, check read data is same as wrote data.

Note3: When using clock gear, set this register according to the maximum frequency in the application. Do not change the setting even if the frequency is lowered with the clock gear.

3. Reset and Power Control

3.1. Outlines

This section describes how to turn on a power supply, and how to assert and deassert a power-on reset and reset.

Function classification	Factor	Functional description
Cold reset (Reset by turning on a power supply)	Power-on reset	Reset which occurs at the time of turning on or off a power supply.
	LVD reset	Reset which occurs when a power supply voltage is the set-up voltage or below.
	Reset pin	Reset by a RESET_N pin
	PORF reset	Reset which occurs at the time of power supply turning on or turning off. Reset the flash memory and debugging circuit with priority.
Warm reset (Reset without turning on a power supply)	Internal reset	Reset by SIWDT, OFD, LVD, LOCKUP, and <SYSRESETREQ>
	Reset pin	Reset by a RESET_N pin
Reset by STOP2 mode release	Interrupt	Reset which is performed to main power domain during return operation from the STOP2 mode. (STOP2REQ)
	LVD reset	Reset when DVDD3 is equal or less than the voltage which is set on LVD circuit.
	Reset pin	Reset by a RESET_N pin
Single Boot mode starts up	-	TMPM4G Group (1) start by Boot ROM after releasing reset.

3.2. Function and Operation

This section explains about power-on, power off and reset.

Note: Refer to "Electrical Characteristics" of a datasheet for the time and voltage of description of the symbol in a figure.

3.2.1. Cold Reset

When turn on a power supply, the stabilization time for the built-in regulator, the built-in flash memory, and the built-in high-speed oscillator is necessary the TXZ+ family automatically insert a wait time for the stabilization of these circuits.

When turning on the power, please make sure that the slope of the power supply voltage rises to the right.

When the power supply voltage drops and rises near POR and PORF detection, it may not operate normally even if the power supply voltage rises to the guaranteed operating range.

3.2.1.1. Reset by Power-on Reset Circuit (without Using RESET_N Pin)

After a supply voltage exceeds the release voltage of a power-on reset (POR), internal reset is deasserted after "Internal initialization time" is elapsed. Please increase a supply voltage goes up into an operating voltage range before "Internal initialization time" is elapsed. The CPU operates after internal reset is released.

After a supply voltage exceeds the release voltage of a power-on reset (POR), LVD continues to output reset signal until supply voltage exceeds the LVD release voltage. And internal reset has priority during the time of "Internal initialization time". When rising time of a supply voltage beyond "Internal initialization time", please refer to "3.2.1.3. Continuation of Reset by LVD".

For example, if the operating voltage of a circuit board is more than 2.7V, after power-on reset released, increase a supply voltage to 2.7V before "Internal initialization time" is elapsed.

DVDD3= DVDD3A= DVDD3B= DVDD3C= DVDD3D= DVDD3E= DVDD3F= DVDD3G= DVDD3H= AVDD3

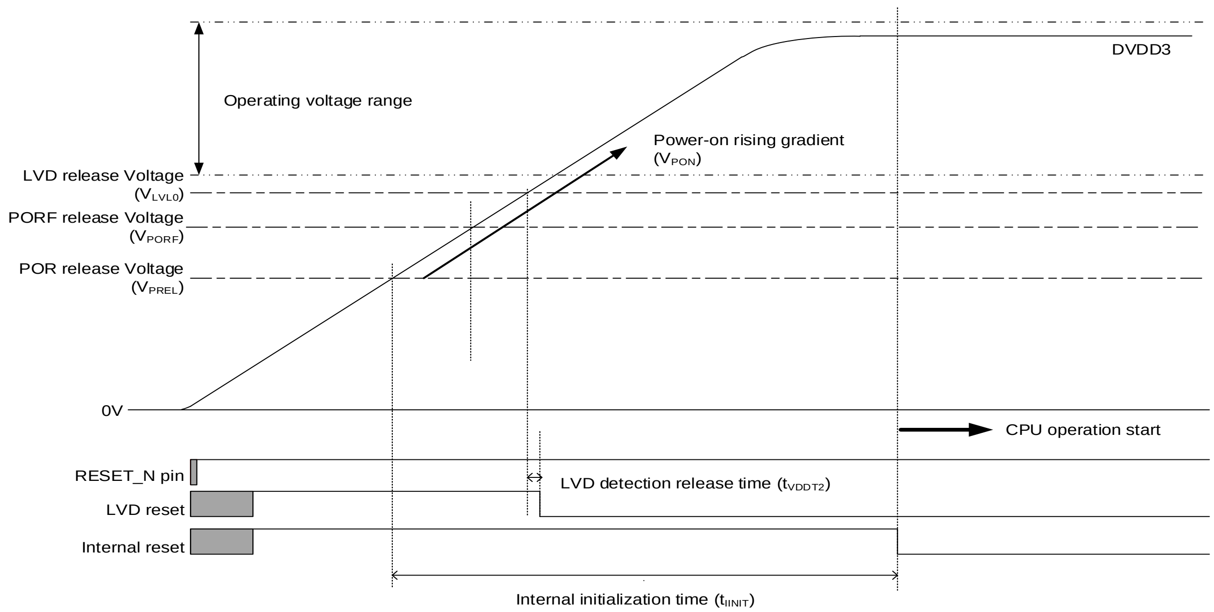


Figure 3.1 Reset Operation by Power-on Reset Circuit

Note: When you use only a power-on reset circuit without RESET_N pin, the RESET_N pin should input "High" level or opened.

3.2.1.2. Reset by RESET_N Pin

When turn on a power supply, it can control the timing of reset release by using RESET_N pin.

After a supply voltage exceeds the release voltage of a power-on reset and even after "Internal initialization time" elapsed, if the RESET_N pin is "Low", internal reset continues.

After a supply voltage goes up into an operating voltage range, if a RESET_N pin becomes "High" level, internal reset is deasserted after "CPU waiting time" elapses.

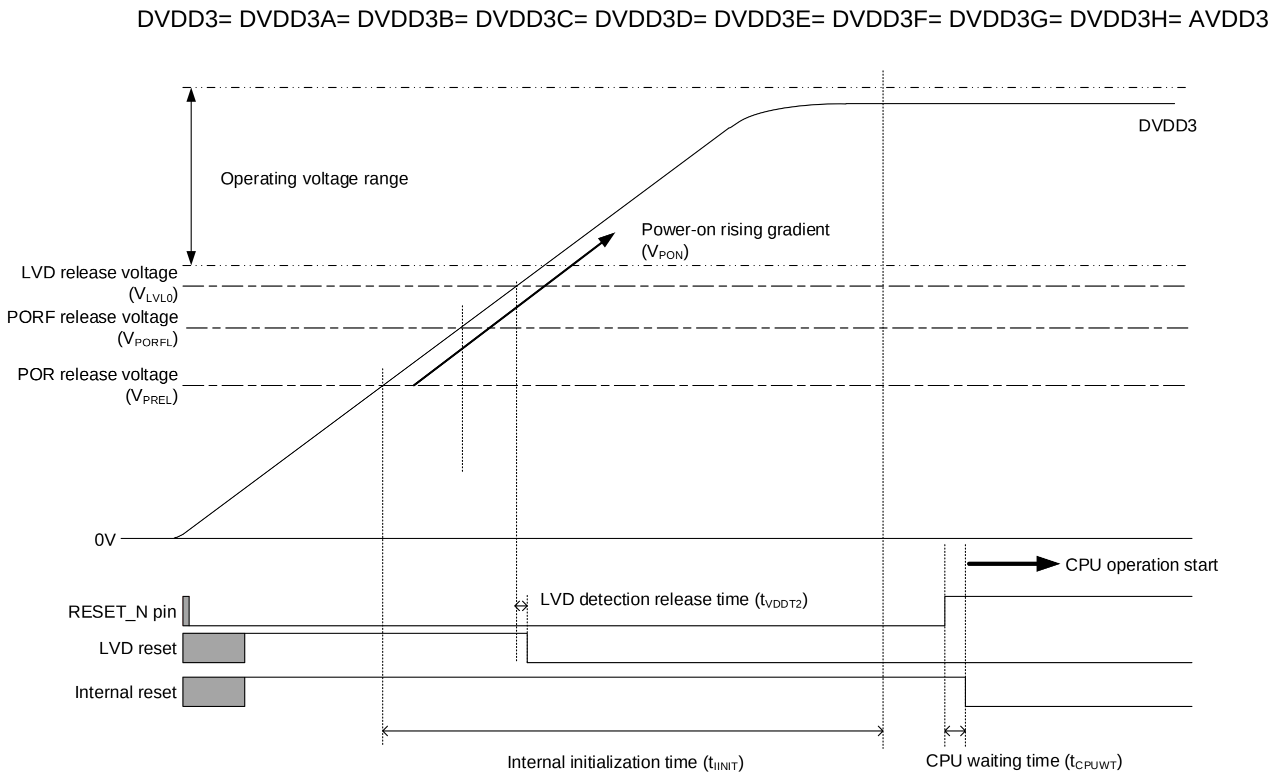


Figure 3.2 Reset Operation by RESET_N Pin (1)

In case of RESET_N pin input change from "Low" level to "High" level before "Internal initialization time" elapses, internal reset signal is released after "Internal initialization time" elapses.

Please goes up a supply voltage into an operating voltage range before "Internal initialization time" elapses. The CPU operates after internal reset release.

DVDD3= DVDD3A= DVDD3B= DVDD3C= DVDD3D= DVDD3E= DVDD3F= DVDD3G= DVDD3H= AVDD3

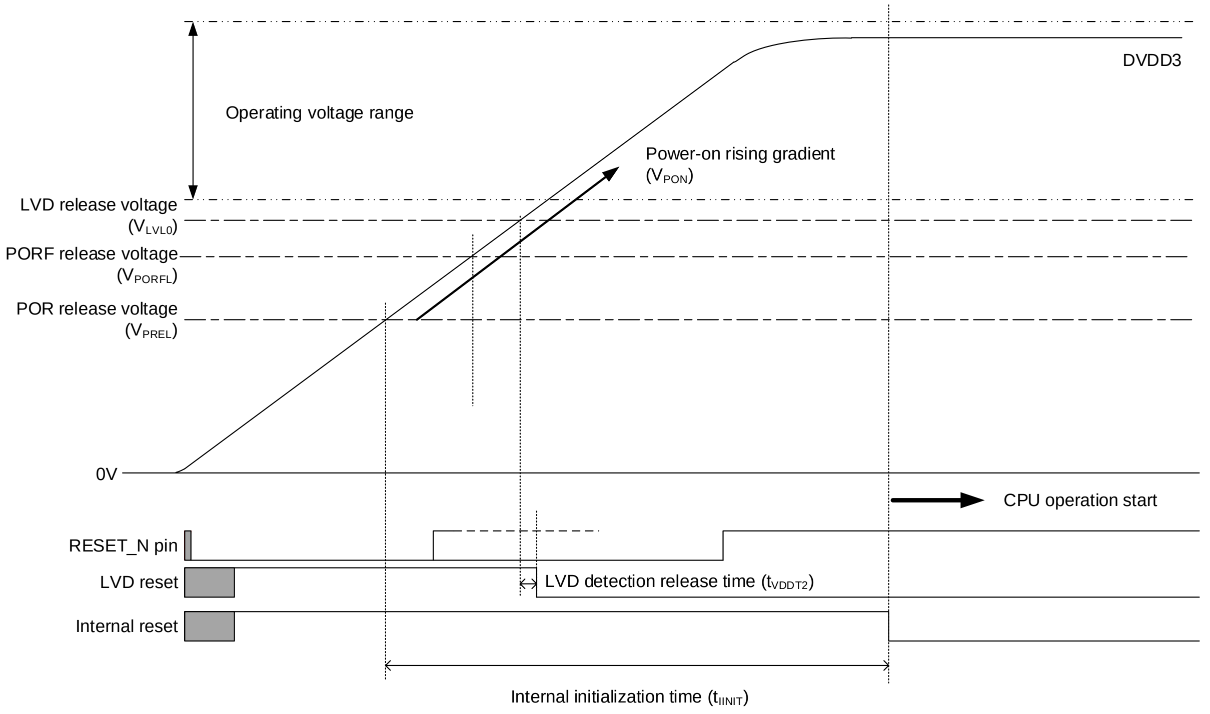


Figure 3.3 Reset Operation by RESET_N Pin (2)

3.2.1.3. Continuation of Reset by LVD

When the power supply voltage has not exceeded the LVD release voltage even after "Internal initialization time" elapsed, LVD generates the reset signal, and the reset state continues. After the power supply voltage exceeds the LVD release voltage and "LVD detection release time" + "CPU operation wait time" elapses, the internal reset is deasserted. And CPU starts operating. Refer to Reference Manual "Voltage detection circuit" for detail of LVD.

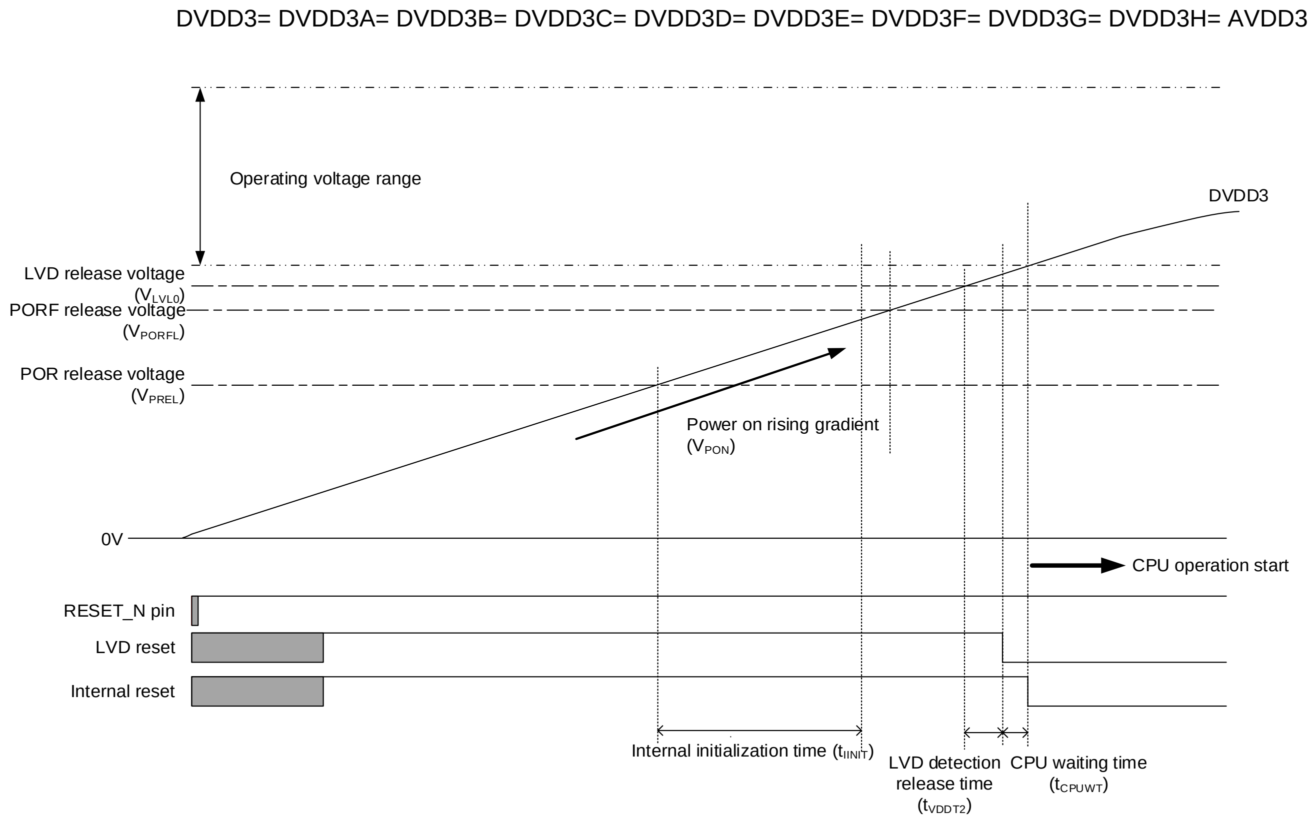


Figure 3.4 Reset Operation by LVD Reset

3.2.2. Warm Reset

3.2.2.1. Warm Reset by REST_N Pin

When resetting with the RESET_N pin, set the RESET_N pin to "Low" level for 17.2 μs or more while the power supply voltage is within the operating range.

When the "Low" level period of a RESET_N pin is longer than "Internal processing time", after a RESET_N pin changes to "High" level, internal reset is released after "CPU waiting time" elapsed.

When the "Low" level period of a RESET_N pin is shorter than "Internal processing time", after internal reset is extended and from a RESET_N pin changes "Low" level, internal reset is release after "Internal processing time" + "CPU waiting time" has elapsed, internal reset will be released.

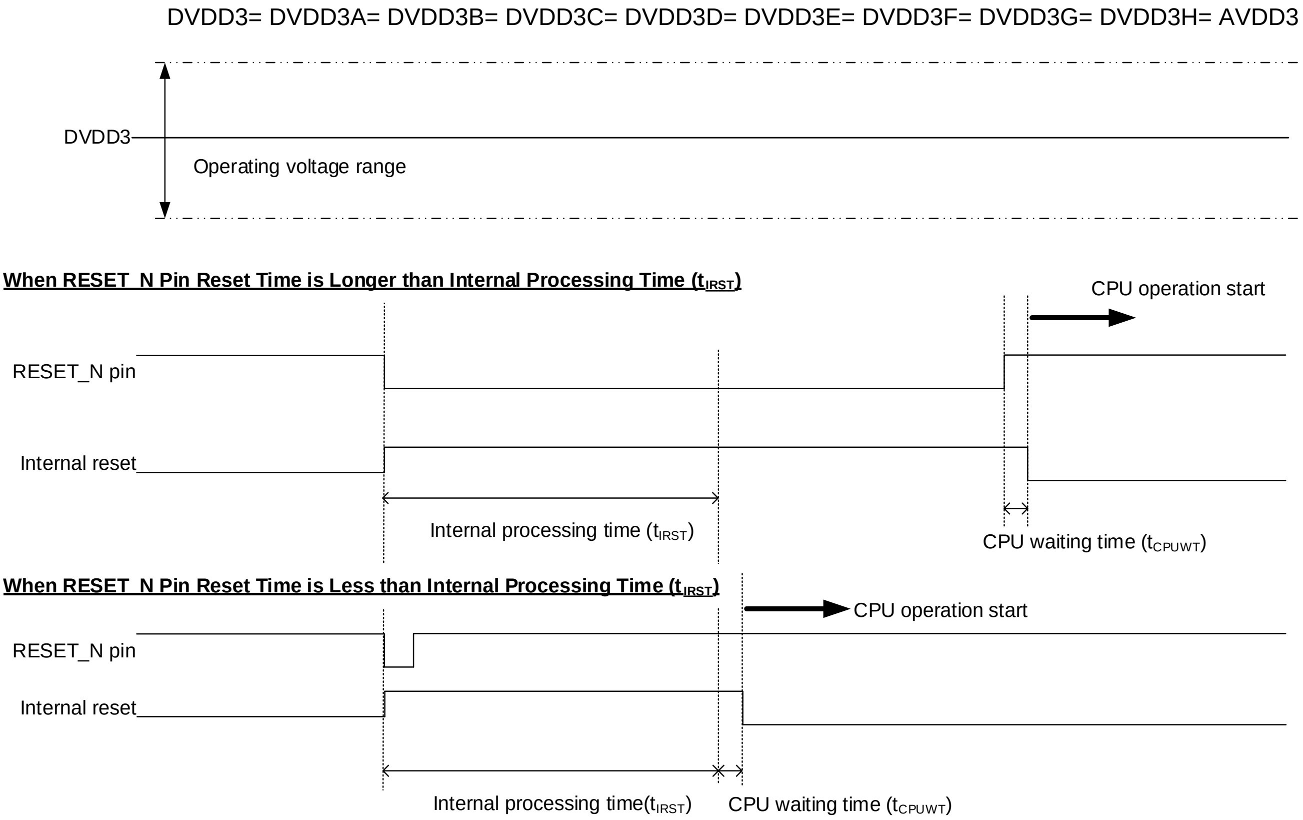


Figure 3.5 Warm Reset Operation

3.2.2.2. Warm Reset by Internal Reset

In case of reset asserted by internal factors, such as SIWDT, OFD, LVD, LOCKUP, and <SYSRESETREQ>, internal reset is released after "Internal processing time" + "CPU waiting time" elapsed.

3.2.3. Reset by STOP2 Mode Release

When RESET_N pin changed "Low" level or LVD reset occurred during STOP2 mode, STOP2 released. The power supply is turned on and assert reset to main power domain. After RESET_N pin changes to "High" level or LVD reset released, start operating in NORMAL mode. At that time, condition of CPU is as same as cold reset except ***[RLMLOSCCR]***, ***[RLMRSTFLG0]***, ***[RLMRSTFLG1]***.

When asserted interrupt request during STOP2 mode, also STOP2 released. The power supply is turned on and assert reset to main power domain in the sequence of releasing STOP2 mode. Refer to "1.3.3.3. Restart Operation from STOP2 Mode" for the operation at the time of STOP2 release.

3.2.4. Starting Single Boot Mode

For the details of the single mode, refer to the reference manual "Flash memory".

3.2.4.1. Starting Single Boot Mode by RESET_N pin

When "Low" level is input to a Boot_N pin, and then reset release, "single Boot mode" will be started.

When turn on power supply, the time of input "Low" level to the RESET_N pin is equal to or longer than "Internal initialization time" to reset. And deassert RESET_N pin to "High", after a supply voltage goes up into an operating voltage range.

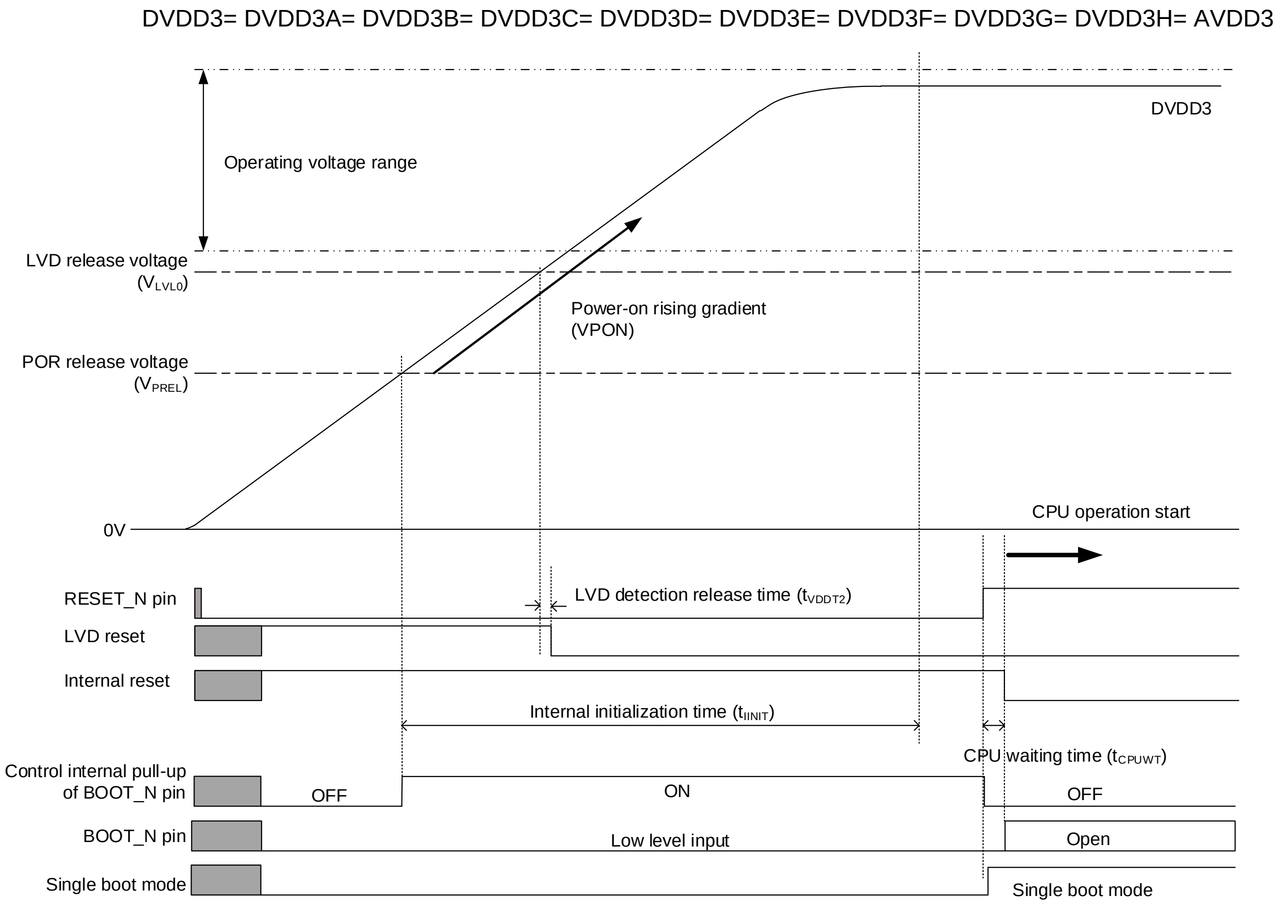


Figure 3.6 Starting Single Boot Mode by RESET_N Pin

3.2.4.2. Starting Single Boot Mode by Power-on Reset (Not Using RESET_N Pin)

When and turning on power supply, "Low" level is input to Boot_N pin. After the internal reset is deasserted, the CPU operation starts, and the single Boot mode starts up.

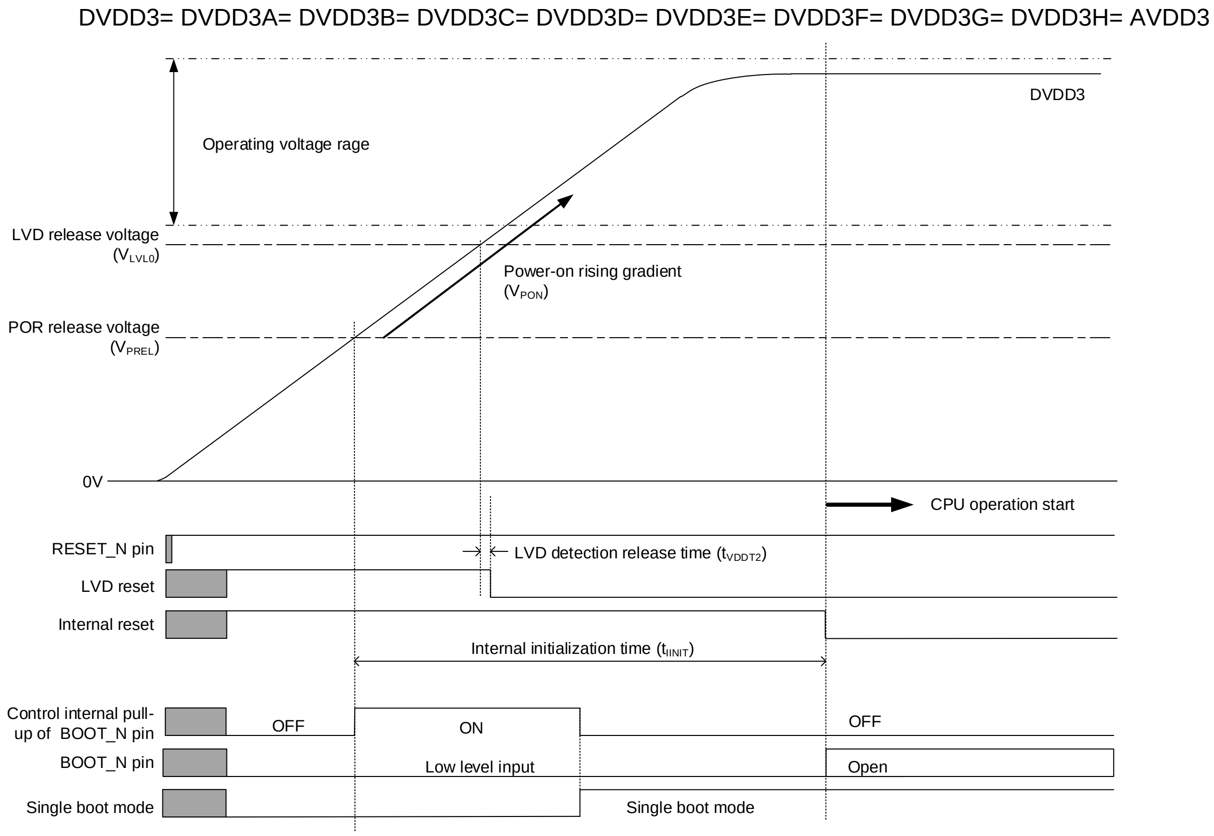


Figure 3.7 Starting Single Boot Mode by Power-on Reset (Not Using RESET_N Pin)

3.2.4.3. Starting Single Boot Mode when Power Supply is Stable

When the supply voltage is stable within an operating voltage range, input "Low" level to RESET_N pin for reset equal to or longer than "Internal processing time", while "Low" level is input to the Boot_N pin.

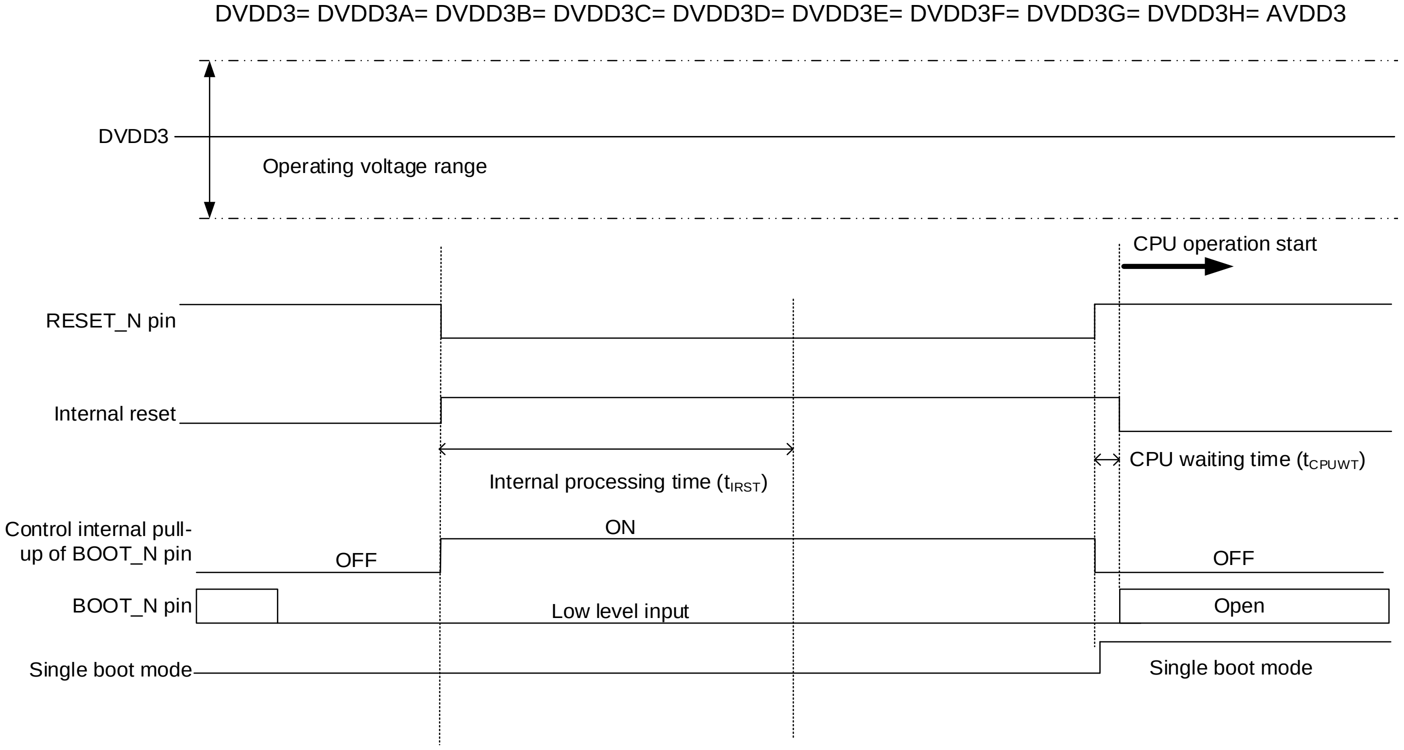


Figure 3.8 Starting Single Boot Mode when Power Supply is Stable

3.2.5. Power-on Reset Circuit

The power-on reset circuit (POR) generates a reset signal when the power is turned on or turned off.

Note: The power-on reset circuit may not operate correctly due to the fluctuation of the power supply. Equipment should be designed with full consideration of the electrical characteristics.

The power-on reset circuit consists of a detection voltage generation circuit, a reference voltage generation circuit, and a comparator.

The supply voltage has referred to DVDD3 (= DVDD3A= DVDD3B= DVDD3C= DVDD3D= DVDD3E= DVDD3F= DVDD3G= DVDD3H).

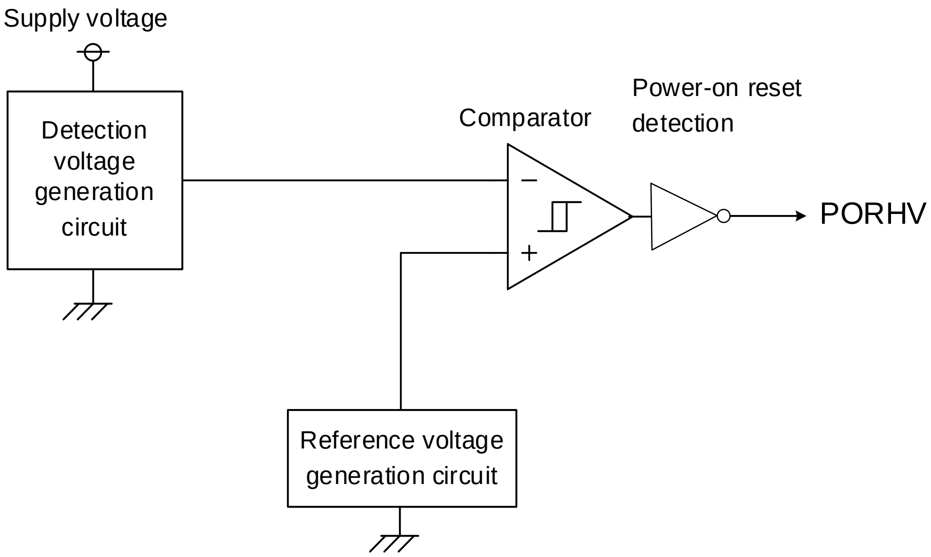


Figure 3.9 Power-on Reset Circuit

3.2.5.1. Operation at Time of Turn On

When turn on power supply, while the power supply voltage is equal to or lower than power-on reset release voltage (V_{PREL}), the power-on reset detection signal is generated. Refer to "Figure 3.1 Reset Operation by Power-on Reset Circuit" for detail.

While the power-on reset signal is generated, the reset is asserted to the CPU and the peripherals.

3.2.5.2. Operation at Time of Turn Off

When turn off power supply, while the power supply voltage is equal to or lower than power-on reset detection voltage (V_{PDET}), the power-on reset detection signal is generated.

While the power-on reset signal is generated, the reset is asserted to the CPU and the peripherals.

3.2.6. Precautions when Turning Off Power

When turning off the power, always follow the prescribed procedure to reduce the power supply voltage.

DVDD3= DVDD3A= DVDD3B= DVDD3C= DVDD3D= DVDD3E= DVDD3F= DVDD3G= DVDD3H= AVDD3

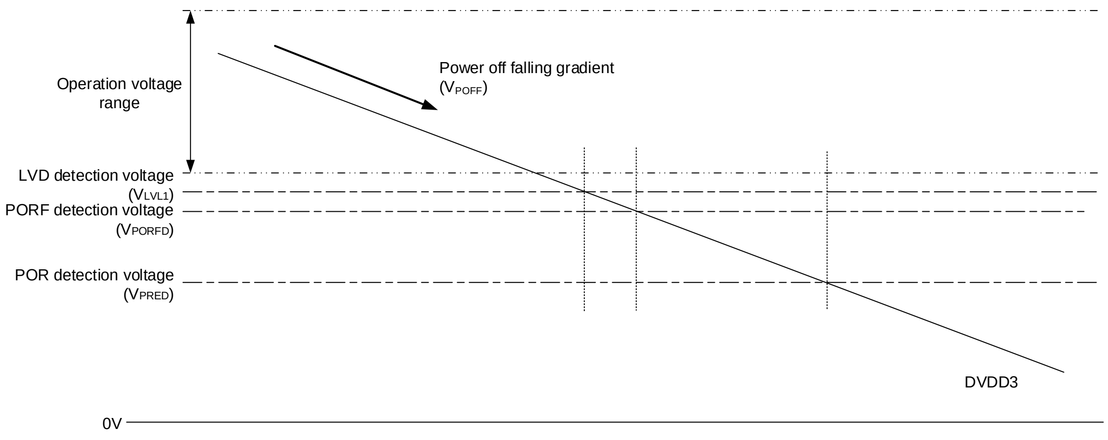


Figure 3.10 Falling Gradient when Turning Off Power

Flash memory and circuits that include debug are reset by PORF reset. Refer to "3.2.8.1. Reset Factor and Reset Range" for detail.

3.2.7. About Turn On Power Supply after Turn Off

3.2.7.1. When Using External Reset Circuit or Internal LVD Reset Output

When the power supply is turned off and the power supply voltage drops below the operation guaranteed voltage, reset is performed with an external reset circuit or built-in LVD (when the voltage is less than the set voltage). After that, from the state where the reset is applied, please follow the same constraints as when turning on the power and turned on the power supply voltage.

3.2.7.2. When not Using External Reset Circuit and Internal LVD Reset Output

When the power supply is turned off and the power supply voltage drops below the operation guaranteed voltage, be sure to lower the power supply voltage below the power-on reset detection voltage (V_{PDET}) and hold it for 200μs or more. After that, please follow the same constraints as when turning on the power and turned on the power supply voltage.
When the power supply voltage drops below the power-on reset detection voltage (V_{PDET}) and cannot be held for 200μs or more, or when the same constraints as at Power on cannot keep , the CPU may not operate properly.

3.2.7.3. When Boundary Scan is Used

When the power supply is turned off and the power supply voltage drops below the operation guaranteed voltage, a voltage of power supply must go to 0V. Follow the same constraints as when turning on the power and turned on the power supply voltage.

3.2.8. After Reset Release

All of the control register of Cortex-M4 (with FPU) core and the peripheral function control register (SFR) are initialized by reset. But depend on the reset factor, initialized range is different.

Please refer to "Table 3.1 Reset Factor and Range Initialized" for the initialized range by each reset factor.

The reset factor when reset occurs can be checked by a reset flag register which are ***[RLMRSTFLG0]*** and ***[RLMRSTFLG1]***. For detail of ***[RLMRSTFLG0]*** and ***[RLMRSTFLG1]***, please refer to reference manual "Exception".

After the reset is released, CPU starts operation by a clock of internal high-speed oscillator 1 (IHOSC1). The external clock and PLL multiple circuit should be set if necessary.

3.2.8.1. Reset Factor and Reset Range

Reset factors and the range initialized are shown in Table 3.1.

Table 3.1 Reset Factor and Range Initialized

Registers and peripheral function		Reset factors								
		STOP2 mode release		Cold Reset	Warm reset (Note1)					
		Interrupt factor	Reset pin (Note1) (Note3)	POR (Note1)	Reset pin	OFD reset	SIWDT reset	LVD reset	CPU <SYS RESET REQ> reset	CPU LOCKUP reset
	Reset signal name	STOP2 REQ	RESET_N	PORHV	RESET_N	OFD RSTOUT	WDT RSTOUT	LVD RSTOUT	SYS RESET REQ	LOCKUP RESET REQ
RTC	***[RTCSECR]*** ***[RTCMINR]*** ***[RTCHOURR]*** ***[RTCDAYR]*** ***[RTCDATER]*** ***[RTCMONTHR]*** ***[RTCYEARR]*** ***[RTCADJCTL]*** ***[RTCADJDAT]*** ***[RTCADJSIGN]*** ***[RTCPAGER]*** (Note2)	-	-	-	-	-	-	-	-	-
	Except above	-	✓	✓	✓	✓	✓	✓	✓	✓
Low-speed oscillation/ power control Reset flag	***[RLMSHTDNOP]*** ***[RLMPROTECT]***	-	✓	✓	✓	✓	✓	✓	✓	✓
	[RLMLOSCCR] ***[RLMRSTFLG0]*** ***[RLMRSTFLG1]***	-	-	✓	-	-	-	-	-	-
Interrupt control	***[IAIMCxx]*** ***[IANIC00]***	-	✓	✓	✓	✓	✓	✓	✓	✓
	[IBIMCxxx] ***[IBNIC00]***	✓	✓	✓	✓	✓	✓	✓	✓	✓
FLASH	***[FCSBMR]***	✓	✓	✓	- (Note4)	-	-	- (Note4)	-	-
Port	All registers	✓	✓	✓	✓	✓	✓	✓	✓	✓
OFD		✓	✓	✓	✓	✓	✓	✓	✓	✓
LVD		-	✓	✓	✓	-	-	-	-	-
LTTMR, ISD, RMC, CEC		-	✓	✓	✓	✓	✓	✓	✓	✓
Debugging interface		✓	✓	✓	- (Note4)	-	-	- (Note4)	-	-
Except above		✓	✓	✓	✓	✓	✓	✓	✓	✓

✓ : It is initialized.

- : It is not initialized.

Note1: When reset is performed, the data of built-in RAM will not be guaranteed.

Note2: ***[RTCPAGER]***<ENATMR><ENAALM> are not initialized. Other symbols are initialized.

Note3: Reset area released by LVD reset in STOP2 mode is reset area released by the warm-reset.

Note4: Debug interface is initialized by the reset in STOP1mode. And it is not initialized by the reset in NORMAL, IDLE, or STOP mode.

4. Revision History

Table 4.1 Revision History

Revision	Date	Description
1.0	2020-12-14	First release
1.1	2021-06-30	- Correct Figure 1.3. - 1.3.3.3. The restart operation from the STOP2 mode Change Note2 to Note3, and Note3 is corrected. Added Note2. - 1.3.4.2. NORMAL → ISTOP1 → INORMAL Operation mode transition Added Note. - 1.3.4.3. NORMAL → STOP2 → RESET → NORMAL Operation mode transition Added Note. - 3.1 Outline Table Added LVD reset factor. - 3.2.3. Reset by STOP2 mode release Changed description. - Table 3.1 A reset factor and the initialized range Deleted "PORF" from interrupt factor in table 3.1. Added Note3 in STOP2 Release, Reset pin column. Added Note4 to FLASH ***[FCSBMR]*** in Warm reset, Reset pin and LVD reset. Added Note4 to debug interface in Warm reset, Reset pin and LVD reset. Added Note3 and Note4.
1.2	2023-06-14	- Table 1.10 Block operation status in each low-power Consumption mode The operation status of SIWDT in STOP1 mode is changed. "IDLE mode" in note 2 is changed to "IDLE/STOP1 mode". - 1.3.2.1. IDLE mode transition flow Note is added. - 1.3.2.3. STOP2 mode transition flow Note2 is deleted. - 1.4.2.2. ***[CGOSCCR]*** (Oscillation control register) Note3 is deleted. Note4 is changed to Note 3. Note4 in description of <IHOSC1F> is changed to Note3.
1.3	2023-09-15	- Figure 1.1 Clock system diagram Figure 1.1 is changed. - 1.3.1.4. Peripheral function state in a low-power Consumption mode Note2 is changed. - 1.3.3.1. The release source of a low-power Consumption mode Released by Non-Maskable Interrupt (NMI) The explanation of Released by Non-Maskable Interrupt (NMI) is changed.
1.4	2024-05-31	- 1.2.3. Clock System diagram Figure. 1.1. Clock System Diagram is changed. - 1.2.6.1 Setting Method of System Clock (2) fosc setup (internal oscillation → external clock input) Step 1 in the table "<< Example of switching procedure >>" is changed. (3) fosc setup (external oscillation/external clock input → internal oscillation) Step 5 in the table "<< Example of switching procedure >>" is changed. - 1.2.7. Low-speed Clock (1) ELOSC setup (not used low-speed clock → external low-speed oscillator used) <<Example of switching procedure>> is changed. (2) ELCLKIN setup (No Operation of External Low-speed Oscillator → Operation) <<Example of switching procedure>> is changed. - 1.4.2.13. ***[CGSPCLKEN]*** (Clock Supply for ADC and Debug Circuit Register) Note1 and note2 are added. - 1.4.2.15. ***[RLMLOSCCR]*** (Low-speed Oscillation and Internal High-speed Oscillation 2 Clock Control Register) The function of <XTEN> is changed. - 2.2 Bus Matrix A description is changed. - 3.2.7. About Turn On Power Supply after Turn Off "3.2.7.3. When Boundary Scan is Used" is added.

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