32-bit RISC Microcontroller

TXZ+ Family

Reference manual
8-bit Digital to Analog Converter (DAC-B)

Revision 1.0

2020-09

TOSHIBA ELECTRONIC DEVICES & STORAGE CORPORATION

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Conventions

- Numeric formats follow the rules as shown below:
  Hexadecimal: 0xABC
  Decimal: 123 or 0d123 – Only when it needs to be explicitly shown that they are decimal numbers.
  Binary: 0b111 – It is possible to omit the "0b" when the number of bit can be distinctly understood from a sentence.
- "_N" is added to the end of signal names to indicate low active signals.
- It is called "assert" that a signal moves to its active level, "deassert" to its inactive level.
- When two or more signal names are referred, they are described like as [m: n].
  Example: S[3: 0] shows four signal names S3, S2, S1 and S0 together.
- The characters surrounded by ***[ ]*** defines the register.
  Example: ***[ABCD]***
- "n" substitutes suffix number of two or more same kind of registers, fields, and bit names.
  Example: ***[XYZ1], [XYZ2], [XYZ3] -> [XYZn]***
- "x" substitutes suffix number or character of units and channels in the Register List.
  In case of unit, "x" means A, B, and C ...
  Example: ***[ADACR0]***, ***[ADBCR0]***, ***[ADCCR0] -> [ADxCR0]***
  In case of channel, "x" means 0, 1, and 2 ...
  Example: ***[T32A0RUNA]***, ***[T32A1RUNA]***, ***[T32A2RUNA] -> [T32AxRUNA]***
- The bit range of a register is written like as [m: n].
  Example: Bit[3: 0] expresses the range of bit 3 to 0.
- The configuration value of a register is expressed by either the hexadecimal number or the binary number.
  Example: ***[ABCD]***<EFG> =0x01 (hexadecimal), ***[XYZn]***<VW> =1 (binary)
- Word and Byte represent the following bit length.
  Byte: 8 bits
  Half word: 16 bits
  Word: 32 bits
  Double word: 64 bits
- Properties of each bit in a register are expressed as follows:
  R: Read only
  W: Write only
  R/W: Read and Write are possible
- Unless otherwise specified, register access supports only word access.
- The register defined as reserved must not be rewritten. Moreover, do not use the read value.
- The value read from the bit having default value of "-" is unknown.
- When a register containing both of writable bits and read-only bits is written, read-only bits should be written with their default value, In the cases that default is "-", follow the definition of each register.
- Reserved bits of the Write-only register should be written with their default value.
  In the cases that default is "-", follow the definition of each register.
- Do not use read-modified-write processing to the register of a definition which is different by writing and read out.

Terms and Abbreviations

Some of abbreviations used in this document are as follows:

DAC	Digital to Analog Converter

1. Outlines

8-bit digital / analog converter (DAC) builds in the DAC output circuit of one channel (DACx) per 1 unit.
The main functions are as follows.

Function Classification	Function	Operation
DAC output	Conversion system	R-2R Resistance rudder type
	Resolution	8 bits
	Buffer amplifier	Un-built-in

2. Configuration

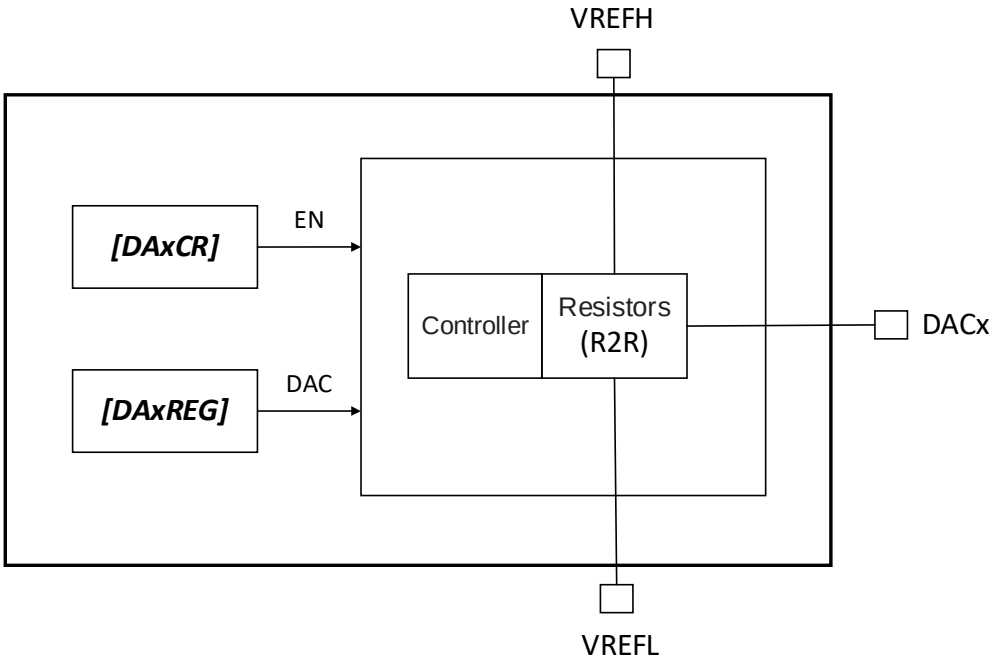

Figure 2.1 8-bit DAC configuration

Table 2.1 List of signals

No.	Symbol	Signal name	I/O	Related Reference Manual
1	DACx	DAC Output terminal	Output	Product Information
2	VREFH	Analog reference power supply terminal	Input	Product Information
3	VREFL	Analog reference GND terminal	Input	Product Information

3. Function and Operation

3.1. Setting

When you use DAC, please set an applicable clock enable bit to "1" (clock supply) in fsys supply stop register A (***[CGFSYSENA]***, ***[CGFSYSMENA]***), fsys supply stop register B (***[CGFSYSENB]***, ***[CGFSYSMENB]***), fsys supply stop register C (***[CGFSYSMENC]***), and fc supply stop register (***[CGFCEN]***). Please refer to "Clock Control and Operation Mode" of the reference manual for the details.

The voltage corresponding to the preset value is outputted to the DACx terminal by setting ***[DAxCR]***<EN> to "1" and setting the conversion value to the ***[DAxREG]*** register.

By setting ***[DAxCR]***<EN> to "0", DAC stops operation and the DAC output becomes Hi-Z.

4. Registers

4.1. List of Registers

The control registers and their addresses are shown in the following tables.

Peripheral function	Function name	Channel/Unit	Base address	
			TYPE 1	TYPE 2
8-bit Digital to Analog Converter	DAC	ch0	0x40054000	0x400BC800
		ch1	0x40055000	0x400BC900

Note: The Channel/Unit and Base address type are different by products. Please refer to "Product Information" of the reference manual for the details.

Register Name		Address(Base+)
Control Register	***[DAxCR]***	0x0000
Converted Value Setting Register	***[DAxREG]***	0x0004

4.2. Details of Registers

4.2.1. *[DAxCR]* (Control Register)

Bit	Bit Symbol	After Reset	Type	Function
31:1	-	0	R	Read as "0"
0	EN	0	R/W	DAC operation 0: Stop 1: Operating

4.2.2. *[DAxREG]* (Converted Value Setting Register)

Bit	Bit Symbol	After Reset	Type	Function
31:8	-	0	R	Read as "0"
7:0	DAC[7:0]	0x00	R/W	Converted value setting: Digital value corresponding to the analog output voltage value is set. The output voltage is calculated with the following formula. DACx = <DAC> × (VREFH - VREFL) / 256

5. Revision History

Table 5.1 Revision History

Revision	Date	Description
1.0	2020-09-25	First release

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