32-Bit RISC Microcontroller

TXZ+ Family
TMPM4G Group(1)

Reference Manual
Exception
(EXCEPT-M4G(1))

Revision 1.0

2020-11

TOSHIBA ELECTRONIC DEVICES & STORAGE CORPORATION

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Arm® Cortex®-M4 Processor Technical Reference Manual

Conventions

- Numeric formats follow the rules as shown below:
  Hexadecimal: 0xABC
  Decimal: 123 or 0d123 – Only when it needs to be explicitly shown that they are decimal numbers.
  Binary: 0b111 – It is possible to omit the "0b" when the number of bit can be distinctly understood from a sentence.
- "_N" is added to the end of signal names to indicate low active signals.
- It is called "assert" that a signal moves to its active level, "deassert" to its inactive level.
- When two or more signal names are referred, they are described like as [m: n].
  Example: S[3: 0] shows four signal names S3, S2, S1 and S0 together.
- The characters surrounded by ***[ ]*** defines the register.
  Example: ***[ABCD]***
- "n" substitutes suffix number of two or more same kind of registers, fields, and bit names.
  Example: ***[XYZ1], [XYZ2], [XYZ3] → [XYZn]***
- "x" substitutes suffix number or character of units and channels in the Register List.
  In case of unit, "x" means A, B, and C ...
  Example: ***[ADACR0], [ADBCR0], [ADCCR0] → [ADxCR0]***
  In case of channel, "x" means 0, 1, and 2 ...
  Example: ***[T32A0RUNA], [T32A1RUNA], [T32A2RUNA] →[T32AxRUNA]***
- The bit range of a register is written like as [m: n].
  Example: Bit[3: 0] expresses the range of bit 3 to 0.
- The configuration value of a register is expressed by either the hexadecimal number or the binary number.
  Example: ***[ABCD]***<EFG> = 0x01 (hexadecimal), ***[XYZn]***<VW> = 1 (binary)
- Word and Byte represent the following bit length.
  Byte: 8 bits
  Half word: 16 bits
  Word: 32 bits
  Double word: 64 bits
- Properties of each bit in a register are expressed as follows:
  R: Read only
  W: Write only
  R/W: Read and Write are possible
- Unless otherwise specified, register access supports only word access.
- The register defined as reserved must not be rewritten. Moreover, do not use the read value.
- The value read from the bit having default value of "-" is unknown.
- When a register containing both of writable bits and read-only bits is written, read-only bits should be written with their default value, In the cases that default is "-", follow the definition of each register.
- Reserved bits of the Write-only register should be written with their default value. In the cases that default is "-", follow the definition of each register.
- Do not use read-modified-write processing to the register of a definition which is different by writing and read out.

Terms and Abbreviations

Some of abbreviations used in this document are as follows:

ADC	Analog to Digital Converter
A-PMD	Advanced Programmable Motor Control Circuit
CEC	Consumer Electronics Control
DMAC	Direct Memory Access Controller
EI2C	I^2C Interface Version A
FIR	Finite Impulse Response
FUART	Full Universal Asynchronous Receiver Transmitter
IA	Interrupt control register A
IB	Interrupt control register B
INT	Interrupt
INTIF	Interrupt Interface Logic
IMCxx	Interrupt Mode Control xx
IMNFLGNMI	Interrupt Monitor Flag NMI
IMNFLGx	Interrupt Monitor Flag x
ISD	Interval Sensor Detection
ISR	Interrupt Service Routine
I2C	Inter-Integrated Circuit
I2S	Inter-IC Sound
LTTMR	Long Term Timer
LVD	Voltage Detection Circuit
NICxx	Non maskable Interrupt Control xx
OFD	Oscillation Frequency Detector
POR	Power On Reset Circuit
PORF	Power On Reset for FLASH and debug
RLM	Low speed oscillation / power supply control / reset
RLMRSTFLGx	RLM Reset Flag x
RMC	Remote Control Signal Preprocessor
RTC	Real Time Clock
SIWDT	Clock Selective Watchdog Timer
SMIF	Serial Memory Interface
TSPI	Serial Peripheral Interface
TSSI	Synchronized Serial Interface
T32A	32-bit Timer Event Counter
UART	Universal Asynchronous Receiver Transmitter

Exceptions have close relation to the CPU core. Refer to "Arm documentation set for the Arm Cortex-M4 processor" if needed.

1. Outlines

Exceptions require CPU to suspend the currently executing process, and to start another process.

There are two types of exceptions: those that are generated when some error condition occurs or when an instruction to generate an exception is executed; and those that are generated by hardware, such as an interrupt request signal from an external pin or peripheral function.

All exceptions are handled by the Nested Vectored Interrupt Controller (NVIC) in the CPU according to the respective priority levels. When an exception occurs, the CPU stores the current state to the stack and branches to the corresponding interrupt service routine (ISR). Upon completion of the ISR, the information stored to the stack is automatically restored.

1.1. Exception Types

The following types of exceptions exist in the Cortex-M4.

For detailed descriptions on each exception, refer to "Arm documentation set for the Arm Cortex-M4 processor".

- Reset
- Non-maskable Interrupt (NMI)
- Hard Fault
- Memory Management
- Bus Fault
- Usage Fault
- SVCall (Supervisor Call)
- Debug Monitor
- PendSV
- SysTick
- External Interrupt

1.2. Exception Handling Flowchart

The following shows how an exception/interrupt is handled. In the following descriptions, exception handling by hardware and that by software are explained.
Each step is described later in this reference manual.

Process	Description	See
Detection by INTIF/CPU	The INTIF/CPU detects the exception request.	Section 1.2.1
⇩		
Handling by CPU	The CPU handles the exception request.	Section 1.2.2
⇩		
Branch to ISR	The CPU branches to the corresponding interrupt service routine (ISR).	Section 1.2.2
⇩		
Execution of ISR	Necessary processing is executed	Section 1.2.3
⇩		
Return from exception	The CPU branches to another ISR or returns to the previous program.	Section 1.2.4

1.2.1. Exception Request and Detection

(1) Exception Occurrence

Exception sources include instruction execution by the CPU, memory accesses, and interrupt requests from external interrupt pins or peripheral functions.
An exception by the instruction execution occurs when the CPU executes an instruction that causes an exception or when an error condition occurs during instruction execution.
An exception also occurs by an instruction fetch from the Execute Never (XN) region or an access violation to the Fault region.
The request of the exception by the external interrupt terminal or the peripheral function occurs by each functional factor. Regarding to the interrupt which connected via INTIF, the setup of the Interrupt Control Register is needed. For details, refer to the chapter, "4 Interrupts".

(2) Exception Detection

If multiple exceptions occur simultaneously, the CPU takes the exception with the highest priority.
Table 1.1 shows the priority of exceptions. "Configurable" means that you can assign a priority level to that exception. Memory Management, Bus Fault and Usage Fault exceptions can be enabled or disabled. If a disabled exception occurs, it is handled as Hard Fault.

Table 1.1 Exception Types and Priority

Exception Type	Priority	Description	Offset
Reset	-3(highest)	Reset pin, POR, PORF, OFD, SIWDT, LVD, STOP2, SYSRESETREQ, LOCKUP signal	0x00
Non-maskable Interrupt	-2	SIWDT, LVD	0x08
Hard Fault	-1	Fault that cannot activate because a higher priority fault is being handled or it is disabled	0x0C
Memory Management	Configurable	Exception from the Memory Protection Unit (MPU) Instruction fetch from the Execute Never (XN) region	0x10
Bus Fault	Configurable	Access violation to the Hard Fault region of the memory map	0x14
Usage Fault	Configurable	Undefined instruction execution or other faults related to instruction execution	0x18
Reserved	-		0x1C to 0x28
SVCall	Configurable	System service call with SVC instruction	0x2C
Debug Monitor	Configurable	Debug monitor when the CPU is not faulting	0x30
Reserved	-		0x34
PendSV	Configurable	Pending system service request	0x38
SysTick	Configurable	Notification from system timer	0x3C
External Interrupt	Configurable	External interrupt pin or peripheral function (Note)	0x40

Note: External interrupts have different sources and numbers in each product. For details, see "4.4. List of Interrupt Factors".

(3) Priority Setting

- Priority Level

  The external interrupt priority is set to the Interrupt Priority Register and other exceptions are set to <PRI_n> bit in the System Handler Priority Register.
  The configuration <PRI_n> can be changed, and the number of bits required for setting the priority varies from 3 bits to 8 bits depending on products. Thus, the range of priority values you can specify is different depending on products.
  In the case of 8-bit configuration, the priority can be configured in the range from 0 to 255. The highest priority is "0". If multiple elements with the same priority exist, the smaller the number, the higher the priority becomes.

  <PRI_n[7:0]> bit is defined as the upper 4-bit configuration with TMPM4G group(1) products. The priority can be configured in the range from 0 to 15.

- Priority Grouping

  The priority group can be split into groups. By setting the <PRIGROUP> of the Application Interrupt and Reset Control Register, <PRI_n> can be divided into the pre-emption priority and the sub priority.
  A priority is compared with the pre-emption priority. If the priority is the same as the pre-emption priority, then it is compared with the sub priority. If the sub priority is the same as the priority, the smaller the exception number, the higher the priority.
  The Table 1.2 shows the priority group setting. The pre-emption priority and the sub priority in the table are the number in the case that <PRI_n> is defined as an 8-bit configuration.

Table 1.2 Priority grouping setting

<PRIGROUP[2:0]> setting	<PRI_n[7:0]>		Number of pre-emption priorities	Number of sub priorities
	Pre-emption field	Sub priority field		
000	[7:1]	[0]	128	2
001	[7:2]	[1:0]	64	4
010	[7:3]	[2:0]	32	8
011	[7:4]	[3:0]	16	16
100	[7:5]	[4:0]	8	32
101	[7:6]	[5:0]	4	64
110	[7]	[6:0]	2	128
111	None	[7:0]	1	256

Note: If the configuration of <PRI_n> is less than 8 bits, the lower bit is "0". For the example in the case of 4-bit configuration, the priority is set as <PRI_n [7:4]> and <PRI_n[3:0]> is "0000".

1.2.2. Exception Handling and Branch to Interrupt Service Routine (Pre-emption)

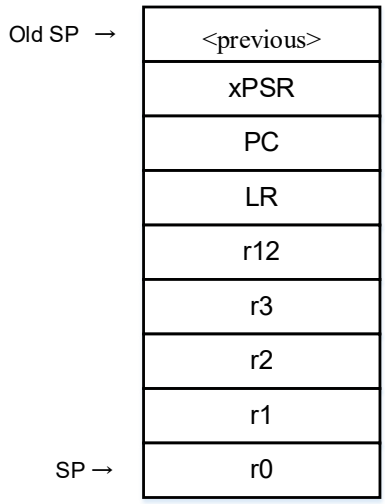
When an exception occurs, the CPU suspends the currently executing process and branches to the interrupt service routine. This is called "pre-emption".

(1) Stacking

When the CPU detects an exception, it pushes the contents of the following eight registers to the stack in the following order:

1. Program Counter (PC)
2. Program Status Register (xPSR)
3. r0 to r3
4. r12
5. Link Register (LR)

The SP is decremented by eight words by the completion of the stack push. The following shows the state of the stack after the register contents have been pushed.



(2) Fetching an ISR

The CPU performs the evacuation of the register. In addition, the CPU performs instruction fetch of the interrupt service routine at the same time.

Prepare a vector table containing the top addresses of ISRs for each exception. After reset, the vector table is located at address 0x00000000 in the Code area. By setting the Vector Table Offset Register, you can place the vector table at any address in the Code or SRAM space.
The vector table should also contain the initial value of the main stack.

(3) Late-arriving

If the CPU detects a higher priority exception before executing the ISR for a previous exception, the CPU handles the higher priority exception first. This is called "late-arriving".

A late-arriving exception causes the CPU to fetch a new vector address for branching to the corresponding ISR, but the CPU does not newly push the register contents to the stack.

(4) Vector Table

The vector table is configured as shown below.
You must always set the first four words (stack top address, reset ISR address, NMI ISR address, and Hard Fault ISR address). Set ISR addresses for other exceptions if necessary.

For other exceptions, you should prepare the ISR addresses if necessary.

Offset	Exception	Contents	Setting
0x00	Reset	Initial value of the main stack	Required
0x04	Reset	ISR address	Required
0x08	Non-maskable Interrupt	ISR address	Required
0x0C	Hard Fault	ISR address	Required
0x10	Memory Management	ISR address	Optional
0x14	Bus Fault	ISR address	Optional
0x18	Usage Fault	ISR address	Optional
0x1C to 0x28	Reserved	-	
0x2C	SVCall	ISR address	Optional
0x30	Debug Monitor	ISR address	Optional
0x34	Reserved	-	
0x38	PendSV	ISR address	Optional
0x3C	SysTick	ISR address	Optional
0x40	External Interrupt	ISR address	Optional

1.2.3. Executing an ISR

An ISR performs necessary processing for the corresponding exception. ISRs must be prepared by the user.

An ISR may need to include code for clearing the interrupt request so that the same interrupt will not occur again upon return to normal program execution.

For details about interrupt handling, see "4 Interrupts".

If a higher priority exception occurs during ISR execution for the current exception, the CPU abandons the currently executing ISR and services the newly detected exception.

1.2.4. Exception Exit

(1) Execution after Returning from ISR

When returning from an ISR, the CPU takes one of the following actions:

- Tail-chaining
  If a pending exception exists and there are no stacked exceptions or the pending exception has higher priority than all stacked exceptions, the CPU returns to the ISR of the pending exception.
  In this case, the CPU skips the pop of eight registers and push of eight registers when exiting one ISR and entering another. This is called "tail-chaining".

- Returning to the last stacked ISR
  If there are no pending exceptions or if the highest priority stacked exception is of higher priority than the highest priority pending exception, the CPU returns to the last stacked ISR.

- Returning to the previous program
  If there are no pending or stacked exceptions, the CPU returns to the previous program.

(2) Exception Exit Sequence

When returning from an ISR, the CPU performs the following operations:

- Pop eight registers
  Pop eight registers (PC, xPSR, r0 to r3, r12, and LR) from the stack and adjust the SP.

- Lord current active interrupt number
  Loads the current active interrupt number from the stacked xPSR. The CPU uses this to track which interrupt to return to.

- Select SP
  If returning to an exception (Handler Mode), SP is SP_main. If returning to Thread Mode, SP can be SP_main or SP_process.

2. Reset Exception

Reset exceptions are generated from the following sources.
Use the ***[RLMRSTFLGn]*** of the Reset Flag Register to identify the source of a reset.

- Reset exception by external reset pin
  A reset exception occurs when an external reset pin changes from "Low" to "High".

- Reset exception by POR
  A reset exception occurs by POR. For details, refer to Reference Manual "Clock Control and Operation Mode".

- Reset exception by OFD
  The OFD has a reset generating feature. For details, refer to Reference Manual "Oscillation Frequency Detector".

- Reset exception by SIWDT
  The SIWDT has a reset generating feature. For details, refer to Reference Manual "Clock Selective Watchdog Timer".

- Reset exception by LVD
  The LVD has a reset generating feature. For details, refer to Reference Manual "Voltage Detector Circuit".

- Reset exception by PORF
  A reset exception occurs by PORF. For details, refer to Reference Manual "Clock Control and Operation Mode ".

- Reset exception by STOP2 mode release
  A reset exception occurs when releasing STOP2 mode. For details, refer to Reference Manual "Clock Control and Operation Mode".

- Reset exception by <SYSRESETREQ>
  A reset can be generated by setting the <SYSRESETREQ> bit in the NVIC's Application Interrupt and Reset Control Register.

- Reset exception by LOCKUP signal
  A reset can be generated by the LOCKUP signal which can be output from the CPU when the un-recoverable exception occurs. For details on the LOCKUP signal, please refer to "Arm Cortex-M4 processor Technical Reference Manual".

3. SysTick

SysTick provides interrupt features using the CPU's system timer.

When you set a value in the SysTick Reload Value Register and enable the SysTick features in the SysTick Control and Status Register, the counter loads with the value set in the Reload Value Register and begins counting down. When the counter reaches "0", a SysTick exception occurs. You may be pending exceptions and use a flag to know when the timer reaches "0".

4. Interrupts

This section explains the route from which a factor and an interrupt request are transmitted, and a required setup.

4.1. Non-maskable Interrupt (NMI)

Non-maskable interrupts are generated from the following two sources.

- Non-maskable interrupt by SIWDT
  The SIWDT has a non-maskable interrupt generating feature. For details, refer to Reference Manual "Clock Selective Watchdog Timer".

- Non-maskable interrupt by LVD
  The LVD has a non-maskable interrupt generating feature. For details, refer to Reference Manual "Voltage Detection Circuit".

4.2. Maskable Interrupt

Please refer to Interrupt control register A / Interrupt control register B of the "4.4. List of Interrupt Factors" for the factors of the maskable interrupts.

4.3. Interrupt Request

The CPU is notified of interrupt requests by the interrupt signal from each interrupt factor. It sets priority on interrupts and handles an interrupt request with the highest priority.

4.3.1. Interrupt Route

The interrupt is available for the cancellation from a low power consumption mode, and a route varies according to a factor.

Figure 4.1 shows the interrupt transfer route diagram and Table 4.1 shows the explanation of each interrupt transfer route.

- The interrupt that is releasable from IDLE, STOP1, STOP2 mode

  Interrupt which can be canceled of IDLE, STOP1, and the STOP2 mode is controlled by the Interrupt Control Register A in INTIF via INTIF, and is notified to CPU. (Route A, B, C)

- The interrupt that is releasable from IDLE, STOP1 mode

  Interrupt which can be canceled of IDLE and the STOP1 mode is controlled by the Interrupt Control Register B in INTIF via INTIF, and is notified to CPU. (Route D, E, F)

- The interrupt that is releasable from IDLE mode

  Although some factors of the interrupt which can be canceled of IDLE mode are controlled by the Interrupt Control Register B via INTIF (Route G), other factors are notified to CPU directly (Route H) not passing through INTIF.

When the interrupt factor that goes by way of INTIF regardless of low power consumption mode cancellation is used, setting of Interrupt Control Register A or B is necessary.

Please refer to the chapter of "Release Sources for Low Power Consumption Mode" of the reference manual "Clock Control and Operation Mode" for the details of a low-power-consumption mode release factor.

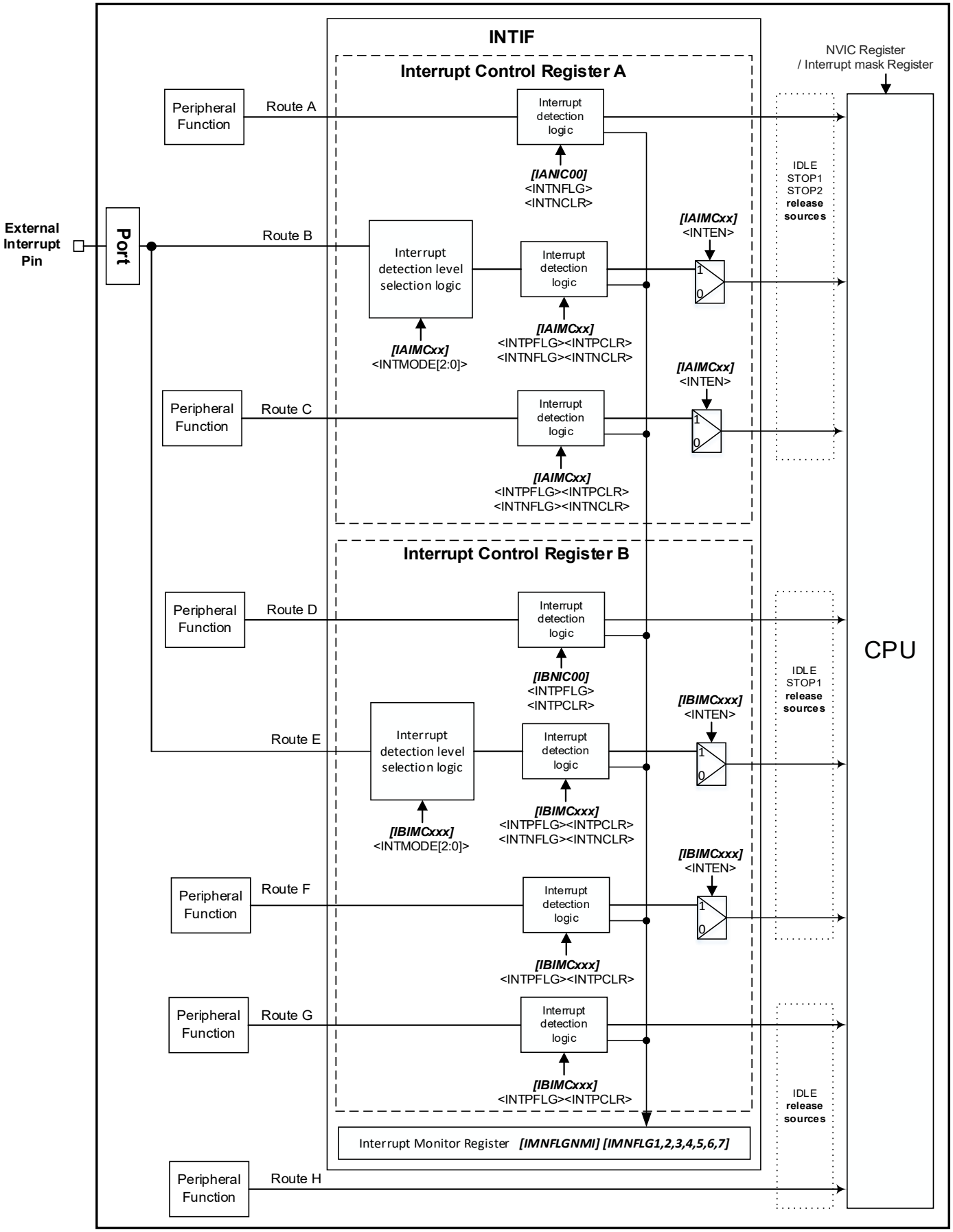


Figure 4.1 Interrupt transfer route diagram

Table 4.1 Explanation of each interrupt transfer route

Route	Interrupt No.	Interrupt Request	Route Description
A	-	LVD Interrupt	It is a non-maskable interrupt. It is a route input into CPU via INTIF. An interrupt release setup is carried out by Interrupt Control Register A (***[IANIC00]***).
B	00 to 15	External interrupts 00 to 15	An interrupt request from a port is input into CPU via INTIF. Selection of Interrupt detection level, Interrupt release, and permission/prohibition of Interrupt request are set up by Interrupt Control Register A (***[IAIMCxx]***) for each factor.
C	16	RTC interrupt	It is a route input into CPU via INTIF. Interrupt release and permission/prohibition of Interrupt request are set up by Interrupt Control Register A (***[IAIMCxx]***).
	17, 18	CEC ch0 reception interrupt CEC ch0 transmission interrupt	
	19, 20, 21	ISD interrupt A, B, C	
	22, 23	RMC ch0 Remote controller interrupt RMC ch1 Remote controller interrupt	
	24	LTTMR ch0 interrupt	
D	-	WDT Interrupt	It is a non-maskable interrupt. It is a route input into CPU via INTIF. An interrupt release setup is carried out by Interrupt Control Register B (***[IBNIC00]***).
E	N/A	N/A	N/A
F	30 to 57, 168 to 169, 171 to 173	T32A timer interrupt	It is a route input into CPU via INTIF. Interrupt release and permission/prohibition of Interrupt request are set up by Interrupt Control Register B (***[IBIMCxxx]***).
	139, 140	MDMAC unit A buss error interrupt MDMAC unit A descriptor error interrupt	
G	N/A	N/A	N/A
H	170	T32A ch14 Timer C match, overflow, and underflow interrupt	It is the route where an interrupt request is directly input into CPU, not passing through INTIF.
	174	MDMAC unit A descriptor completion interrupt	
	25 to 29, 58 to 136, 141 to 155	Other interrupts (Note)	

Note: For the details of "Other interrupts", refer to "4.4. List of Interrupt Factors".

4.3.2. Interrupt Request Generation

An interrupt request is generated from an external interrupt pin or peripheral function which are assigned as interrupt request sources, or by setting the relevant bit of NVIC's Interrupt Set-Pending Register for interrupt request source.

- Interrupt from external interrupt pin
  Set the port control register so that the external pin can perform as an interrupt function pin.
- Interrupt from peripheral function
  Set the peripheral function to make it possible to output interrupt requests.
  See the chapter of each peripheral function for details.
- By setting Interrupt Set-Pending Register (forced pending)
  An interrupt request can be forced to be generated by setting the relevant bit of the Interrupt Set-Pending Register of NVIC.

CPU will recognize the "High" level of the interrupt request as an interrupt.

4.3.3. Monitor of the Interrupt Request

INTIF has the interrupt monitor flags. It can know that the interrupt request has occurred by monitoring the flag. If one request source is representing several interrupt requests, Interrupt Monitor Register can be used to identify the actual interrupt request source.
For detail, please refer to "4.4. List of Interrupt Factors".

4.3.4. Transmission of Interrupt Request

An interrupt request which is not passing through the Interrupt Control Register will be directly input to the CPU. The interrupts connected to the CPU through INTIF, which are used as interrupt request sources for releasing the low power consumption mode, will need proper setting of the Interrupt Control Register in INTIF. An "High" level interrupt signal will be sent to the CPU, when the interrupt is used to release the low power consumption mode.
Please set up an interrupt detection level and the interrupt enable/disable by INTIF.
By the way, please be cautious about an external interrupt as in the next section.

4.3.5. Precautions When Using External Interrupt Pins

When you use external interrupt, please care about the following points so that an unexpected interrupt does not occur.

If input is disabled (***[PxIE]***<PxmIE>=0), inputs from external interrupt pins are "Low". When the <INTMODE> bit of Interrupt Control Register A (***[IAIMCxx]***) is "Low", input signals from the external interrupt pins are sent to the CPU as is. Since the CPU recognizes "Low" input as an interrupt, interrupts occur if corresponding interrupts are enabled by the CPU. The interrupt pins should be "High" and the inputs should be enabled. Then the interrupts should be enabled by the CPU.

4.4. List of Interrupt Factors

Table 4.2 shows the list of interrupt factors of non-maskable interrupts. The setting for clearing the NMI sources can be done by Interrupt Control Registers A and B.

Table 4.2 List of Interrupt Factors (Non-maskable Interrupt)

Interrupt Source	Interrupt Request	Interrupt Control Register	Interrupt Monitor Register
INTLVD	LVD interrupt	***[IANIC00]***	***[IMNFLGNMI]*** <INT000FLG>
INTWDT0	WDT interrupt	***[IBNIC00]***	***[IMNFLGNMI]*** <INT016FLG>

Table 4.3 shows the list of interrupt factors of Interrupt Control Register A. These interrupt factors can be the sources for releasing the low power consumption mode. The Interrupt Control Register A will perform several setting for detecting the release of the low power consumption mode, and interrupt detection enable/disable.

Table 4.3 List of Interrupt Factors (Interrupt Control Register A) (1/2)

Interrupt No.	Interrupt Source	Interrupt Request	Interrupt Control Register	Interrupt Monitor Register
0	INT00	External interrupt 00a	***[IAIMC00]***	***[IMNFLG1]*** <INT032FLG>
		External interrupt 00b	***[IAIMC01]***	***[IMNFLG1]*** <INT033FLG>
1	INT01	External interrupt 01a	***[IAIMC02]***	***[IMNFLG1]*** <INT034FLG>
		External interrupt 01b	***[IAIMC03]***	***[IMNFLG1]*** <INT035FLG>
2	INT02	External interrupt 02a	***[IAIMC04]***	***[IMNFLG1]*** <INT036FLG>
		External interrupt 02b	***[IAIMC05]***	***[IMNFLG1]*** <INT037FLG>
3	INT03	External interrupt 03a	***[IAIMC06]***	***[IMNFLG1]*** <INT038FLG>
		External interrupt 03b	***[IAIMC07]***	***[IMNFLG1]*** <INT039FLG>
4	INT04	External interrupt 04a	***[IAIMC08]***	***[IMNFLG1]*** <INT040FLG>
		External interrupt 04b	***[IAIMC09]***	***[IMNFLG1]*** <INT041FLG>
5	INT05	External interrupt 05a	***[IAIMC10]***	***[IMNFLG1]*** <INT042FLG>
		External interrupt 05b	***[IAIMC11]***	***[IMNFLG1]*** <INT043FLG>
6	INT06	External interrupt 06a	***[IAIMC12]***	***[IMNFLG1]*** <INT044FLG>
		External interrupt 06b	***[IAIMC13]***	***[IMNFLG1]*** <INT045FLG>
7	INT07	External interrupt 07a	***[IAIMC14]***	***[IMNFLG1]*** <INT046FLG>
		External interrupt 07b	***[IAIMC15]***	***[IMNFLG1]*** <INT047FLG>

Table 4.4 List of Interrupt Factors (Interrupt Control Register A) (2/2)

Interrupt No.	Interrupt Source	Interrupt Request	Interrupt Control Register	Interrupt Monitor Register
8	INT08	External interrupt 08a	***[IAIMC16]***	***[IMNFLG1]*** <INT048FLG>
		External interrupt 08b	***[IAIMC17]***	***[IMNFLG1]*** <INT049FLG>
9	INT09	External interrupt 09a	***[IAIMC18]***	***[IMNFLG1]*** <INT050FLG>
		External interrupt 09b	***[IAIMC19]***	***[IMNFLG1]*** <INT051FLG>
10	INT10	External interrupt 10a	***[IAIMC20]***	***[IMNFLG1]*** <INT052FLG>
		External interrupt 10b	***[IAIMC21]***	***[IMNFLG1]*** <INT053FLG>
11	INT11	External interrupt 11a	***[IAIMC22]***	***[IMNFLG1]*** <INT054FLG>
		External interrupt 11b	***[IAIMC23]***	***[IMNFLG1]*** <INT055FLG>
12	INT12	External interrupt 12a	***[IAIMC24]***	***[IMNFLG1]*** <INT056FLG>
		External interrupt 12b	***[IAIMC25]***	***[IMNFLG1]*** <INT057FLG>
13	INT13	External interrupt 13a	***[IAIMC26]***	***[IMNFLG1]*** <INT058FLG>
		External interrupt 13b	***[IAIMC27]***	***[IMNFLG1]*** <INT059FLG>
14	INT14	External interrupt 14a	***[IAIMC28]***	***[IMNFLG1]*** <INT060FLG>
		External interrupt 14b	***[IAIMC29]***	***[IMNFLG1]*** <INT061FLG>
15	INT15	External interrupt 15a	***[IAIMC30]***	***[IMNFLG1]*** <INT062FLG>
		External interrupt 15b	***[IAIMC31]***	***[IMNFLG1]*** <INT063FLG>
16	INTRTC	RTC interrupt	***[IAIMC49]***	***[IMNFLG2]*** <INT081FLG>
17	INTCEC0RX	CEC ch0 reception interrupt	***[IAIMC50]***	***[IMNFLG2]*** <INT082FLG>
18	INTCEC0TX	CEC ch0 transmission interrupt	***[IAIMC51]***	***[IMNFLG2]*** <INT083FLG>
19	INTISDA	ISD unit A interrupt	***[IAIMC52]***	***[IMNFLG2]*** <INT084FLG>
20	INTISDB	ISD unit B interrupt	***[IAIMC53]***	***[IMNFLG2]*** <INT085FLG>
21	INTISDC	ISD unit C interrupt	***[IAIMC54]***	***[IMNFLG2]*** <INT086FLG>
22	INTRMC0	RMC ch0 Remote controller interrupt	***[IAIMC55]***	***[IMNFLG2]*** <INT087FLG>
23	INTRMC1	RMC ch1 Remote controller interrupt	***[IAIMC56]***	***[IMNFLG2]*** <INT088FLG>
24	INTLTTMR0	LTTMR ch0 interrupt	***[IAIMC57]***	***[IMNFLG2]*** <INT089FLG>

The factor list of the Interrupt Control Register B is shown in Table 4.5to Table 4.12. The interrupt detection enable/disable is set for a part of interrupts by Interrupt Control Register B.

Table 4.5 List of Interrupt Factors (Interrupt Control Register B) (1/9)

Interrupt No.	Interrupt Source	Interrupt Request	Interrupt Control Register	Interrupt Monitor Register
25	INTHDMAATC	HDMA unit A transfer completion		
26	INTHDMAAERR	HDMA unit A transfer error		
27	INTHDMABTC	HDMA unit B transfer completion		
28	INTHDMABERR	HDMA unit B transfer error		
29	INTMDMAATC	MDMA unit A transfer completion		
30	INTT32A00_A_CT	T32A ch0 Timer A match, overflow, and underflow	***[IBIMC000]***	***[IMNFLG3]*** <INT096FLG>
		T32A ch0 Timer A capture 0	***[IBIMC001]***	***[IMNFLG3]*** <INT097FLG>
		T32A ch0 Timer A capture 1	***[IBIMC002]***	***[IMNFLG3]*** <INT098FLG>
		T32A ch0 Timer C match, overflow, and underflow	***[IBIMC006]***	***[IMNFLG3]*** <INT102FLG>
31	INTT32A00_B_C01_CPC	T32A ch0 Timer B match, overflow, and underflow	***[IBIMC003]***	***[IMNFLG3]*** <INT099FLG>
		T32A ch0 Timer B capture 0	***[IBIMC004]***	***[IMNFLG3]*** <INT100FLG>
		T32A ch0 Timer B capture 1	***[IBIMC005]***	***[IMNFLG3]*** <INT101FLG>
		T32A ch0 Timer C capture 0	***[IBIMC007]***	***[IMNFLG3]*** <INT103FLG>
		T32A ch0 Timer C capture 1	***[IBIMC008]***	***[IMNFLG3]*** <INT104FLG>
		T32A ch0 Timer C pulse count	***[IBIMC009]***	***[IMNFLG3]*** <INT105FLG>
32	INTT32A01_A_CT	T32A ch1 Timer A match, overflow, and underflow	***[IBIMC010]***	***[IMNFLG3]*** <INT106FLG>
		T32A ch1 Timer A capture 0	***[IBIMC011]***	***[IMNFLG3]*** <INT107FLG>
		T32A ch1 Timer A capture 1	***[IBIMC012]***	***[IMNFLG3]*** <INT108FLG>
		T32A ch1 Timer C match, overflow, and underflow	***[IBIMC016]***	***[IMNFLG3]*** <INT112FLG>
33	INTT32A01_B_C01_CPC	T32A ch1 Timer B match, overflow, and underflow	***[IBIMC013]***	***[IMNFLG3]*** <INT109FLG>
		T32A ch1 Timer B capture 0	***[IBIMC014]***	***[IMNFLG3]*** <INT110FLG>
		T32A ch1 Timer B capture 1	***[IBIMC015]***	***[IMNFLG3]*** <INT111FLG>
		T32A ch1 Timer C capture 0	***[IBIMC017]***	***[IMNFLG3]*** <INT113FLG>
		T32A ch1 Timer C capture 1	***[IBIMC018]***	***[IMNFLG3]*** <INT114FLG>
		T32A ch1 Timer C pulse count	***[IBIMC019]***	***[IMNFLG3]*** <INT115FLG>

Table 4.6 List of Interrupt Factors (Interrupt Control Register B) (2/9)

Interrupt No.	Interrupt Source	Interrupt Request	Interrupt Control Register	Interrupt Monitor Register
34	INTT32A02_A_CT	T32A ch2 Timer A match, overflow, and underflow	***[IBIMC020]***	***[IMNFLG3]*** <INT116FLG>
		T32A ch2 Timer A capture 0	***[IBIMC021]***	***[IMNFLG3]*** <INT117FLG>
		T32A ch2 Timer A capture 1	***[IBIMC022]***	***[IMNFLG3]*** <INT118FLG>
		T32A ch2 Timer C match, overflow, and underflow	***[IBIMC026]***	***[IMNFLG3]*** <INT122FLG>
35	INTT32A02_B_C01_CPC	T32A ch2 Timer B match, overflow, and underflow	***[IBIMC023]***	***[IMNFLG3]*** <INT119FLG>
		T32A ch2 Timer B capture 0	***[IBIMC024]***	***[IMNFLG3]*** <INT120FLG>
		T32A ch2 Timer B capture 1	***[IBIMC025]***	***[IMNFLG3]*** <INT121FLG>
		T32A ch2 Timer C capture 0	***[IBIMC027]***	***[IMNFLG3]*** <INT123FLG>
		T32A ch2 Timer C capture 1	***[IBIMC028]***	***[IMNFLG3]*** <INT124FLG>
		T32A ch2 Timer C pulse count	***[IBIMC029]***	***[IMNFLG3]*** <INT125FLG>
36	INTT32A03_A_CT	T32A ch3 Timer A match, overflow, and underflow	***[IBIMC030]***	***[IMNFLG3]*** <INT126FLG>
		T32A ch3 Timer A capture 0	***[IBIMC031]***	***[IMNFLG3]*** <INT127FLG>
		T32A ch3 Timer A capture 1	***[IBIMC032]***	***[IMNFLG4]*** <INT128FLG>
		T32A ch3 Timer C match, overflow, and underflow	***[IBIMC036]***	***[IMNFLG4]*** <INT132FLG>
37	INTT32A03_B_C01_CPC	T32A ch3 Timer B match, overflow, and underflow	***[IBIMC033]***	***[IMNFLG4]*** <INT129FLG>
		T32A ch3 Timer B capture 0	***[IBIMC034]***	***[IMNFLG4]*** <INT130FLG>
		T32A ch3 Timer B capture 1	***[IBIMC035]***	***[IMNFLG4]*** <INT131FLG>
		T32A ch3 Timer C capture 0	***[IBIMC037]***	***[IMNFLG4]*** <INT133FLG>
		T32A ch3 Timer C capture 1	***[IBIMC038]***	***[IMNFLG4]*** <INT134FLG>
		T32A ch3 Timer C pulse count	***[IBIMC039]***	***[IMNFLG4]*** <INT135FLG>
38	INTT32A04_A_CT	T32A ch4 Timer A match, overflow, and underflow	***[IBIMC040]***	***[IMNFLG4]*** <INT136FLG>
		T32A ch4 Timer A capture 0	***[IBIMC041]***	***[IMNFLG4]*** <INT137FLG>
		T32A ch4 Timer A capture 1	***[IBIMC042]***	***[IMNFLG4]*** <INT138FLG>
		T32A ch4 Timer C match, overflow, and underflow	***[IBIMC046]***	***[IMNFLG4]*** <INT142FLG>

Table 4.7 List of Interrupt Factors (Interrupt Control Register B) (3/9)

Interrupt No.	Interrupt Source	Interrupt Request	Interrupt Control Register	Interrupt Monitor Register
39	INTT32A04_B_C01_CPC	T32A ch4 Timer B match, overflow, and underflow	***[IBIMC043]***	***[IMNFLG4]*** <INT139FLG>
		T32A ch4 Timer B capture 0	***[IBIMC044]***	***[IMNFLG4]*** <INT140FLG>
		T32A ch4 Timer B capture 1	***[IBIMC045]***	***[IMNFLG4]*** <INT141FLG>
		T32A ch4 Timer C capture 0	***[IBIMC047]***	***[IMNFLG4]*** <INT143FLG>
		T32A ch4 Timer C capture 1	***[IBIMC048]***	***[IMNFLG4]*** <INT144FLG>
		T32A ch4 Timer C pulse count	***[IBIMC049]***	***[IMNFLG4]*** <INT145FLG>
40	INTT32A05_A_CT	T32A ch5 Timer A match, overflow, and underflow	***[IBIMC050]***	***[IMNFLG4]*** <INT146FLG>
		T32A ch5 Timer A capture 0	***[IBIMC051]***	***[IMNFLG4]*** <INT147FLG>
		T32A ch5 Timer A capture 1	***[IBIMC052]***	***[IMNFLG4]*** <INT148FLG>
		T32A ch5 Timer C match, overflow, and underflow	***[IBIMC056]***	***[IMNFLG4]*** <INT152FLG>
41	INTT32A05_B_C01_CPC	T32A ch5 Timer B match, overflow, and underflow	***[IBIMC053]***	***[IMNFLG4]*** <INT149FLG>
		T32A ch5 Timer B capture 0	***[IBIMC054]***	***[IMNFLG4]*** <INT150FLG>
		T32A ch5 Timer B capture 1	***[IBIMC055]***	***[IMNFLG4]*** <INT151FLG>
		T32A ch5 Timer C capture 0	***[IBIMC057]***	***[IMNFLG4]*** <INT153FLG>
		T32A ch5 Timer C capture 1	***[IBIMC058]***	***[IMNFLG4]*** <INT154FLG>
		T32A ch5 Timer C pulse count	***[IBIMC059]***	***[IMNFLG4]*** <INT155FLG>
42	INTT32A06_A_CT	T32A ch6 Timer A match, overflow, and underflow	***[IBIMC060]***	***[IMNFLG4]*** <INT156FLG>
		T32A ch6 Timer A capture 0	***[IBIMC061]***	***[IMNFLG4]*** <INT157FLG>
		T32A ch6 Timer A capture 1	***[IBIMC062]***	***[IMNFLG4]*** <INT158FLG>
		T32A ch6 Timer C match, overflow, and underflow	***[IBIMC066]***	***[IMNFLG5]*** <INT162FLG>
43	INTT32A06_B_C01_CPC	T32A ch6 Timer B match, overflow, and underflow	***[IBIMC063]***	***[IMNFLG4]*** <INT159FLG>
		T32A ch6 Timer B capture 0	***[IBIMC064]***	***[IMNFLG5]*** <INT160FLG>
		T32A ch6 Timer B capture 1	***[IBIMC065]***	***[IMNFLG5]*** <INT161FLG>
		T32A ch6 Timer C capture 0	***[IBIMC067]***	***[IMNFLG5]*** <INT163FLG>
		T32A ch6 Timer C capture 1	***[IBIMC068]***	***[IMNFLG5]*** <INT164FLG>
		T32A ch6 Timer C pulse count	***[IBIMC069]***	***[IMNFLG5]*** <INT165FLG>

Table 4.8 List of Interrupt Factors (Interrupt Control Register B) (4/9)

Interrupt No.	Interrupt Source	Interrupt Request	Interrupt Control Register	Interrupt Monitor Register
44	INTT32A07_A_CT	T32A ch7 Timer A match, overflow, and underflow	***[IBIMC070]***	***[IMNFLG5]*** <INT166FLG>
		T32A ch7 Timer A capture 0	***[IBIMC071]***	***[IMNFLG5]*** <INT167FLG>
		T32A ch7 Timer A capture 1	***[IBIMC072]***	***[IMNFLG5]*** <INT168FLG>
		T32A ch7 Timer C match, overflow, and underflow	***[IBIMC076]***	***[IMNFLG5]*** <INT172FLG>
45	INTT32A07_B_C01_CPC	T32A ch7 Timer B match, overflow, and underflow	***[IBIMC073]***	***[IMNFLG5]*** <INT169FLG>
		T32A ch7 Timer B capture 0	***[IBIMC074]***	***/[IMNFLG5]*** <INT170FLG>
		T32A ch7 Timer B capture 1	***[IBIMC075]***	***[IMNFLG5]*** <INT171FLG>
		T32A ch7 Timer C capture 0	***[IBIMC077]***	***[IMNFLG5]*** <INT173FLG>
		T32A ch7 Timer C capture 1	***[IBIMC078]***	***[IMNFLG5]*** <INT174FLG>
		T32A ch7 Timer C pulse count	***[IBIMC079]***	***[IMNFLG5]*** <INT175FLG>
46	INTT32A08_A_CT	T32A ch8 Timer A match, overflow, and underflow	***[IBIMC080]***	***[IMNFLG5]*** <INT176FLG>
		T32A ch8 Timer A capture 0	***[IBIMC081]***	***/[IMNFLG5]*** <INT177FLG>
		T32A ch8 Timer A capture 1	***[IBIMC082]***	***[IMNFLG5]*** <INT178FLG>
		T32A ch8 Timer C match, overflow, and underflow	***[IBIMC086]***	***[IMNFLG5]*** <INT182FLG>
47	INTT32A08_B_C01_CPC	T32A ch8 Timer B match, overflow, and underflow	***[IBIMC083]***	***[IMNFLG5]*** <INT179FLG>
		T32A ch8 Timer B capture 0	***[IBIMC084]***	***[IMNFLG5]*** <INT180FLG>
		T32A ch8 Timer B capture 1	***[IBIMC085]***	***[IMNFLG5]*** <INT181FLG>
		T32A ch8 Timer C capture 0	***[IBIMC087]***	***[IMNFLG5]*** <INT183FLG>
		T32A ch8 Timer C capture 1	***[IBIMC088]***	***[IMNFLG5]*** <INT184FLG>
		T32A ch8 Timer C pulse count	***[IBIMC089]***	***[IMNFLG5]*** <INT185FLG>
48	INTT32A09_A_CT	T32A ch9 Timer A match, overflow, and underflow	***[IBIMC090]***	***[IMNFLG5]*** <INT186FLG>
		T32A ch9 Timer A capture 0	***[IBIMC091]***	***[IMNFLG5]*** <INT187FLG>
		T32A ch9 Timer A capture 1	***[IBIMC092]***	***[IMNFLG5]*** <INT188FLG>
		T32A ch9 Timer C match, overflow, and underflow	***[IBIMC096]***	***[IMNFLG6]*** <INT192FLG>

Table 4.9 List of Interrupt Factors (Interrupt Control Register B) (5/9)

Interrupt No.	Interrupt Source	Interrupt Request	Interrupt Control Register	Interrupt Monitor Register
49	INTT32A09_B_C01_CPC	T32A ch9 Timer B match, overflow, and underflow	***[IBIMC093]***	***[IMNFLG5]*** <INT189FLG>
		T32A ch9 Timer B capture 0	***[IBIMC094]***	***[IMNFLG5]*** <INT190FLG>
		T32A ch9 Timer B capture 1	***[IBIMC095]***	***[IMNFLG5]*** <INT191FLG>
		T32A ch9 Timer C capture 0	***[IBIMC097]***	***[IMNFLG6]*** <INT193FLG>
		T32A ch9 Timer C capture 1	***[IBIMC098]***	***[IMNFLG6]*** <INT194FLG>
		T32A ch9 Timer C pulse count	***[IBIMC099]***	***[IMNFLG6]*** <INT195FLG>
50	INTT32A10_A_CT	T32A ch10 Timer A match, overflow, and underflow	***[IBIMC100]***	***[IMNFLG6]*** <INT196FLG>
		T32A ch10 Timer A capture 0	***[IBIMC101]***	***[IMNFLG6]*** <INT197FLG>
		T32A ch10 Timer A capture 1	***[IBIMC102]***	***[IMNFLG6]*** <INT198FLG>
		T32A ch10 Timer C match, overflow, and underflow	***[IBIMC106]***	***[IMNFLG6]*** <INT202FLG>
51	INTT32A10_B_C01_CPC	T32A ch10 Timer B match, overflow, and underflow	***[IBIMC103]***	***[IMNFLG6]*** <INT199FLG>
		T32A ch10 Timer B capture 0	***[IBIMC104]***	***[IMNFLG6]*** <INT200FLG>
		T32A ch10 Timer B capture 1	***[IBIMC105]***	***[IMNFLG6]*** <INT201FLG>
		T32A ch10 Timer C capture 0	***[IBIMC107]***	***[IMNFLG6]*** <INT203FLG>
		T32A ch10 Timer C capture 1	***[IBIMC108]***	***[IMNFLG6]*** <INT204FLG>
		T32A ch10 Timer C pulse count	***[IBIMC109]***	***[IMNFLG6]*** <INT205FLG>
52	INTT32A11_A_CT	T32A ch11 Timer A match, overflow, and underflow	***[IBIMC110]***	***[IMNFLG6]*** <INT206FLG>
		T32A ch11 Timer A capture 0	***[IBIMC111]***	***[IMNFLG6]*** <INT207FLG>
		T32A ch11 Timer A capture 1	***[IBIMC112]***	***[IMNFLG6]*** <INT208FLG>
		T32A ch11 Timer C match, overflow, and underflow	***[IBIMC116]***	***[IMNFLG6]*** <INT212FLG>
53	INTT32A11_B_C01_CPC	T32A ch11 Timer B match, overflow, and underflow	***[IBIMC113]***	***[IMNFLG6]*** <INT209FLG>
		T32A ch11 Timer B capture 0	***[IBIMC114]***	***[IMNFLG6]*** <INT210FLG>
		T32A ch11 Timer B capture 1	***[IBIMC115]***	***[IMNFLG6]*** <INT211FLG>
		T32A ch11 Timer C capture 0	***[IBIMC117]***	***[IMNFLG6]*** <INT213FLG>
		T32A ch11 Timer C capture 1	***[IBIMC118]***	***[IMNFLG6]*** <INT214FLG>
		T32A ch11 Timer C pulse count	***[IBIMC119]***	***[IMNFLG6]*** <INT215FLG>

Table 4.10 List of Interrupt Factors (Interrupt Control Register B) (6/9)

Interrupt No.	Interrupt Source	Interrupt Request	Interrupt Control Register	Interrupt Monitor Register
54	INTT32A12_A_CT	T32A ch12 Timer A match, overflow, and underflow	***[IBIMC120]***	***[IMNFLG6]*** <INT216FLG>
		T32A ch12 Timer A capture 0	***[IBIMC121]***	***[IMNFLG6]*** <INT217FLG>
		T32A ch12 Timer A capture 1	***[IBIMC122]***	***[IMNFLG6]*** <INT218FLG>
		T32A ch12 Timer C match, overflow, and underflow	***[IBIMC126]***	***[IMNFLG6]*** <INT222FLG>
55	INTT32A12_B_C01_CPC	T32A ch12 Timer B match, overflow, and underflow	***[IBIMC123]***	***[IMNFLG6]*** <INT219FLG>
		T32A ch12 Timer B capture 0	***[IBIMC124]***	***[IMNFLG6]*** <INT220FLG>
		T32A ch12 Timer B capture 1	***[IBIMC125]***	***[IMNFLG6]*** <INT221FLG>
		T32A ch12 Timer C capture 0	***[IBIMC127]***	***[IMNFLG6]*** <INT223FLG>
		T32A ch12 Timer C capture 1	***[IBIMC128]***	***[IMNFLG7]*** <INT224FLG>
		T32A ch12 Timer C pulse count	***[IBIMC129]***	***[IMNFLG7]*** <INT225FLG>
56	INTT32A13_A_CT	T32A ch13 Timer A match, overflow, and underflow	***[IBIMC130]***	***[IMNFLG7]*** <INT226FLG>
		T32A ch13 Timer A capture 0	***[IBIMC131]***	***[IMNFLG7]*** <INT227FLG>
		T32A ch13 Timer A capture 1	***[IBIMC132]***	***[IMNFLG7]*** <INT228FLG>
		T32A ch13 Timer C match, overflow, and underflow	***[IBIMC136]***	***[IMNFLG7]*** <INT232FLG>
57	INTT32A13_B_C01_CPC	T32A ch13 Timer B match, overflow, and underflow	***[IBIMC133]***	***[IMNFLG7]*** <INT229FLG>
		T32A ch13 Timer B capture 0	***[IBIMC134]***	***[IMNFLG7]*** <INT230FLG>
		T32A ch13 Timer B capture 1	***[IBIMC135]***	***[IMNFLG7]*** <INT231FLG>
		T32A ch13 Timer C capture 0	***[IBIMC137]***	***[IMNFLG7]*** <INT233FLG>
		T32A ch13 Timer C capture 1	***[IBIMC138]***	***[IMNFLG7]*** <INT234FLG>
		T32A ch13 Timer C pulse count	***[IBIMC139]***	***[IMNFLG7]*** <INT235FLG>
58	INTEMG0	A-PMD ch0 EMG interrupt		
59	INTOVV0	A-PMD ch0 OVV interrupt		
60	INTPWM0	A-PMD ch0 PWM interrupt		
61	INTT0RX	TSPI ch0 reception interrupt		
62	INTT0TX	TSPI ch0 transmission interrupt		
63	INTT0ERR	TSPI ch0 error interrupt		
64	INTT1RX	TSPI ch1 reception interrupt		
65	INTT1TX	TSPI ch1 transmission interrupt		
66	INTT1ERR	TSPI ch1 error interrupt		
67	INTT2RX	TSPI ch2 reception interrupt		
68	INTT2TX	TSPI ch2 transmission interrupt		
69	INTT2ERR	TSPI ch2 error interrupt		

Table 4.11 List of Interrupt Factors (Interrupt Control Register B) (7/9)

Interrupt No.	Interrupt Source	Interrupt Request	Interrupt Control Register	Interrupt Monitor Register
70	INTT3RX	TSPI ch3 reception interrupt		
71	INTT3TX	TSPI ch3 transmission interrupt		
72	INTT3ERR	TSPI ch3 error interrupt		
73	INTT4RX	TSPI ch4 reception interrupt		
74	INTT4TX	TSPI ch4 transmission interrupt		
75	INTT4ERR	TSPI ch4 error interrupt		
76	INTT5RX	TSPI ch5 reception interrupt		
77	INTT5TX	TSPI ch5 transmission interrupt		
78	INTT5ERR	TSPI ch5 error interrupt		
79	INTT6RX	TSPI ch6 reception interrupt		
80	INTT6TX	TSPI ch6 transmission interrupt		
81	INTT6ERR	TSPI ch6 error interrupt		
82	INTT7RX	TSPI ch7 reception interrupt		
83	INTT7TX	TSPI ch7 transmission interrupt		
84	INTT7ERR	TSPI ch7 error interrupt		
85	INTT8RX	TSPI ch8 reception interrupt		
86	INTT8TX	TSPI ch8 transmission interrupt		
87	INTT8ERR	TSPI ch8 error interrupt		
88	INTSMI0	SMI ch0 interrupt		
89	INTUART0RX	UART ch0 reception interrupt		
90	INTUART0TX	UART ch0 transmission interrupt		
91	INTUART0ERR	UART ch0 error interrupt		
92	INTUART1RX	UART ch1 reception interrupt		
93	INTUART1TX	UART ch1 transmission interrupt		
94	INTUART1ERR	UART ch1 error interrupt		
95	INTUART2RX	UART ch2 reception interrupt		
96	INTUART2TX	UART ch2 transmission interrupt		
97	INTUART2ERR	UART ch2 error interrupt		
98	INTUART3RX	UART ch3 reception interrupt		
99	INTUART3TX	UART ch3 transmission interrupt		
100	INTUART3ERR	UART ch3 error interrupt		
101	INTUART4RX	UART ch4 reception interrupt		
102	INTUART4TX	UART ch4 transmission interrupt		
103	INTUART4ERR	UART ch4 error interrupt		
104	INTUART5RX	UART ch5 reception interrupt		
105	INTUART5TX	UART ch5 transmission interrupt		
106	INTUART5ERR	UART ch5 error interrupt		
107	INTFUART0	FUART ch0 interrupt		
108	INTFUART1	FUART ch1 interrupt		
109	INTI2C0NST (Note)	I2C ch0 interrupt / EI2C ch0 status interrupt		
110	INTI2C0ATX (Note)	I2C ch0 arbitration lost detection interrupt / EI2C ch0 transmit buffer empty interrupt		
111	INTI2C0BRX (Note)	I2C ch0 bus free detection interrupt / EI2C ch0 receive buffer full interrupt		
112	INTI2C0NA	I2C ch0 NACK detection interrupt		
113	INTI2C1NST (Note)	I2C ch1 interrupt / EI2C ch1 status interrupt		
114	INTI2C1ATX (Note)	I2C ch1 arbitration lost detection interrupt / EI2C ch1 transmit buffer empty interrupt		
115	INTI2C1BRX (Note)	I2C ch1 bus free detection interrupt / EI2C ch1 receive buffer full interrupt		
116	INTI2C1NA	I2C ch1 NACK detection interrupt		

Note: Please refer to "4.4.1. Joint interruption".

Table 4.12 List of Interrupt Factors (Interrupt Control Register B) (8/9)

Interrupt No.	Interrupt Source	Interrupt Request	Interrupt Control Register	Interrupt Monitor Register
117	INTI2C2NST (Note)	I2C ch2 interrupt / EI2C ch2 status interrupt		
118	INTI2C2ATX (Note)	I2C ch2 arbitration lost detection interrupt / EI2C ch2 transmit buffer empty interrupt		
119	INTI2C2BRX (Note)	I2C ch2 bus free detection interrupt / EI2C ch2 receive buffer full interrupt		
120	INTI2C2NA	I2C ch2 NACK detection interrupt		
121	INTI2C3NST (Note)	I2C ch3 interrupt / EI2C ch3 status interrupt		
122	INTI2C3ATX (Note)	I2C ch3 arbitration lost detection interrupt / EI2C ch3 transmit buffer empty interrupt		
123	INTI2C3BRX (Note)	I2C ch3 bus free detection interrupt / EI2C ch3 receive buffer full interrupt		
124	INTI2C3NA	I2C ch3 NACK detection interrupt		
125	INTI2C4NST (Note)	I2C ch4 interrupt / EI2C ch4 status interrupt		
126	INTI2C4ATX (Note)	I2C ch4 arbitration lost detection interrupt / EI2C ch4 transmit buffer empty interrupt		
127	INTI2C4BRX (Note)	I2C ch4 bus free detection interrupt / EI2C ch4 receive buffer full interrupt		
128	INTI2C4NA	I2C ch4 NACK detection interrupt		
129	INTADACP0	ADC unit A monitor function 0 interrupt		
130	INTADACP1	ADC unit A monitor function 1 interrupt		
131	INTADATRG	ADC unit A general purpose trigger interrupt		
132	INTADASGL	ADC unit A single conversion interrupt		
133	INTADACNT	ADC unit A Continuous conversion interrupt		
134	INTADAHP	ADC unit A highest priority conversion completion interrupt		
135	INTFLDRDY	Data FLASH Ready interrupt		
136	INTFLCRDY	Code FLASH Ready interrupt		
137	Reserved			
138	Reserved			
139	INTMDMAABERR	MDMAC unit A bus error interrupt	***[IBIMC140]***	***[IMNFLG7]*** <INT236FLG>
140	INTMDMAADERR	MDMAC unit A descriptor error interrupt	***[IBIMC141]***	***[IMNFLG7]*** <INT237FLG>
141	INTI2S0SI	I2S ch0 reception data transfer request interrupt		
142	INTI2S0SIERR	I2S ch0 reception error interrupt		
143	INTI2S0SO	I2S ch0 transmission data transfer request interrupt		
144	INTI2S0SOERR	I2S ch0 transmission error interrupt		
145	INTI2S1SI	I2S ch1 reception data transfer request interrupt		
146	INTI2S1SIERR	I2S ch1 reception error interrupt		
147	INTI2S1SO	I2S ch1 transmission data transfer request interrupt		
148	INTI2S1SOERR	I2S ch1 transmission error interrupt		
149	INTFIR	FIR interrupt		
150	INTTSSI0RX	TSSI ch0 receive interrupt		
151	INTTSSI0TX	TSSI ch0 transmission interrupt		
152	INTTSSI0ERR	TSSI ch0 error interrupt		
153	INTTSSI1RX	TSSI ch1 receive interrupt		
144	INTTSSI1TX	TSSI ch1 transmission interrupt		
155	INTTSSI1ERR	TSSI ch1 error interrupt		

Note: Please refer to "4.4.1. Joint interruption".

Table 4.13 List of Interrupt Factors (Interrupt Control Register B) (9/9)

Interrupt No.	Interrupt Source	Interrupt Request	Interrupt Control Register	Interrupt Monitor Register
156	Reserved			
157	Reserved			
158	Reserved			
159	Reserved			
160	Reserved			
161	Reserved			
162	Reserved			
163	Reserved			
164	Reserved			
165	Reserved			
166	Reserved			
167	Reserved			
168	INTT32A14_A	T32A ch14 Timer A match, overflow, and underflow	***[IBIMC145]***	***[IMNFLG7]*** <INT241FLG>
		T32A ch14 Timer A capture 0	***[IBIMC146]***	***[IMNFLG7]*** <INT242FLG>
		T32A ch14 Timer A capture 1	***[IBIMC147]***	***[IMNFLG7]*** <INT243FLG>
169	INTT32A14_B	T32A ch14 Timer B match, overflow, and underflow	***[IBIMC148]***	***[IMNFLG7]*** <INT244FLG>
		T32A ch14 Timer B capture 0	***[IBIMC149]***	***[IMNFLG7]*** <INT245FLG>
		T32A ch14 Timer B capture 1	***[IBIMC150]***	***[IMNFLG7]*** <INT246FLG>
170	INTT32A14_CT	T32A ch14 Timer C match, overflow, and underflow		
171	INTT32A15_A	T32A ch15 Timer A match, overflow, and underflow	***[IBIMC151]***	***[IMNFLG7]*** <INT247FLG>
		T32A ch15 Timer A capture 0	***[IBIMC152]***	***[IMNFLG7]*** <INT248FLG>
		T32A ch15 Timer A capture 1	***[IBIMC153]***	***[IMNFLG7]*** <INT249FLG>
172	INTT32A15_B	T32A ch15 Timer B match, overflow, and underflow	***[IBIMC154]***	***[IMNFLG7]*** <INT250FLG>
		T32A ch15 Timer B capture 0	***[IBIMC155]***	***[IMNFLG7]*** <INT251FLG>
		T32A ch15 Timer B capture 1	***[IBIMC156]***	***[IMNFLG7]*** <INT252FLG>
173	INTT32A15_C	T32A ch15 Timer C match, overflow, and underflow	***[IBIMC157]***	***[IMNFLG7]*** <INT253FLG>
		T32A ch15 Timer C capture 0	***[IBIMC158]***	***[IMNFLG7]*** <INT254FLG>
		T32A ch15 Timer C capture 1	***[IBIMC159]***	***[IMNFLG7]*** <INT255FLG>
174	INTMDMAADS	MDMAC unit A descriptor completion interrupt		

4.4.1. Joint interruption

Details of interrupts that are coupled in TMPM4G Group (1) are as follows.

Table 4.14 Joint interruption list

Interrupt No.	Joint Interrupt Source	Interrupt Source	Interrupt Request	Interrupt Control Register	Interrupt Monitor Register
109	INTI2C0NST	INTI2C0	I2C ch0 interrupt		
		INTI2C0ST	EI2C ch0 status interrupt		
110	INTI2C0ATX	INTI2C0AL	I2C ch0 arbitration lost detection interrupt		
		INTI2C0TBE	EI2C ch0 transmit buffer empty interrupt		
111	INTI2C0BRX	INTI2C0BF	I2C ch0 bus free detection interrupt		
		INTI2C0RBF	EI2C ch0 receive buffer full interrupt		
113	INTI2C1NST	INTI2C1	I2C ch1 interrupt		
		INTI2C1ST	EI2C ch1 status interrupt		
114	INTI2C1ATX	INTI2C1AL	I2C ch1 arbitration lost detection interrupt		
		INTI2C1TBE	EI2C ch1 transmit buffer empty interrupt		
115	INTI2C1BRX	INTI2C1BF	I2C ch1 bus free detection interrupt		
		INTI2C1RBF	EI2C ch1 receive buffer full interrupt		
117	INTI2C2NST	INTI2C2	I2C ch2 interrupt		
		INTI2C2ST	EI2C ch2 status interrupt		
118	INTI2C2ATX	INTI2C2AL	I2C ch2 arbitration lost detection interrupt		
		INTI2C2TBE	EI2C ch2 transmit buffer empty interrupt		
119	INTI2C2BRX	INTI2C2BF	I2C ch2 bus free detection interrupt		
		INTI2C2RBF	EI2C ch2 receive buffer full interrupt		
121	INTI2C3NST	INTI2C3	I2C ch3 interrupt		
		INTI2C3ST	EI2C ch3 status interrupt		
122	INTI2C3ATX	INTI2C3AL	I2C ch3 arbitration lost detection interrupt		
		INTI2C3TBE	EI2C ch3 transmit buffer empty interrupt		
123	INTI2C3BRX	INTI2C3BF	I2C ch3 bus free detection interrupt		
		INTI2C3RBF	EI2C ch3 receive buffer full interrupt		
125	INTI2C4NST	INTI2C4	I2C ch4 interrupt		
		INTI2C4ST	EI2C ch4 status interrupt		
126	INTI2C4ATX	INTI2C4AL	I2C ch4 arbitration lost detection interrupt		
		INTI2C4TBE	EI2C ch4 transmit buffer empty interrupt		
127	INTI2C4BRX	INTI2C4BF	I2C ch4 bus free detection interrupt		
		INTI2C4RBF	EI2C ch4 receive buffer full interrupt		

Note: Select these interrupts on each IP side. Please select only one IP.

4.5. Interrupt detection level

When using interrupt via INTIF, interrupt detection level ("Low" level / "High" level / Rising edge / Falling edge) can be selected by interrupt control register A or B. The detected interrupt is output to the CPU with a "High" level signal.
The interrupt signals which are directly transmitted from the various peripheral functions to the CPU, a "High" pulse is output to the CPU as an interrupt request.
The CPU detects the interrupt signal "High" to be an interrupt factor.

4.5.1. Precautions When Releasing the Low Power Consumption Mode

Following setting should be done when releasing STOP1/2 mode.

- The setup of the Interrupt Control Register. (***[IAIMCxx], [IBIMCxxx]***)
  - Interrupt detection level
  - Interrupt enable/disable

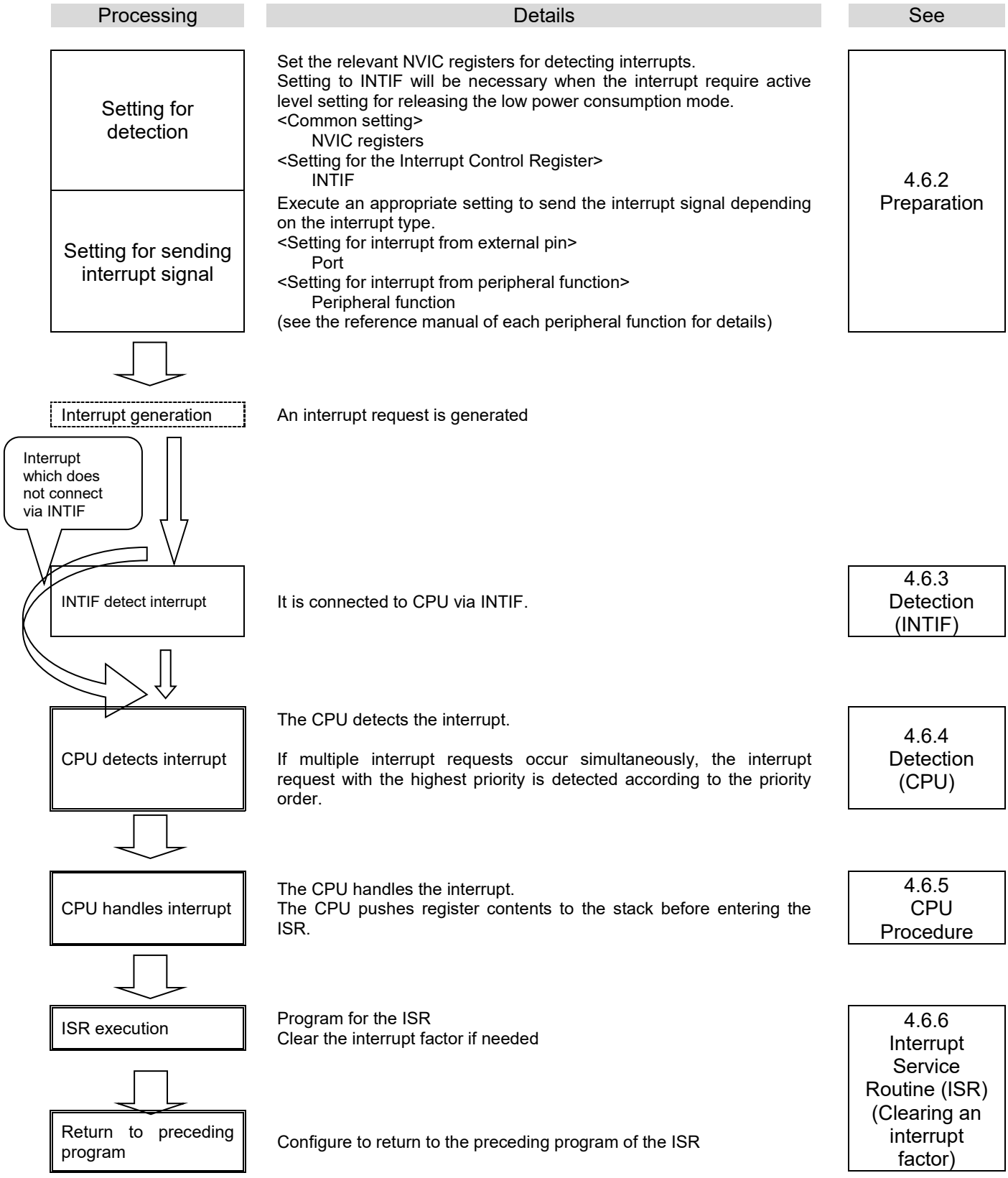
- The setup of the NVIC interrupt enabling set register. (at the time of the STOP1 mode)
  - enable/disable setup

In order to return to NORMAL mode from STOP1 mode, resume suspended instruction by jumping into interrupt after high speed clock oscillation. The operation which returns to NORMAL mode from the STOP2 mode turns on the power supply to the power supply interception domain, and is restart from the reset sequence.

4.6. Interrupt Handling

4.6.1. Flowchart

The following shows how an interrupt is handled.
The flowchart below explains the interrupt handling process by hardware and software.



4.6.2. Preparation

When preparing for an interrupt, you need to pay attention to the order of configuration to avoid any unexpected interrupt on the way.
Initiating an interrupt or changing its configuration must be implemented in the following order basically. First, disable the interrupt by the CPU. Then, configure from the farthest route from the CPU. Finally, enable the interrupt by the CPU.
To configure the INTIF, you must follow the order indicated here not to cause any unexpected interrupt. First, configure the precondition. Secondly, clear the data related to the interrupt in the INTIF and then enable the interrupt.
The following sections are listed in the order of interrupt handling and describe how to configure them.

1. Disabling interrupt by CPU
2. CPU registers setting
3. Preconfiguration (1) (Interrupt from external pin)
4. Preconfiguration (2) (Interrupt from peripheral function)
5. Preconfiguration (3) (Interrupt Set-Pending Register)
6. Configuring the INTIF
7. Enabling interrupt by CPU

(1) Disabling Interrupt by CPU

To make the CPU for not accepting any interrupt, write "1" to the corresponding bit of the ***[PRIMASK]*** register. All interrupts and exceptions other than non-maskable interrupts and hard faults can be masked.

Use "MSR" instruction to set this register.

Interrupt Mask Register		
[PRIMASK]	←	"1" (interrupt disabled)

Note 1: ***[PRIMASK]*** register cannot be modified in the user access level.
Note 2: If a fault causes when "1" is set to the ***[PRIMASK]*** register, it is treated as a hard fault.

(2) CPU Registers Setting

You can assign a priority level by writing to <PRI_n> field in an Interrupt Priority Register in the NVIC. Each interrupt factor is provided with eight bits for assigning a priority level from 0 to 255, but the number of bits actually used varies with each product. Priority level 0 is the highest priority level. If multiple sources have the same priority, the smallest-numbered interrupt factor has the highest priority.
You can assign grouping priority by using the <PRIGROUP> in the Application Interrupt and Reset Control Register.

NVIC Register		
<PRI_n>	←	"Priority"
<PRIGROUP>	←	"group priority" (This is configurable if required)

Note: "n" indicates the number of the corresponding exceptions/interrupts.
This product uses four bits for assigning a priority level.

(3) Preconfiguration (1) (Interrupt from external pin)

In order to use external interrupt pin, it is necessary to do proper setting to the port function register of the corresponding pin. Setting ***[PxIE]***<PxmIE> to "1". allows the pin to be used as the function pin and the input port.

Port Register		
[PxIE]<PxmIE>	←	"1"

Note: x: port number, m: corresponding bit of function register number. Be careful not to enable interrupts that are not used when performing interrupt setting. Also be aware of the description of "4.3.5 Precautions When Using External Interrupt Pins"

(4) Preconfiguration (2) (Interrupt from peripheral function)

The setting varies depending on the peripheral function to be used. See the reference manual of each peripheral function for details

(5) Preconfiguration (3) (Interrupt from Set-Pending Register)

To generate an interrupt by using the Interrupt Set-Pending Register, set the corresponding bit of this register to "1".

NVIC Register		
<SETPEND>	←	"1"

Note: <SETPEND>: corresponding bit.

(6) Configuring the INTIF

The interrupt by way of INTIF sets the permission of the interrupt detection in Interrupt Control Registers.

The ***[IANIC00]/[IBNIC00]/[IAIMCxx]/[IBIMCxxx]*** Registers are capable of configuring each interrupt factor. Before enabling an interrupt detection, clear the interrupt request having active level in order to avoid unexpected interrupt.
The Interrupt Control Register can clear the interrupt request currently held by clearing the interrupt flag corresponding to the interrupt request.

Interrupt Control Register		
[IAIMCxx]<INTMODE> ***[IBIMCxxx]***<INTMODE>	←	Value corresponding to the interrupt to be used (Only for the interrupt having interrupt detection level)
[IANIC00]<INTNCLR> ***[IBNIC00]***<INTPCLR> ***[IAIMCxx]***<INTPCLR><INTNCLR> ***IBIMCxxx]***<INTPCLR><INTNCLR>	←	Interrupt request clear to use
[IAIMCxx]<INTEN> ***[IBIMCxxx]***<INTEN>	←	"1" (Interrupt detection enabled)

Note: xx or xxx: number specific to the interrupt request

(7) Enabling Interrupt by CPU

Enable the interrupt by the CPU as shown below.
Clear the suspended interrupt in the Interrupt Clear-Pending Register. Enable the intended interrupt with the Interrupt Set-Enable Register. Each bit of the register is assigned to a single interrupt factor.
Writing "1" to the corresponding bit of the Interrupt Clear-Pending Register clears the suspended interrupt. Writing "1" to the corresponding bit of the Interrupt Set-Enable Register enables the intended interrupt.
To generate interrupts in the Interrupt Set-Pending Register setting, factors to trigger interrupts are lost if pending interrupts are cleared. Thus, this operation is not necessary.
At the end, ***[PRIMASK]*** register is zero cleared.

NVIC Register		
<CLRPEND>	←	"1"
<SETENA>	←	"1"
Interrupt Mask Register		
[PRIMASK]	←	"0"

Note 1: <CLRPEND>,<SETENA>: corresponding bit
Note 2: ***[PRIMASK]*** Register cannot be modified by the user access level;

4.6.3. Detection (INTIF)

When the INTIF detects an interrupt request, it sends the interrupt signal in "High" level to the CPU.

INTIF has the functions of the interrupt detection level selection logic, the functions of interrupt detection logic, and the function of the interrupt detection enable/disable. Each function of INTIF is set up by the Interrupt Control Register A or B.
It keeps sending the interrupt signal in "High" level to the CPU until the <Detection flag> is cleared in the Interrupt Control Register. If the ISR is exited without clearing the <Detection flag>, the same interrupt will be detected again when normal operation is resumed. Thus, be sure to clear each <Detection flag> in the ISR. At the same time, the corresponding Interrupt Monitor Register is also cleared.

4.6.4. Detection (CPU)

The CPU detects an interrupt request with the highest priority.

4.6.5. CPU Procedure

On detecting an interrupt, the CPU pushes the contents of xPSR, PC, LR, r12, and r3 to r0 to the stack then enter the ISR.

4.6.6. Interrupt Service Routine (ISR) (Clearing an interrupt factor)

An ISR requires specific programming according to the application to be used. This section describes what is recommended at the service routine programming and how the source is cleared.

(1) Process in the Interrupt Service Routine

An ISR normally pushes register contents to the stack and handles an interrupt as required.
The Cortex-M4 processor automatically pushes the contents of xPSR, PC, LR, r12, and r3-r0 to the stack. No extra programming is required for them.
Push the contents of other registers if needed.
Interrupt requests with higher priority and exceptions such as NMI are accepted even when an ISR is being executed. We recommend you to push the contents of general-purpose registers that might be rewritten.

(2) Clearing an Interrupt Source

Some interrupt requests have to be cleared with the Interrupt Control Register.
If an interrupt detection level is set as level-sensitive, an interrupt request continues to exist until it is cleared at its source. Therefore, the interrupt factor must be cleared. If a factor is withdrawn in level detection, the interrupt request signal from INTIF will be withdrawn automatically.
A factor is withdrawn by clearing the <Detection flag> of the Interrupt Control Register of INTIF in the case of edge detection. When effective edge occurs again, it is anew recognized as a factor.

Note: After clearing the interrupt flag of the Interrupt Control Register, please be sure to read the flag which was cleared.

5. Exception/Interrupt-Related Registers

5.1. Register List

Control Registers and their addresses are as follows;

Interrupt Control Registers A

Peripheral function	Function name	Channel/Unit	Base address
Interrupt Control Register A	IA	-	0x4003E000

(1/2)

Register name		Address (+BASE)
Non-maskable Interrupt A Control Register 00	***[IANIC00]***	0x0000
Interrupt A Mode Control Register 00	***[IAIMC00]***	0x0020
Interrupt A Mode Control Register 01	***[IAIMC01]***	0x0021
Interrupt A Mode Control Register 02	***[IAIMC02]***	0x0022
Interrupt A Mode Control Register 03	***[IAIMC03]***	0x0023
Interrupt A Mode Control Register 04	***[IAIMC04]***	0x0024
Interrupt A Mode Control Register 05	***[IAIMC05]***	0x0025
Interrupt A Mode Control Register 06	***[IAIMC06]***	0x0026
Interrupt A Mode Control Register 07	***[IAIMC07]***	0x0027
Interrupt A Mode Control Register 08	***[IAIMC08]***	0x0028
Interrupt A Mode Control Register 09	***[IAIMC09]***	0x0029
Interrupt A Mode Control Register 10	***[IAIMC10]***	0x002A
Interrupt A Mode Control Register 11	***[IAIMC11]***	0x002B
Interrupt A Mode Control Register 12	***[IAIMC12]***	0x002C
Interrupt A Mode Control Register 13	***[IAIMC13]***	0x002D
Interrupt A Mode Control Register 14	***[IAIMC14]***	0x002E
Interrupt A Mode Control Register 15	***[IAIMC15]***	0x002F
Interrupt A Mode Control Register 16	***[IAIMC16]***	0x0030
Interrupt A Mode Control Register 17	***[IAIMC17]***	0x0031
Interrupt A Mode Control Register 18	***[IAIMC18]***	0x0032
Interrupt A Mode Control Register 19	***[IAIMC19]***	0x0033
Interrupt A Mode Control Register 20	***[IAIMC20]***	0x0034
Interrupt A Mode Control Register 21	***[IAIMC21]***	0x0035
Interrupt A Mode Control Register 22	***[IAIMC22]***	0x0036
Interrupt A Mode Control Register 23	***[IAIMC23]***	0x0037
Interrupt A Mode Control Register 24	***[IAIMC24]***	0x0038
Interrupt A Mode Control Register 25	***[IAIMC25]***	0x0039
Interrupt A Mode Control Register 26	***[IAIMC26]***	0x003A
Interrupt A Mode Control Register 27	***[IAIMC27]***	0x003B
Interrupt A Mode Control Register 28	***[IAIMC28]***	0x003C
Interrupt A Mode Control Register 29	***[IAIMC29]***	0x003D
Interrupt A Mode Control Register 30	***[IAIMC30]***	0x003E
Interrupt A Mode Control Register 31	***[IAIMC31]***	0x003F

Note: Byte access is needed for ***[IANIC00]*** and ***[IAIMCxx]*** Registers.

(2/2)

Register name		Address (+BASE)
Interrupt A Mode Control Register 49	***[IAIMC49]***	0x0051
Interrupt A Mode Control Register 50	***[IAIMC50]***	0x0052
Interrupt A Mode Control Register 51	***[IAIMC51]***	0x0053
Interrupt A Mode Control Register 52	***[IAIMC52]***	0x0054
Interrupt A Mode Control Register 53	***[IAIMC53]***	0x0055
Interrupt A Mode Control Register 54	***[IAIMC54]***	0x0056
Interrupt A Mode Control Register 55	***[IAIMC55]***	0x0057
Interrupt A Mode Control Register 56	***[IAIMC56]***	0x0058
Interrupt A Mode Control Register 57	***[IAIMC57]***	0x0059

Note: Byte access is needed for ***[IAIMCxx]*** Registers.

Interrupt Control Registers B

Peripheral function	Function name	Channel/Unit	Base address
Interrupt Control Register B	IB	-	0x40083200

(1/4)

Register name		Address (+BASE)
Non-maskable Interrupt B Control Register 00	***[IBNIC00]***	0x0010
Interrupt B Mode Control Register 000	***[IBIMC000]***	0x0060
Interrupt B Mode Control Register 001	***[IBIMC001]***	0x0061
Interrupt B Mode Control Register 002	***[IBIMC002]***	0x0062
Interrupt B Mode Control Register 003	***[IBIMC003]***	0x0063
Interrupt B Mode Control Register 004	***[IBIMC004]***	0x0064
Interrupt B Mode Control Register 005	***[IBIMC005]***	0x0065
Interrupt B Mode Control Register 006	***[IBIMC006]***	0x0066
Interrupt B Mode Control Register 007	***[IBIMC007]***	0x0067
Interrupt B Mode Control Register 008	***[IBIMC008]***	0x0068
Interrupt B Mode Control Register 009	***[IBIMC009]***	0x0069
Interrupt B Mode Control Register 010	***[IBIMC010]***	0x006A
Interrupt B Mode Control Register 011	***[IBIMC011]***	0x006B
Interrupt B Mode Control Register 012	***[IBIMC012]***	0x006C
Interrupt B Mode Control Register 013	***[IBIMC013]***	0x006D
Interrupt B Mode Control Register 014	***[IBIMC014]***	0x006E
Interrupt B Mode Control Register 015	***[IBIMC015]***	0x006F
Interrupt B Mode Control Register 016	***[IBIMC016]***	0x0070
Interrupt B Mode Control Register 017	***[IBIMC017]***	0x0071
Interrupt B Mode Control Register 018	***[IBIMC018]***	0x0072
Interrupt B Mode Control Register 019	***[IBIMC019]***	0x0073
Interrupt B Mode Control Register 020	***[IBIMC020]***	0x0074
Interrupt B Mode Control Register 021	***[IBIMC021]***	0x0075
Interrupt B Mode Control Register 022	***[IBIMC022]***	0x0076
Interrupt B Mode Control Register 023	***[IBIMC023]***	0x0077
Interrupt B Mode Control Register 024	***[IBIMC024]***	0x0078
Interrupt B Mode Control Register 025	***[IBIMC025]***	0x0079
Interrupt B Mode Control Register 026	***[IBIMC026]***	0x007A
Interrupt B Mode Control Register 027	***[IBIMC027]***	0x007B
Interrupt B Mode Control Register 028	***[IBIMC028]***	0x007C
Interrupt B Mode Control Register 029	***[IBIMC029]***	0x007D
Interrupt B Mode Control Register 030	***[IBIMC030]***	0x007E
Interrupt B Mode Control Register 031	***[IBIMC031]***	0x007F
Interrupt B Mode Control Register 032	***[IBIMC032]***	0x0080
Interrupt B Mode Control Register 033	***[IBIMC033]***	0x0081
Interrupt B Mode Control Register 034	***[IBIMC034]***	0x0082
Interrupt B Mode Control Register 035	***[IBIMC035]***	0x0083
Interrupt B Mode Control Register 036	***[IBIMC036]***	0x0084
Interrupt B Mode Control Register 037	***[IBIMC037]***	0x0085
Interrupt B Mode Control Register 038	***[IBIMC038]***	0x0086
Interrupt B Mode Control Register 039	***[IBIMC039]***	0x0087

Note: Byte access is needed for ***[IBNIC00]*** and ***[IBIMCxxx]*** Registers.

(2/4)

Register name		Address (+BASE)
Interrupt B Mode Control Register 040	***[IBIMC040]***	0x0088
Interrupt B Mode Control Register 041	***[IBIMC041]***	0x0089
Interrupt B Mode Control Register 042	***[IBIMC042]***	0x008A
Interrupt B Mode Control Register 043	***[IBIMC043]***	0x008B
Interrupt B Mode Control Register 044	***[IBIMC044]***	0x008C
Interrupt B Mode Control Register 045	***[IBIMC045]***	0x008D
Interrupt B Mode Control Register 046	***[IBIMC046]***	0x008E
Interrupt B Mode Control Register 047	***[IBIMC047]***	0x008F
Interrupt B Mode Control Register 048	***[IBIMC048]***	0x0090
Interrupt B Mode Control Register 049	***[IBIMC049]***	0x0091
Interrupt B Mode Control Register 050	***[IBIMC050]***	0x0092
Interrupt B Mode Control Register 051	***[IBIMC051]***	0x0093
Interrupt B Mode Control Register 052	***[IBIMC052]***	0x0094
Interrupt B Mode Control Register 053	***[IBIMC053]***	0x0095
Interrupt B Mode Control Register 054	***[IBIMC054]***	0x0096
Interrupt B Mode Control Register 055	***[IBIMC055]***	0x0097
Interrupt B Mode Control Register 056	***[IBIMC056]***	0x0098
Interrupt B Mode Control Register 057	***[IBIMC057]***	0x0099
Interrupt B Mode Control Register 058	***[IBIMC058]***	0x009A
Interrupt B Mode Control Register 059	***[IBIMC059]***	0x009B
Interrupt B Mode Control Register 060	***[IBIMC060]***	0x009C
Interrupt B Mode Control Register 061	***[IBIMC061]***	0x009D
Interrupt B Mode Control Register 062	***[IBIMC062]***	0x009E
Interrupt B Mode Control Register 063	***[IBIMC063]***	0x009F
Interrupt B Mode Control Register 064	***[IBIMC064]***	0x00A0
Interrupt B Mode Control Register 065	***[IBIMC065]***	0x00A1
Interrupt B Mode Control Register 066	***[IBIMC066]***	0x00A2
Interrupt B Mode Control Register 067	***[IBIMC067]***	0x00A3
Interrupt B Mode Control Register 068	***[IBIMC068]***	0x00A4
Interrupt B Mode Control Register 069	***[IBIMC069]***	0x00A5
Interrupt B Mode Control Register 070	***[IBIMC070]***	0x00A6
Interrupt B Mode Control Register 071	***[IBIMC071]***	0x00A7
Interrupt B Mode Control Register 072	***[IBIMC072]***	0x00A8
Interrupt B Mode Control Register 073	***[IBIMC073]***	0x00A9
Interrupt B Mode Control Register 074	***[IBIMC074]***	0x00AA
Interrupt B Mode Control Register 075	***[IBIMC075]***	0x00AB
Interrupt B Mode Control Register 076	***[IBIMC076]***	0x00AC
Interrupt B Mode Control Register 077	***[IBIMC077]***	0x00AD
Interrupt B Mode Control Register 078	***[IBIMC078]***	0x00AE
Interrupt B Mode Control Register 079	***[IBIMC079]***	0x00AF

Note: Byte access is needed for ***[IBIMCxxx]*** Registers.

(3/4)

Register name		Address (+BASE)
Interrupt B Mode Control Register 080	***[IBIMC080]***	0x00B0
Interrupt B Mode Control Register 081	***[IBIMC081]***	0x00B1
Interrupt B Mode Control Register 082	***[IBIMC082]***	0x00B2
Interrupt B Mode Control Register 083	***[IBIMC083]***	0x00B3
Interrupt B Mode Control Register 084	***[IBIMC084]***	0x00B4
Interrupt B Mode Control Register 085	***[IBIMC085]***	0x00B5
Interrupt B Mode Control Register 086	***[IBIMC086]***	0x00B6
Interrupt B Mode Control Register 087	***[IBIMC087]***	0x00B7
Interrupt B Mode Control Register 088	***[IBIMC088]***	0x00B8
Interrupt B Mode Control Register 089	***[IBIMC089]***	0x00B9
Interrupt B Mode Control Register 090	***[IBIMC090]***	0x00BA
Interrupt B Mode Control Register 091	***[IBIMC091]***	0x00BB
Interrupt B Mode Control Register 092	***[IBIMC092]***	0x00BC
Interrupt B Mode Control Register 093	***[IBIMC093]***	0x00BD
Interrupt B Mode Control Register 094	***[IBIMC094]***	0x00BE
Interrupt B Mode Control Register 095	***[IBIMC095]***	0x00BF
Interrupt B Mode Control Register 096	***[IBIMC096]***	0x00C0
Interrupt B Mode Control Register 097	***[IBIMC097]***	0x00C1
Interrupt B Mode Control Register 098	***[IBIMC098]***	0x00C2
Interrupt B Mode Control Register 099	***[IBIMC099]***	0x00C3
Interrupt B Mode Control Register 100	***[IBIMC100]***	0x00C4
Interrupt B Mode Control Register 101	***[IBIMC101]***	0x00C5
Interrupt B Mode Control Register 102	***[IBIMC102]***	0x00C6
Interrupt B Mode Control Register 103	***[IBIMC103]***	0x00C7
Interrupt B Mode Control Register 104	***[IBIMC104]***	0x00C8
Interrupt B Mode Control Register 105	***[IBIMC105]***	0x00C9
Interrupt B Mode Control Register 106	***[IBIMC106]***	0x00CA
Interrupt B Mode Control Register 107	***[IBIMC107]***	0x00CB
Interrupt B Mode Control Register 108	***[IBIMC108]***	0x00CC
Interrupt B Mode Control Register 109	***[IBIMC109]***	0x00CD
Interrupt B Mode Control Register 110	***[IBIMC110]***	0x00CE
Interrupt B Mode Control Register 111	***[IBIMC111]***	0x00CF
Interrupt B Mode Control Register 112	***[IBIMC112]***	0x00D0
Interrupt B Mode Control Register 113	***[IBIMC113]***	0x00D1
Interrupt B Mode Control Register 114	***[IBIMC114]***	0x00D2
Interrupt B Mode Control Register 115	***[IBIMC115]***	0x00D3
Interrupt B Mode Control Register 116	***[IBIMC116]***	0x00D4
Interrupt B Mode Control Register 117	***[IBIMC117]***	0x00D5
Interrupt B Mode Control Register 118	***[IBIMC118]***	0x00D6
Interrupt B Mode Control Register 119	***[IBIMC119]***	0x00D7

Note: Byte access is needed for ***[IBIMCxxx]*** Registers

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Register name		Address (+BASE)
Interrupt B Mode Control Register 120	***[IBIMC120]***	0x00D8
Interrupt B Mode Control Register 121	***[IBIMC121]***	0x00D9
Interrupt B Mode Control Register 122	***[IBIMC122]***	0x00DA
Interrupt B Mode Control Register 123	***[IBIMC123]***	0x00DB
Interrupt B Mode Control Register 124	***[IBIMC124]***	0x00DC
Interrupt B Mode Control Register 125	***[IBIMC125]***	0x00DD
Interrupt B Mode Control Register 126	***[IBIMC126]***	0x00DE
Interrupt B Mode Control Register 127	***[IBIMC127]***	0x00DF
Interrupt B Mode Control Register 128	***[IBIMC128]***	0x00E0
Interrupt B Mode Control Register 129	***[IBIMC129]***	0x00E1
Interrupt B Mode Control Register 130	***[IBIMC130]***	0x00E2
Interrupt B Mode Control Register 131	***[IBIMC131]***	0x00E3
Interrupt B Mode Control Register 132	***[IBIMC132]***	0x00E4
Interrupt B Mode Control Register 133	***[IBIMC133]***	0x00E5
Interrupt B Mode Control Register 134	***[IBIMC134]***	0x00E6
Interrupt B Mode Control Register 135	***[IBIMC135]***	0x00E7
Interrupt B Mode Control Register 136	***[IBIMC136]***	0x00E8
Interrupt B Mode Control Register 137	***[IBIMC137]***	0x00E9
Interrupt B Mode Control Register 138	***[IBIMC138]***	0x00EA
Interrupt B Mode Control Register 139	***[IBIMC139]***	0x00EB
Interrupt B Mode Control Register 140	***[IBIMC140]***	0x00EC
Interrupt B Mode Control Register 141	***[IBIMC141]***	0x00ED
Reserved	**-**	0x00EE to 0x00F0
Interrupt B Mode Control Register 145	***[IBIMC145]***	0x00F1
Interrupt B Mode Control Register 146	***[IBIMC146]***	0x00F2
Interrupt B Mode Control Register 147	***[IBIMC147]***	0x00F3
Interrupt B Mode Control Register 148	***[IBIMC148]***	0x00F4
Interrupt B Mode Control Register 149	***[IBIMC149]***	0x00F5
Interrupt B Mode Control Register 150	***[IBIMC150]***	0x00F6
Interrupt B Mode Control Register 151	***[IBIMC151]***	0x00F7
Interrupt B Mode Control Register 152	***[IBIMC152]***	0x00F8
Interrupt B Mode Control Register 153	***[IBIMC153]***	0x00F9
Interrupt B Mode Control Register 154	***[IBIMC154]***	0x00FA
Interrupt B Mode Control Register 155	***[IBIMC155]***	0x00FB
Interrupt B Mode Control Register 156	***[IBIMC156]***	0x00FC
Interrupt B Mode Control Register 157	***[IBIMC157]***	0x00FD
Interrupt B Mode Control Register 158	***[IBIMC158]***	0x00FE
Interrupt B Mode Control Register 159	***[IBIMC159]***	0x00FF

Note: Byte access is needed for ***[IBIMCxxx]*** Registers

Reset Flag Registers

Peripheral function		Channel/Unit	Base address
Low speed oscillation/power control/reset	RLM	-	0x4003E400

Register name		Address (+BASE)
Reset Flag Register 0	***[RLMRSTFLG0]***	0x0002
Reset Flag Register 1	***[RLMRSTFLG1]***	0x0003

Note: Byte access is needed for Reset Flag Registers

Interrupt Monitor Registers

Peripheral function		Channel/Unit	Base address
Interrupt Monitor	IMN	-	0x40083300

Register name		Address (+BASE)
Non-maskable Interrupt Monitor Flag Register	***[IMNFLGNMI]***	0x0000
Interrupt Monitor Flag Register 1	***[IMNFLG1]***	0x0004
Interrupt Monitor Flag Register 2	***[IMNFLG2]***	0x0008
Interrupt Monitor Flag Register 3	***[IMNFLG3]***	0x000C
Interrupt Monitor Flag Register 4	***[IMNFLG4]***	0x0010
Interrupt Monitor Flag Register 5	***[IMNFLG5]***	0x0014
Interrupt Monitor Flag Register 6	***[IMNFLG6]***	0x0018
Interrupt Monitor Flag Register 7	***[IMNFLG7]***	0x001C

NVIC Registers

Peripheral function	Channel/Unit	Base address
NVIC Register	-	0xE000E000

Register name	Address (+BASE)
SysTick Control and Status Register	0x0010
SysTick Reload Value Register	0x0014
SysTick Current Value Register	0x0018
SysTick Calibration Value Register	0x001C
Interrupt Set-Enable Register 0	0x0100
Interrupt Set-Enable Register 1	0x0104
Interrupt Set-Enable Register 2	0x0108
Interrupt Set-Enable Register 3	0x010C
Interrupt Set-Enable Register 4	0x0110
Interrupt Set-Enable Register 5	0x0114
Interrupt Clear-Enable Register 0	0x0180
Interrupt Clear-Enable Register 1	0x0184
Interrupt Clear-Enable Register 2	0x0188
Interrupt Clear-Enable Register 3	0x018C
Interrupt Clear-Enable Register 4	0x0190
Interrupt Clear-Enable Register 5	0x0194
Interrupt Set-Pending Register 0	0x0200
Interrupt Set-Pending Register 1	0x0204
Interrupt Set-Pending Register 2	0x0208
Interrupt Set-Pending Register 3	0x020C
Interrupt Set-Pending Register 4	0x0210
Interrupt Set-Pending Register 5	0x0214
Interrupt Clear-Pending Register 0	0x0280
Interrupt Clear-Pending Register 1	0x0284
Interrupt Clear-Pending Register 2	0x0288
Interrupt Clear-Pending Register 3	0x028C
Interrupt Clear-Pending Register 4	0x0290
Interrupt Clear-Pending Register 5	0x0294
Interrupt Priority Register	0x0400 to 0x04AC
Vector Table Offset Register	0x0D08
Application Interrupt and Reset Control Register	0x0D0C
System Handler Priority Register	0x0D18, 0x0D1C, 0x0D20
System Handler Control and State Register	0x0D24

5.2. Interrupt Control Registers A

5.2.1. *[IANIC00]* (Non-maskable Interrupt A Control Register 00)

Bit	Bit Symbol	After Reset	Type	Function
7	INTNCLR	0	W	Detection flag clear control 0: - 1: Clear Read as "0".
6	-	0	R	Read as "0".
5	INTNFLG	0	R	Detection flag 0: Not detected 1: Detected
4	-	0	R	Read as "0".
3:1	-	010	R	Read as "010".
0	-	1	R	Read as "0".

5.2.2. *[IAIMC00 to 31,49 to 57]* (Interrupt A Mode Control Register n)

(1) ***[IAIMC00 to 31]*** Registers

Bit	Bit Symbol	After Reset	Type	Function
7	INTNCLR	0	W	Falling edge detection flag clear control 0: - 1: Clear Read as "0".
6	INTPCLR	0	W	Rising edge detection flag clear control 0: - 1: Clear Read as "0".
5	INTNFLG	0	R	Falling edge detection flag 0: Not detected 1: Detected
4	INTPFLG	0	R	Rising edge detection flag 0: Not detected 1: Detected
3:1	INTMODE[2:0]	000	R/W	Interrupt detection level selection 000: Low level 001: High level 010: Falling edge 011: Rising edge 100: Both edge 101: Reserved. 110: Reserved. 111: Reserved.
0	INTEN	0	R/W	Interrupt control 0: Interrupt detection disabled 1: Interrupt detection enabled

(2) ***[IAIMC49]*** Register

Bit	Bit Symbol	After Reset	Type	Function
7	INTNCLR	0	W	Detection flag clear control 0: - 1: Clear Read as "0".
6	-	0	R	Read as "0".
5	INTNFLG	0	R	Detection flag 0: Not detected 1: Detected
4	-	0	R	Read as "0".
3:1	-	010	R	Read as "010".
0	INTEN	0	R/W	Interrupt control 0: Interrupt detection disabled 1: Interrupt detection enabled

(3) ***[IAIMC50 to 57]*** Registers

Bit	Bit Symbol	After Reset	Type	Function
7	-	0	R	Read as "0".
6	INTPCLR	0	W	Detection flag clear control 0: - 1: Clear Read as "0".
5	-	0	R	Read as "0".
4	INTPFLG	0	R	Detection flag 0: Not detected 1: Detected
3:1	-	011	R	Read as "011".
0	INTEN	0	R/W	Interrupt control 0: Interrupt detection disabled 1: Interrupt detection enabled

5.3. Interrupt Control Registers B

5.3.1. *[IBNIC00]* (Non-maskable Interrupt B Control Register 00)

Bit	Bit Symbol	After Reset	Type	Function
7	-	0	R	Read as "0".
6	INTPCLR	0	W	Detection flag clear control 0: - 1: Clear Read as "0".
5	-	0	R	Read as "0".
4	INTPFLG	0	R	Detection flag 0: Not detected 1: Detected
3:1	-	011	R	Read as "011".
0	-	1	R	Read as "1".

5.3.2. *[IBIMC000 to 141, 145 to 159]* (Interrupt B Mode Control Registers n)

Bit	Bit Symbol	After Reset	Type	Function
7	-	0	R	Read as "0".
6	INTPCLR	0	W	Detection flag clear control 0: - 1: Clear Read as "0".
5	-	0	R	Read as "0".
4	INTPFLG	0	R	Detection flag 0: Not detected 1: Detected
3:1	-	011	R	Read as"011".
0	INTEN	0	R/W	Interrupt control 0: Interrupt detection disabled 1: Interrupt detection enabled

5.4. Reset Flag Registers

5.4.1. *[RLMRSTFLG0]* (Reset Flag Register 0)

Bit	Bit Symbol	After Power On Reset	Type	Function
7:6	-	0	R	Read as "0".
5	LVDRSTF	Undefined	R	LVD / PORF reset flag 0: - 1: Reset from LVD/ PORF
			W	LVD / PORF reset flag 0: Clear 1: Don't care
4	STOP2RSTF	Undefined	R	STOP2 reset flag 0: - 1: Reset generated by releasing STOP2 mode
			W	STOP2 reset flag 0: Clear 1: Don't care
3	PINRSTF	Undefined	R	Reset pin flag 0: - 1: Reset from Reset pin
			W	Reset pin flag 0: Clear 1: Don't care
2:1	-	Undefined	R	Read as "Undefined".
			W	Write as "00".
0	PORSTF	1	R	Power On Reset flag 0: - 1: Reset from by Power On Reset
			W	Power On Reset flag 0: Clear 1: Don't care

Note: Reset flags except <PORSTF> become undefined after Power On Reset release. When release of power on reset is detected, please write "0" to all the reset flags for initialization.

5.4.2. *[RLMRSTFLG1]* (Reset Flag Register 1)

Bit	Bit Symbol	After Power On Reset	Type	Function
7:4	-	0	R	Read as "0".
3	OFDRSTF	0	R	OFD reset flag 0: - 1: Reset from OFD
			W	OFD reset flag 0: Clear 1: Don't care
2	WDTRSTF	0	R	SIWDT reset flag 0: - 1: Reset from SIWDT
			W	SIWDT reset flag 0: Clear 1: Don't care
1	LOCKRSTF	0	R	LOCKUP reset flag 0: - 1: Reset from LOCKUP
			W	LOCKUP reset flag 0: Clear 1: Don't care
0	SYSRSTF	0	R	<SYSRESETREQ> reset flag 0: - 1: Reset from <SYSRESETREQ>
			W	<SYSRESETREQ> reset flag 0: Clear 1: Don't care

5.5. Interrupt Monitor Registers

5.5.1. *[IMNFLGNMI]* (Non-maskable Interrupt Monitor Flag Register)

Bit	Bit Symbol	After Reset	Type	Function
31:17	-	0	R	Read as "0".
16	INT016FLG	0	R	INTWDT0 Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
15:1	-	0	R	Read as "0".
0	INT000FLG	0	R	INTLVD Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected

5.5.2. *[IMNFLG1]* (Interrupt Monitor Flag Register 1)

Bit	Bit Symbol	After Reset	Type	Function
31	INT063FLG	0	R	INT15b Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
30	INT062FLG	0	R	INT15a Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
29	INT061FLG	0	R	INT14b Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
28	INT060FLG	0	R	INT14a Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
27	INT059FLG	0	R	INT13b Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
26	INT058FLG	0	R	INT13a Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
25	INT057FLG	0	R	INT12b Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
24	INT056FLG	0	R	INT12a Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
23	INT055FLG	0	R	INT11b Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
22	INT054FLG	0	R	INT11a Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
21	INT053FLG	0	R	INT10b Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
20	INT052FLG	0	R	INT10a Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected

Bit	Bit Symbol	After Reset	Type	Function
19	INT051FLG	0	R	INT09b Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
18	INT050FLG	0	R	INT09a Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
17	INT049FLG	0	R	INT08b Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
16	INT048FLG	0	R	INT08a Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
15	INT047FLG	0	R	INT07bInterrupt detection flag 0: Interrupt not detected 1: Interrupt detected
14	INT046FLG	0	R	INT07a Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
13	INT045FLG	0	R	INT06b Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
12	INT044FLG	0	R	INT06a Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
11	INT043FLG	0	R	INT05b Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
10	INT042FLG	0	R	INT05a Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
9	INT041FLG	0	R	INT04b Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
8	INT040FLG	0	R	INT04a Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
7	INT039FLG	0	R	INT03b Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
6	INT038FLG	0	R	INT03a Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
5	INT037FLG	0	R	INT02b Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
4	INT036FLG	0	R	INT02a Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
3	INT035FLG	0	R	INT01b Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
2	INT034FLG	0	R	INT01a Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
1	INT033FLG	0	R	INT00b Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
0	INT032FLG	0	R	INT00a Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected

5.5.3. *[IMNFLG2]* (Interrupt Monitor Flag Register 2)

Bit	Bit Symbol	After Reset	Type	Function
31:26	-	0	R	Read as "0".
25	INT089FLG	0	R	INTLTTMR0 Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
24	INT088FLG	0	R	INTRMC1 Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
23	INT087FLG	0	R	INTRMC0 Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
22	INT086FLG	0	R	INTISDC Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
21	INT085FLG	0	R	INTISDB Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
20	INT084FLG	0	R	INTISDA Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
19	INT083FLG	0	R	INTCECTX Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
18	INT082FLG	0	R	INTCECRX Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
17	INT081FLG	0	R	INTRTC Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
16:0	-	0	R	Read as "0".

5.5.4. *[IMNFLG3]* (Interrupt Monitor Flag Register 3)

Bit	Bit Symbol	After Reset	Type	Function
31	INT127FLG	0	R	T32A ch3 Timer A capture 0 interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
30	INT126FLG	0	R	T32A ch3 Timer A match, overflow, and underflow interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
29	INT125FLG	0	R	T32A ch2 Timer C pulse count interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
28	INT124FLG	0	R	T32A ch2 Timer C capture 1 interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
27	INT123FLG	0	R	T32A ch2 Timer C capture 0 interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
26	INT122FLG	0	R	T32A ch2 Timer C match, overflow, and underflow interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
25	INT121FLG	0	R	T32A ch2 Timer B capture 1 interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
24	INT120FLG	0	R	T32A ch2 Timer B capture 0 interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
23	INT119FLG	0	R	T32A ch2 Timer B match, overflow, and underflow interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
22	INT118FLG	0	R	T32A ch2 Timer A capture 1 interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
21	INT117FLG	0	R	T32A ch2 Timer A capture 0 interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
20	INT116FLG	0	R	T32A ch2 Timer A match, overflow, and underflow interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
19	INT115FLG	0	R	T32A ch1 Timer C pulse count interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
18	INT114FLG	0	R	T32A ch1 Timer C capture 1 interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
17	INT113FLG	0	R	T32A ch1 Timer C capture 0 interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
16	INT112FLG	0	R	T32A ch1 Timer C match, overflow, and underflow interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
15	INT111FLG	0	R	T32A ch1 Timer B capture 1 interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
14	INT110FLG	0	R	T32A ch1 Timer B capture 0 interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
13	INT109FLG	0	R	T32A ch1 Timer B match, overflow, and underflow interrupt detection flag 0: Interrupt not detected 1: Interrupt detected

Bit	Bit Symbol	After Reset	Type	Function
12	INT108FLG	0	R	T32A ch1 Timer A capture 1 interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
11	INT107FLG	0	R	T32A ch1 Timer A capture 0 interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
10	INT106FLG	0	R	T32A ch1 Timer A match, overflow, and underflow interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
9	INT105FLG	0	R	T32A ch0 Timer C pulse count interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
8	INT104FLG	0	R	T32A ch0 Timer C capture 1 interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
7	INT103FLG	0	R	T32A ch0 Timer C capture 0 interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
6	INT102FLG	0	R	T32A ch0 Timer C match, overflow, and underflow interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
5	INT101FLG	0	R	T32A ch0 Timer B capture 1 interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
4	INT100FLG	0	R	T32A ch0 Timer B capture 0 interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
3	INT099FLG	0	R	T32A ch0 Timer B match, overflow, and underflow interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
2	INT098FLG	0	R	T32A ch0 Timer A capture 1 interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
1	INT097FLG	0	R	T32A ch0 Timer A capture 0 interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
0	INT096FLG	0	R	T32A ch0 Timer A match, overflow, and underflow interrupt detection flag 0: Interrupt not detected 1: Interrupt detected

5.5.5. *[IMNFLG4]* (Interrupt Monitor Flag Register 4)

Bit	Bit Symbol	After Reset	Type	Function
31	INT159FLG	0	R	T32A ch6 Timer B match, overflow, and underflow interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
30	INT158FLG	0	R	T32A ch6 Timer A capture 1 interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
29	INT157FLG	0	R	T32A ch6 Timer A capture 0 interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
28	INT156FLG	0	R	T32A ch6 Timer A match, overflow, and underflow interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
27	INT155FLG	0	R	T32A ch5 Timer C pulse count interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
26	INT154FLG	0	R	T32A ch5 Timer C capture 1 interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
25	INT153FLG	0	R	T32A ch5 Timer C capture 0 interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
24	INT152FLG	0	R	T32A ch5 Timer C match, overflow, and underflow interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
23	INT151FLG	0	R	T32A ch5 Timer B capture 1 interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
22	INT150FLG	0	R	T32A ch5 Timer B capture 0 interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
21	INT149FLG	0	R	T32A ch5 Timer B match, overflow, and underflow interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
20	INT148FLG	0	R	T32A ch5 Timer A capture 1 interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
19	INT147FLG	0	R	T32A ch5 Timer A capture 0 interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
18	INT146FLG	0	R	T32A ch5 Timer A match, overflow, and underflow interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
17	INT145FLG	0	R	T32A ch4 Timer C pulse count interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
16	INT144FLG	0	R	T32A ch4 Timer C capture 1 interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
15	INT143FLG	0	R	T32A ch4 Timer C capture 0 interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
14	INT142FLG	0	R	T32A ch4 Timer C match, overflow, and underflow interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
13	INT141FLG	0	R	T32A ch4 Timer B capture 1 interrupt detection flag 0: Interrupt not detected 1: Interrupt detected

Bit	Bit Symbol	After Reset	Type	Function
12	INT140FLG	0	R	T32A ch4 Timer B capture 0 interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
11	INT139FLG	0	R	T32A ch4 Timer B match, overflow, and underflow interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
10	INT138FLG	0	R	T32A ch4 Timer A capture 1 interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
9	INT137FLG	0	R	T32A ch4 Timer A capture 0 interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
8	INT136FLG	0	R	T32A ch4 Timer A match, overflow, and underflow interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
7	INT135FLG	0	R	T32A ch3 Timer C pulse count interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
6	INT134FLG	0	R	T32A ch3 Timer C capture 1 interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
5	INT133FLG	0	R	T32A ch3 Timer C capture 0 interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
4	INT132FLG	0	R	T32A ch3 Timer C match, overflow, and underflow interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
3	INT131FLG	0	R	T32A ch3 Timer B capture 1 interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
2	INT130FLG	0	R	T32A ch3 Timer B capture 0 interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
1	INT129FLG	0	R	T32A ch3 Timer B match, overflow, and underflow interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
0	INT128FLG	0	R	T32A ch3 Timer A capture 1 interrupt detection flag 0: Interrupt not detected 1: Interrupt detected

5.5.6. *[IMNFLG5]* (Interrupt Monitor Flag Register 5)

Bit	Bit Symbol	After Reset	Type	Function
31	INT191FLG	0	R	T32A ch9 Timer B capture 1 interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
30	INT190FLG	0	R	T32A ch9 Timer B capture 0 interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
29	INT189FLG	0	R	T32A ch9 Timer B match, overflow, and underflow interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
28	INT188FLG	0	R	T32A ch9 Timer A capture 1 interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
27	INT187FLG	0	R	T32A ch9 Timer A capture 0 interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
26	INT186FLG	0	R	T32A ch9 Timer A match, overflow, and underflow interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
25	INT185FLG	0	R	T32A ch8 Timer C pulse count interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
24	INT184FLG	0	R	T32A ch8 Timer C capture 1 interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
23	INT183FLG	0	R	T32A ch8 Timer C capture 0 interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
22	INT182FLG	0	R	T32A ch8 Timer C match, overflow, and underflow interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
21	INT181FLG	0	R	T32A ch8 Timer B capture 1 interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
20	INT180FLG	0	R	T32A ch8 Timer B capture 0 interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
19	INT179FLG	0	R	T32A ch8 Timer B match, overflow, and underflow interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
18	INT178FLG	0	R	T32A ch8 Timer A capture 1 interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
17	INT177FLG	0	R	T32A ch8 Timer A capture 0 interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
16	INT176FLG	0	R	T32A ch8 Timer A match, overflow, and underflow interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
15	INT175FLG	0	R	T32A ch7 Timer C pulse count interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
14	INT174FLG	0	R	T32A ch7 Timer C capture 1 interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
13	INT173FLG	0	R	T32A ch7 Timer C capture 0 interrupt detection flag 0: Interrupt not detected 1: Interrupt detected

Bit	Bit Symbol	After Reset	Type	Function
12	INT172FLG	0	R	T32A ch7 Timer C match, overflow, and underflow interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
11	INT171FLG	0	R	T32A ch7 Timer B capture 1 interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
10	INT170FLG	0	R	T32A ch7 Timer B capture 0 interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
9	INT169FLG	0	R	T32A ch7 Timer B match, overflow, and underflow interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
8	INT168FLG	0	R	T32A ch7 Timer A capture 1 interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
7	INT167FLG	0	R	T32A ch7 Timer A capture 0 interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
6	INT166FLG	0	R	T32A ch7 Timer A match, overflow, and underflow interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
5	INT165FLG	0	R	T32A ch6 Timer C pulse count interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
4	INT164FLG	0	R	T32A ch6 Timer C capture 1 interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
3	INT163FLG	0	R	T32A ch6 Timer C capture 0 interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
2	INT162FLG	0	R	T32A ch6 Timer C match, overflow, and underflow interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
1	INT161FLG	0	R	T32A ch6 Timer B capture 1 interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
0	INT160FLG	0	R	T32A ch6 Timer B capture 0 interrupt detection flag 0: Interrupt not detected 1: Interrupt detected

5.5.7. *[IMNFLG6]* (Interrupt Monitor Flag Register 6)

Bit	Bit Symbol	After Reset	Type	Function
31	INT223FLG	0	R	T32A ch12 Timer C capture 0 interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
30	INT222FLG	0	R	T32A ch12 Timer C match, overflow, and underflow interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
29	INT221FLG	0	R	T32A ch12 Timer B capture 1 interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
28	INT220FLG	0	R	T32A ch12 Timer B capture 0 interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
27	INT219FLG	0	R	T32A ch12 Timer B match, overflow, and underflow interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
26	INT218FLG	0	R	T32A ch12 Timer A capture 1 interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
25	INT217FLG	0	R	T32A ch12 Timer A capture 0 interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
24	INT216FLG	0	R	T32A ch12 Timer A match, overflow, and underflow interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
23	INT215FLG	0	R	T32A ch11 Timer C pulse count interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
22	INT214FLG	0	R	T32A ch11 Timer C capture 1 interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
21	INT213FLG	0	R	T32A ch11 Timer C capture 0 interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
20	INT212FLG	0	R	T32A ch11 Timer C match, overflow, and underflow interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
19	INT211FLG	0	R	T32A ch11 Timer B capture 1 interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
18	INT210FLG	0	R	T32A ch11 Timer B capture 0 interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
17	INT209FLG	0	R	T32A ch11 Timer B match, overflow, and underflow interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
16	INT208FLG	0	R	T32A ch11 Timer A capture 1 interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
15	INT207FLG	0	R	T32A ch11 Timer A capture 0 interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
14	INT206FLG	0	R	T32A ch11 Timer A match, overflow, and underflow interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
13	INT205FLG	0	R	T32A ch10 Timer C pulse count interrupt detection flag 0: Interrupt not detected 1: Interrupt detected

Bit	Bit Symbol	After Reset	Type	Function
12	INT204FLG	0	R	T32A ch10 Timer C capture 1 interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
11	INT203FLG	0	R	T32A ch10 Timer C capture 0 interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
10	INT202FLG	0	R	T32A ch10 Timer C match, overflow, and underflow interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
9	INT201FLG	0	R	T32A ch10 Timer B capture 1 interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
8	INT200FLG	0	R	T32A ch10 Timer B capture 0 interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
7	INT199FLG	0	R	T32A ch10 Timer B match, overflow, and underflow interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
6	INT198FLG	0	R	T32A ch10 Timer A capture 1 interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
5	INT197FLG	0	R	T32A ch10 Timer A capture 0 interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
4	INT196FLG	0	R	T32A ch10 Timer A match, overflow, and underflow interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
3	INT195FLG	0	R	T32A ch9 Timer C pulse count interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
2	INT194FLG	0	R	T32A ch9 Timer C capture 1 interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
1	INT193FLG	0	R	T32A ch9 Timer C capture 0 interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
0	INT192FLG	0	R	T32A ch9 Timer C match, overflow, and underflow interrupt detection flag 0: Interrupt not detected 1: Interrupt detected

5.5.8. *[IMNFLG7]* (Interrupt Monitor Flag Register 7)

Bit	Bit Symbol	After Reset	Type	Function
31	INT255FLG	0	R	T32A ch15 Timer C capture 1 detection flag 0: Interrupt not detected 1: Interrupt detected
30	INT254FLG	0	R	T32A ch15 Timer C capture 0 detection flag 0: Interrupt not detected 1: Interrupt detected
29	INT253FLG	0	R	T32A ch15 Timer C match, overflow, and underflow detection flag 0: Interrupt not detected 1: Interrupt detected
28	INT252FLG	0	R	T32A ch15 Timer B capture 1 detection flag 0: Interrupt not detected 1: Interrupt detected
27	INT251FLG	0	R	T32A ch15 Timer B capture 0 detection flag 0: Interrupt not detected 1: Interrupt detected
26	INT250FLG	0	R	T32A ch15 Timer B match, overflow, and underflow detection flag 0: Interrupt not detected 1: Interrupt detected
25	INT249FLG	0	R	T32A ch15 Timer A capture 1 detection flag 0: Interrupt not detected 1: Interrupt detected
24	INT248FLG	0	R	T32A ch15 Timer A capture 0 detection flag 0: Interrupt not detected 1: Interrupt detected
23	INT247FLG	0	R	T32A ch15 Timer A match, overflow, and underflow detection flag 0: Interrupt not detected 1: Interrupt detected
22	INT246FLG	0	R	T32A ch14 Timer B capture 1 detection flag 0: Interrupt not detected 1: Interrupt detected
21	INT245FLG	0	R	T32A ch14 Timer B capture 0 detection flag 0: Interrupt not detected 1: Interrupt detected
20	INT244FLG	0	R	T32A ch14 Timer B match, overflow, and underflow detection flag 0: Interrupt not detected 1: Interrupt detected
19	INT243FLG	0	R	T32A ch14 Timer A capture 1 detection flag 0: Interrupt not detected 1: Interrupt detected
18	INT242FLG	0	R	T32A ch14 Timer A capture 0 detection flag 0: Interrupt not detected 1: Interrupt detected
17	INT241FLG	0	R	T32A ch14 Timer A match, overflow, and underflow detection flag 0: Interrupt not detected 1: Interrupt detected
16	-	0	R	Read as "0".
15	-	0	R	Read as "0".
14	-	0	R	Read as "0".
13	INT237FLG	0	R	MDMAC unit A descriptor error interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
12	INT236FLG	0	R	MDMAC unit A bus error interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
11	INT235FLG	0	R	T32A ch13 Timer C pulse count interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
10	INT234FLG	0	R	T32A ch13 Timer C capture 1 interrupt detection flag 0: Interrupt not detected 1: Interrupt detected

Bit	Bit Symbol	After Reset	Type	Function
9	INT233FLG	0	R	T32A ch13 Timer C capture 0 interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
8	INT232FLG	0	R	T32A ch13 Timer C match, overflow, and underflow interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
7	INT231FLG	0	R	T32A ch13 Timer B capture 1 interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
6	INT230FLG	0	R	T32A ch13 Timer B capture 0 interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
5	INT229FLG	0	R	T32A ch13 Timer B match, overflow, and underflow interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
4	INT228FLG	0	R	T32A ch13 Timer A capture 1 interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
3	INT227FLG	0	R	T32A ch13 Timer A capture 0 interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
2	INT226FLG	0	R	T32A ch13 Timer A match, overflow, and underflow interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
1	INT225FLG	0	R	T32A ch12 Timer C pulse count interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
0	INT224FLG	0	R	T32A ch12 Timer C capture 1 interrupt detection flag 0: Interrupt not detected 1: Interrupt detected

5.6. NVIC Registers

5.6.1. SysTick Control and Status Register

Bit	Bit Symbol	After Reset	Type	Function
31:17	-	0	R	Read as "0".
16	COUNTFLAG	0	R/W	0: Timer not counted to 0 1: Timer counted to 0 Returns "1" if timer counted to "0" since last time this was read. Clears on read of any part of the SysTick Control and Status Register.
15:3	-	0	R	Read as "0".
2	CLKSOURCE	0	R/W	0: External reference clock (fosc/64) 1: CPU clock(fsys)
1	TICKINT	0	R/W	0: Do not pend SysTick. 1: Pend SysTick.
0	ENABLE	0	R/W	0: Disable 1: Enable If "1" is set, it re-loads with the value of the Reload Value Register and starts operation.

5.6.2. SysTick Reload Value Register

Bit	Bit Symbol	After Reset	Type	Function
31:24	-	0	R	Read as "0".
23:0	RELOAD[23:0]	Undefined	R/W	Reload value Set the value to load into the SysTick Current Value Register when the timer reaches "0".

5.6.3. SysTick Current Value Register

Bit	Bit Symbol	After Reset	Type	Function
31:24	-	0	R	Read as "0".
23:0	CURRENT[23:0]	Undefined	R	Current SysTick timer value
			W	Clear Writing to this register with any value clears it to 0. Clearing this register also clears the <COUNTFLAG> bit of the SysTick Control and Status Register.

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5.6.4. SysTick Calibration Value Register

Bit	Bit Symbol	After Reset	Type	Function
31	NOREF	0	R	0: Reference clock provided. 1: No reference clock
30	SKEW	1	R	0: Calibration value is 10 ms. 1: Calibration value is not 10 ms.
29:24	-	0	R	Read as "0".
23:0	TENMS	0x000000	R	Calibration value (Note)

Note: This product does not prepare the calibration value.

5.6.5. Interrupt Control Registers

Following four registers will be used to control each interrupt factor; Interrupt Set-Enable Register, Interrupt Clear-Enable Register, Interrupt Set-Pending Register, and Interrupt Clear-Pending Register.
Each bit corresponds to specified interruption.

5.6.5.1. Interrupt Set-Enable Register

Each bit corresponds to the specified number of interrupts. It can enable interrupts and check if interrupts are enabled.
Writing "1" to a bit in this register enables the corresponding interrupt.
Writing "0" has no effect.
Reading the bits can see the enable/disable condition of the corresponding interrupts. Writing "1" to a corresponding bit in the Interrupt Clear-Enable Register clears the bit in this register.

(a) Interrupt Set-Enable Register 0

Bit	Bit Symbol	After Reset	Type	Function
31	SETENA (Interrupt31)	0	R/W	[Write] 1: Enable interrupt [Read] 0: Interrupt is disabled 1: Interrupt is enabled
30	SETENA (Interrupt30)	0		
29	SETENA (Interrupt29)	0		
28	SETENA (Interrupt28)	0		
27	SETENA (Interrupt27)	0		
26	SETENA (Interrupt26)	0		
25	SETENA (Interrupt25)	0		
24	SETENA (Interrupt24)	0		
23	SETENA (Interrupt23)	0		
22	SETENA (Interrupt22)	0		
21	SETENA (Interrupt21)	0		
20	SETENA (Interrupt20)	0		
19	SETENA (Interrupt19)	0		
18	SETENA (Interrupt18)	0		
17	SETENA (Interrupt17)	0		
16	SETENA (Interrupt16)	0		
15	SETENA (Interrupt15)	0		
14	SETENA (Interrupt14)	0		
13	SETENA (Interrupt13)	0		
12	SETENA (Interrupt12)	0		
11	SETENA (Interrupt11)	0		
10	SETENA (Interrupt10)	0		
9	SETENA (Interrupt9)	0		
8	SETENA (Interrupt8)	0		
7	SETENA (Interrupt7)	0		
6	SETENA (Interrupt6)	0		
5	SETENA (Interrupt5)	0		
4	SETENA (Interrupt4)	0		
3	SETENA (Interrupt3)	0		
2	SETENA (Interrupt2)	0		
1	SETENA (Interrupt1)	0		
0	SETENA (Interrupt0)	0		

(b) Interrupt Set-Enable Register 1

Bit	Bit Symbol	After Reset	Type	Function
31	SETENA (Interrupt63)	0	R/W	[Write] 1: Enable interrupt [Read] 0: Interrupt is disabled 1: Interrupt is enabled
30	SETENA (Interrupt62)	0		
29	SETENA (Interrupt61)	0		
28	SETENA (Interrupt60)	0		
27	SETENA (Interrupt59)	0		
26	SETENA (Interrupt58)	0		
25	SETENA (Interrupt57)	0		
24	SETENA (Interrupt56)	0		
23	SETENA (Interrupt55)	0		
22	SETENA (Interrupt54)	0		
21	SETENA (Interrupt53)	0		
20	SETENA (Interrupt52)	0		
19	SETENA (Interrupt51)	0		
18	SETENA (Interrupt50)	0		
17	SETENA (Interrupt49)	0		
16	SETENA (Interrupt48)	0		
15	SETENA (Interrupt47)	0		
14	SETENA (Interrupt46)	0		
13	SETENA (Interrupt45)	0		
12	SETENA (Interrupt44)	0		
11	SETENA (Interrupt43)	0		
10	SETENA (Interrupt42)	0		
9	SETENA (Interrupt41)	0		
8	SETENA (Interrupt40)	0		
7	SETENA (Interrupt39)	0		
6	SETENA (Interrupt38)	0		
5	SETENA (Interrupt37)	0		
4	SETENA (Interrupt36)	0		
3	SETENA (Interrupt35)	0		
2	SETENA (Interrupt34)	0		
1	SETENA (Interrupt33)	0		
0	SETENA (Interrupt32)	0		

(c) Interrupt Set-Enable Register 2

Bit	Bit Symbol	After Reset	Type	Function
31	SETENA (Interrupt95)	0	R/W	[Write] 1: Enable interrupt [Read] 0: Interrupt is disabled 1: Interrupt is enabled
30	SETENA (Interrupt94)	0		
29	SETENA (Interrupt93)	0		
28	SETENA (Interrupt92)	0		
27	SETENA (Interrupt91)	0		
26	SETENA (Interrupt90)	0		
25	SETENA (Interrupt89)	0		
24	SETENA (Interrupt88)	0		
23	SETENA (Interrupt87)	0		
22	SETENA (Interrupt86)	0		
21	SETENA (Interrupt85)	0		
20	SETENA (Interrupt84)	0		
19	SETENA (Interrupt83)	0		
18	SETENA (Interrupt82)	0		
17	SETENA (Interrupt81)	0		
16	SETENA (Interrupt80)	0		
15	SETENA (Interrupt79)	0		
14	SETENA (Interrupt78)	0		
13	SETENA (Interrupt77)	0		
12	SETENA (Interrupt76)	0		
11	SETENA (Interrupt75)	0		
10	SETENA (Interrupt74)	0		
9	SETENA (Interrupt73)	0		
8	SETENA (Interrupt72)	0		
7	SETENA (Interrupt71)	0		
6	SETENA (Interrupt70)	0		
5	SETENA (Interrupt69)	0		
4	SETENA (Interrupt68)	0		
3	SETENA (Interrupt67)	0		
2	SETENA (Interrupt66)	0		
1	SETENA (Interrupt65)	0		
0	SETENA (Interrupt64)	0		

(d) Interrupt Set-Enable Register 3

Bit	Bit Symbol	After Reset	Type	Function
31	SETENA (Interrupt127)	0	R/W	[Write] 1: Enable interrupt [Read] 0: Interrupt is disabled 1: Interrupt is enabled
30	SETENA (Interrupt126)	0		
29	SETENA (Interrupt125)	0		
28	SETENA (Interrupt124)	0		
27	SETENA (Interrupt123)	0		
26	SETENA (Interrupt122)	0		
25	SETENA (Interrupt121)	0		
24	SETENA (Interrupt120)	0		
23	SETENA (Interrupt119)	0		
22	SETENA (Interrupt118)	0		
21	SETENA (Interrupt117)	0		
20	SETENA (Interrupt116)	0		
19	SETENA (Interrupt115)	0		
18	SETENA (Interrupt114)	0		
17	SETENA (Interrupt113)	0		
16	SETENA (Interrupt112)	0		
15	SETENA (Interrupt111)	0		
14	SETENA (Interrupt110)	0		
13	SETENA (Interrupt109)	0		
12	SETENA (Interrupt108)	0		
11	SETENA (Interrupt107)	0		
10	SETENA (Interrupt106)	0		
9	SETENA (Interrupt105)	0		
8	SETENA (Interrupt104)	0		
7	SETENA (Interrupt103)	0		
6	SETENA (Interrupt102)	0		
5	SETENA (Interrupt101)	0		
4	SETENA (Interrupt100)	0		
3	SETENA (Interrupt99)	0		
2	SETENA (Interrupt98)	0		
1	SETENA (Interrupt97)	0		
0	SETENA (Interrupt96)	0		

(e) Interrupt Set-Enable Register 4

Bit	Bit Symbol	After Reset	Type	Function
31	-	0	R/W	Write as "0".
30	-	0	R/W	Write as "0".
29	-	0	R/W	Write as "0".
28	-	0	R/W	Write as "0".
27	SETENA (Interrupt155)	0	R/W	[Write] 1: Enable interrupt [Read] 0: Interrupt is disabled 1: Interrupt is enabled
26	SETENA (Interrupt154)	0		
25	SETENA (Interrupt153)	0		
24	SETENA (Interrupt152)	0		
23	SETENA (Interrupt151)	0		
22	SETENA (Interrupt150)	0		
21	SETENA (Interrupt149)	0		
20	SETENA (Interrupt148)	0		
19	SETENA (Interrupt147)	0		
18	SETENA (Interrupt146)	0		
17	SETENA (Interrupt145)	0		
16	SETENA (Interrupt144)	0		
15	SETENA (Interrupt143)	0		
14	SETENA (Interrupt142)	0		
13	SETENA (Interrupt141)	0		
12	SETENA (Interrupt140)	0		
11	SETENA (Interrupt139)	0		
10	-	0	R/W	Write as "0".
9	-	0	R/W	Write as "0".
8	SETENA (Interrupt136)	0	R/W	[Write] 1: Enable interrupt [Read] 0: Interrupt is disabled 1: Interrupt is enabled
7	SETENA (Interrupt135)	0		
6	SETENA (Interrupt134)	0		
5	SETENA (Interrupt133)	0		
4	SETENA (Interrupt132)	0		
3	SETENA (Interrupt131)	0		
2	SETENA (Interrupt130)	0		
1	SETENA (Interrupt129)	0		
0	SETENA (Interrupt128)	0		

(f) Interrupt Set-Enable Register 5

Bit	Bit Symbol	After Reset	Type	Function
31:15	-	0	R	Read as "0".
14	SETENA (Interrupt174)	0	R/W	[Write] 1: Enable interrupt [Read] 0: Interrupt is disabled 1: Interrupt is enabled
13	SETENA (Interrupt173)	0		
12	SETENA (Interrupt172)	0		
11	SETENA (Interrupt171)	0		
10	SETENA (Interrupt170)	0		
9	SETENA (Interrupt169)	0		
8	SETENA (Interrupt168)	0		
7	-	0	R/W	Write as "0".
6	-	0	R/W	Write as "0".
5	-	0	R/W	Write as "0".
4	-	0	R/W	Write as "0".
3	-	0	R/W	Write as "0".
2	-	0	R/W	Write as "0".
1	-	0	R/W	Write as "0".
0	-	0	R/W	Write as "0".

5.6.5.2. Interrupt Clear-Enable Register

Each bit corresponds to the specified number of interrupts. It can disable interrupts and check if interrupts are disabled.
Writing "1" to a bit in this register disables the corresponding interrupt.
Writing "0" has no effect.
Reading the bits can see the enable/disable condition of the corresponding interrupts.

(a) Interrupt Clear-Enable Register 0

Bit	Bit Symbol	After Reset	Type	Function
31	CLRENA (Interrupt31)	0	R/W	[Write] 1: Disable Interrupt [Read] 0: Interrupt is disabled 1: Interrupt is enabled
30	CLRENA (Interrupt30)	0		
29	CLRENA (Interrupt29)	0		
28	CLRENA (Interrupt28)	0		
27	CLRENA (Interrupt27)	0		
26	CLRENA (Interrupt26)	0		
25	CLRENA (Interrupt25)	0		
24	CLRENA (Interrupt24)	0		
23	CLRENA (Interrupt23)	0		
22	CLRENA (Interrupt22)	0		
21	CLRENA (Interrupt21)	0		
20	CLRENA (Interrupt20)	0		
19	CLRENA (Interrupt19)	0		
18	CLRENA (Interrupt18)	0		
17	CLRENA (Interrupt17)	0		
16	CLRENA (Interrupt16)	0		
15	CLRENA (Interrupt15)	0		
14	CLRENA (Interrupt14)	0		
13	CLRENA (Interrupt13)	0		
12	CLRENA (Interrupt12)	0		
11	CLRENA (Interrupt11)	0		
10	CLRENA (Interrupt10)	0		
9	CLRENA (Interrupt9)	0		
8	CLRENA (Interrupt8)	0		
7	CLRENA (Interrupt7)	0		
6	CLRENA (Interrupt6)	0		
5	CLRENA (Interrupt5)	0		
4	CLRENA (Interrupt4)	0		
3	CLRENA (Interrupt3)	0		
2	CLRENA (Interrupt2)	0		
1	CLRENA (Interrupt1)	0		
0	CLRENA (Interrupt0)	0		

(b) Interrupt Clear-Enable Register 1

Bit	Bit Symbol	After Reset	Type	Function
31	CLRENA (Interrupt63)	0	R/W	[Write] 1: Disable Interrupt [Read] 0: Interrupt is disabled 1: Interrupt is enabled
30	CLRENA (Interrupt62)	0		
29	CLRENA (Interrupt61)	0		
28	CLRENA (Interrupt60)	0		
27	CLRENA (Interrupt59)	0		
26	CLRENA (Interrupt58)	0		
25	CLRENA (Interrupt57)	0		
24	CLRENA (Interrupt56)	0		
23	CLRENA (Interrupt55)	0		
22	CLRENA (Interrupt54)	0		
21	CLRENA (Interrupt53)	0		
20	CLRENA (Interrupt52)	0		
19	CLRENA (Interrupt51)	0		
18	CLRENA (Interrupt50)	0		
17	CLRENA (Interrupt49)	0		
16	CLRENA (Interrupt48)	0		
15	CLRENA (Interrupt47)	0		
14	CLRENA (Interrupt46)	0		
13	CLRENA (Interrupt45)	0		
12	CLRENA (Interrupt44)	0		
11	CLRENA (Interrupt43)	0		
10	CLRENA (Interrupt42)	0		
9	CLRENA (Interrupt41)	0		
8	CLRENA (Interrupt40)	0		
7	CLRENA (Interrupt39)	0		
6	CLRENA (Interrupt38)	0		
5	CLRENA (Interrupt37)	0		
4	CLRENA (Interrupt36)	0		
3	CLRENA (Interrupt35)	0		
2	CLRENA (Interrupt34)	0		
1	CLRENA (Interrupt33)	0		
0	CLRENA (Interrupt32)	0		

(c) Interrupt Clear-Enable Register 2

Bit	Bit Symbol	After Reset	Type	Function
31	CLRENA (Interrupt95)	0	R/W	[Write] 1: Disable Interrupt [Read] 0: Interrupt is disabled 1: Interrupt is enabled
30	CLRENA (Interrupt94)	0		
29	CLRENA (Interrupt93)	0		
28	CLRENA (Interrupt92)	0		
27	CLRENA (Interrupt91)	0		
26	CLRENA (Interrupt90)	0		
25	CLRENA (Interrupt89)	0		
24	CLRENA (Interrupt88)	0		
23	CLRENA (Interrupt87)	0		
22	CLRENA (Interrupt86)	0		
21	CLRENA (Interrupt85)	0		
20	CLRENA (Interrupt84)	0		
19	CLRENA (Interrupt83)	0		
18	CLRENA (Interrupt82)	0		
17	CLRENA (Interrupt81)	0		
16	CLRENA (Interrupt80)	0		
15	CLRENA (Interrupt79)	0		
14	CLRENA (Interrupt78)	0		
13	CLRENA (Interrupt77)	0		
12	CLRENA (Interrupt76)	0		
11	CLRENA (Interrupt75)	0		
10	CLRENA (Interrupt74)	0		
9	CLRENA (Interrupt73)	0		
8	CLRENA (Interrupt72)	0		
7	CLRENA (Interrupt71)	0		
6	CLRENA (Interrupt70)	0		
5	CLRENA (Interrupt69)	0		
4	CLRENA (Interrupt68)	0		
3	CLRENA (Interrupt67)	0		
2	CLRENA (Interrupt66)	0		
1	CLRENA (Interrupt65)	0		
0	CLRENA (Interrupt64)	0		

(d) Interrupt Clear-Enable Register 3

Bit	Bit Symbol	After Reset	Type	Function
31	CLRENA (Interrupt127)	0	R/W	[Write] 1: Disable Interrupt. [Read] 0: Interrupt is disabled 1: Interrupt is enabled
30	CLRENA (Interrupt126)	0		
29	CLRENA (Interrupt125)	0		
28	CLRENA (Interrupt124)	0		
27	CLRENA (Interrupt123)	0		
26	CLRENA (Interrupt122)	0		
25	CLRENA (Interrupt121)	0		
24	CLRENA (Interrupt120)	0		
23	CLRENA (Interrupt119)	0		
22	CLRENA (Interrupt118)	0		
21	CLRENA (Interrupt117)	0		
20	CLRENA (Interrupt116)	0		
19	CLRENA (Interrupt115)	0		
18	CLRENA (Interrupt114)	0		
17	CLRENA (Interrupt113)	0		
16	CLRENA (Interrupt112)	0		
15	CLRENA (Interrupt111)	0		
14	CLRENA (Interrupt110)	0		
13	CLRENA (Interrupt109)	0		
12	CLRENA (Interrupt108)	0		
11	CLRENA (Interrupt107)	0		
10	CLRENA (Interrupt106)	0		
9	CLRENA (Interrupt105)	0		
8	CLRENA (Interrupt104)	0		
7	CLRENA (Interrupt103)	0		
6	CLRENA (Interrupt102)	0		
5	CLRENA (Interrupt101)	0		
4	CLRENA (Interrupt100)	0		
3	CLRENA (Interrupt99)	0		
2	CLRENA (Interrupt98)	0		
1	CLRENA (Interrupt97)	0		
0	CLRENA (Interrupt96)	0		

(e) Interrupt Clear-Enable Register 4

Bit	Bit Symbol	After Reset	Type	Function
31	-	0	R/W	Write as "1".
30	-	0	R/W	Write as "1".
29	-	0	R/W	Write as "1".
28	-	0	R/W	Write as "1".
27	CLRENA (Interrupt155)	0	R/W	[Write] 1: Disable Interrupt. [Read] 0: Interrupt is disabled 1: Interrupt is enabled
26	CLRENA (Interrupt154)	0		
25	CLRENA (Interrupt153)	0		
24	CLRENA (Interrupt152)	0		
23	CLRENA (Interrupt151)	0		
22	CLRENA (Interrupt150)	0		
21	CLRENA (Interrupt149)	0		
20	CLRENA (Interrupt148)	0		
19	CLRENA (Interrupt147)	0		
18	CLRENA (Interrupt146)	0		
17	CLRENA (Interrupt145)	0		
16	CLRENA (Interrupt144)	0		
15	CLRENA (Interrupt143)	0		
14	CLRENA (Interrupt142)	0		
13	CLRENA (Interrupt141)	0		
12	CLRENA (Interrupt140)	0		
11	CLRENA (Interrupt139)	0		
10	-	0	R/W	Write as "1".
9	-	0	R/W	Write as "1".
8	CLRENA (Interrupt136)	0	R/W	[Write] 1: Disable Interrupt. [Read] 0: Interrupt is disabled 1: Interrupt is enabled
7	CLRENA (Interrupt135)	0		
6	CLRENA (Interrupt134)	0		
5	CLRENA (Interrupt133)	0		
4	CLRENA (Interrupt132)	0		
3	CLRENA (Interrupt131)	0		
2	CLRENA (Interrupt130)	0		
1	CLRENA (Interrupt129)	0		
0	CLRENA (Interrupt128)	0		

(f) Interrupt Clear-Enable Register 5

Bit	Bit Symbol	After Reset	Type	Function
31:15	-	0	R	Read as "0".
14	CLRENA (Interrupt174)	0	R/W	[Write] 1: Disable Interrupt. [Read] 0: Interrupt is disabled 1: Interrupt is enabled
13	CLRENA (Interrupt173)	0		
12	CLRENA (Interrupt172)	0		
11	CLRENA (Interrupt171)	0		
10	CLRENA (Interrupt170)	0		
9	CLRENA (Interrupt169)	0		
8	CLRENA (Interrupt168)	0		
7	-	0	R/W	Write as "1".
6	-	0	R/W	Write as "1".
5	-	0	R/W	Write as "1".
4	-	0	R/W	Write as "1".
3	-	0	R/W	Write as "1".
2	-	0	R/W	Write as "1".
1	-	0	R/W	Write as "1".
0	-	0	R/W	Write as "1".

5.6.5.3. Interrupt Set-Pending Register

Each bit corresponds to the specified number of interrupts. It can force interrupts into the pending state and determines which interrupts are currently pending.
Writing "1" to a bit in this register pends the corresponding interrupt. However, writing "1" has no effect on an interrupt that is already pending or is disabled.
Writing "0" has no effect.
Reading the bit returns the current state of the corresponding interrupts.
Writing "1" to a corresponding bit in the Interrupt Clear-Pending Register clears the bit in this register.

(a) Interrupt Set-Pending Register 0

Bit	Bit Symbol	After Reset	Type	Function
31	SETPEND (Interrupt31)	Undefined	R/W	[Write] 1: Pend interrupt [Read] 0: Not pending 1: Pending
30	SETPEND (Interrupt30)	Undefined		
29	SETPEND (Interrupt29)	Undefined		
28	SETPEND (Interrupt28)	Undefined		
27	SETPEND (Interrupt27)	Undefined		
26	SETPEND (Interrupt26)	Undefined		
25	SETPEND (Interrupt25)	Undefined		
24	SETPEND (Interrupt24)	Undefined		
23	SETPEND (Interrupt23)	Undefined		
22	SETPEND (Interrupt22)	Undefined		
21	SETPEND (Interrupt21)	Undefined		
20	SETPEND (Interrupt20)	Undefined		
19	SETPEND (Interrupt19)	Undefined		
18	SETPEND (Interrupt18)	Undefined		
17	SETPEND (Interrupt17)	Undefined		
16	SETPEND (Interrupt16)	Undefined		
15	SETPEND (Interrupt15)	Undefined		
14	SETPEND (Interrupt14)	Undefined		
13	SETPEND (Interrupt13)	Undefined		
12	SETPEND (Interrupt12)	Undefined		
11	SETPEND (Interrupt11)	Undefined		
10	SETPEND (Interrupt10)	Undefined		
9	SETPEND (Interrupt9)	Undefined		
8	SETPEND (Interrupt8)	Undefined		
7	SETPEND (Interrupt7)	Undefined		
6	SETPEND (Interrupt6)	Undefined		
5	SETPEND (Interrupt5)	Undefined		
4	SETPEND (Interrupt4)	Undefined		
3	SETPEND (Interrupt3)	Undefined		
2	SETPEND (Interrupt2)	Undefined		
1	SETPEND (Interrupt1)	Undefined		
0	SETPEND (Interrupt0)	Undefined		

(b) Interrupt Set-Pending Register 1

Bit	Bit Symbol	After Reset	Type	Function
31	SETPEND (Interrupt63)	Undefined	R/W	[Write] 1: Pend interrupt [Read] 0: Not pending 1: Pending
30	SETPEND (Interrupt62)	Undefined		
29	SETPEND (Interrupt61)	Undefined		
28	SETPEND (Interrupt60)	Undefined		
27	SETPEND (Interrupt59)	Undefined		
26	SETPEND (Interrupt58)	Undefined		
25	SETPEND (Interrupt57)	Undefined		
24	SETPEND (Interrupt56)	Undefined		
23	SETPEND (Interrupt55)	Undefined		
22	SETPEND (Interrupt54)	Undefined		
21	SETPEND (Interrupt53)	Undefined		
20	SETPEND (Interrupt52)	Undefined		
19	SETPEND (Interrupt51)	Undefined		
18	SETPEND (Interrupt50)	Undefined		
17	SETPEND (Interrupt49)	Undefined		
16	SETPEND (Interrupt48)	Undefined		
15	SETPEND (Interrupt47)	Undefined		
14	SETPEND (Interrupt46)	Undefined		
13	SETPEND (Interrupt45)	Undefined		
12	SETPEND (Interrupt44)	Undefined		
11	SETPEND (Interrupt43)	Undefined		
10	SETPEND (Interrupt42)	Undefined		
9	SETPEND (Interrupt41)	Undefined		
8	SETPEND (Interrupt40)	Undefined		
7	SETPEND (Interrupt39)	Undefined		
6	SETPEND (Interrupt38)	Undefined		
5	SETPEND (Interrupt37)	Undefined		
4	SETPEND (Interrupt36)	Undefined		
3	SETPEND (Interrupt35)	Undefined		
2	SETPEND (Interrupt34)	Undefined		
1	SETPEND (Interrupt33)	Undefined		
0	SETPEND (Interrupt32)	Undefined		

(c) Interrupt Set-Pending Register 2

Bit	Bit Symbol	After Reset	Type	Function
31	SETPEND (Interrupt95)	Undefined	R/W	[Write] 1: Pend interrupt [Read] 0: Not pending 1: Pending
30	SETPEND (Interrupt94)	Undefined		
29	SETPEND (Interrupt93)	Undefined		
28	SETPEND (Interrupt92)	Undefined		
27	SETPEND (Interrupt91)	Undefined		
26	SETPEND (Interrupt90)	Undefined		
25	SETPEND (Interrupt89)	Undefined		
24	SETPEND (Interrupt88)	Undefined		
23	SETPEND (Interrupt87)	Undefined		
22	SETPEND (Interrupt86)	Undefined		
21	SETPEND (Interrupt85)	Undefined		
20	SETPEND (Interrupt84)	Undefined		
19	SETPEND (Interrupt83)	Undefined		
18	SETPEND (Interrupt82)	Undefined		
17	SETPEND (Interrupt81)	Undefined		
16	SETPEND (Interrupt80)	Undefined		
15	SETPEND (Interrupt79)	Undefined		
14	SETPEND (Interrupt78)	Undefined		
13	SETPEND (Interrupt77)	Undefined		
12	SETPEND (Interrupt76)	Undefined		
11	SETPEND (Interrupt75)	Undefined		
10	SETPEND (Interrupt74)	Undefined		
9	SETPEND (Interrupt73)	Undefined		
8	SETPEND (Interrupt72)	Undefined		
7	SETPEND (Interrupt71)	Undefined		
6	SETPEND (Interrupt70)	Undefined		
5	SETPEND (Interrupt69)	Undefined		
4	SETPEND (Interrupt68)	Undefined		
3	SETPEND (Interrupt67)	Undefined		
2	SETPEND (Interrupt66)	Undefined		
1	SETPEND (Interrupt65)	Undefined		
0	SETPEND (Interrupt64)	Undefined		

(d) Interrupt Set-Pending Register 3

Bit	Bit Symbol	After Reset	Type	Function
31	SETPEND (Interrupt127)	Undefined	R/W	[Write] 1: Pend interrupt [Read] 0: Not pending 1: Pending
30	SETPEND (Interrupt126)	Undefined		
29	SETPEND Interrupt125)	Undefined		
28	SETPEND (Interrupt124)	Undefined		
27	SETPEND (Interrupt123)	Undefined		
26	SETPEND (Interrupt122)	Undefined		
25	SETPEND (Interrupt121)	Undefined		
24	SETPEND (Interrupt120)	Undefined		
23	SETPEND (Interrupt119)	Undefined		
22	SETPEND (Interrupt118)	Undefined		
21	SETPEND (Interrupt117)	Undefined		
20	SETPEND (Interrupt116)	Undefined		
19	SETPEND (Interrupt115)	Undefined		
18	SETPEND (Interrupt114)	Undefined		
17	SETPEND (Interrupt113)	Undefined		
16	SETPEND (Interrupt112)	Undefined		
15	SETPEND (Interrupt111)	Undefined		
14	SETPEND (Interrupt110)	Undefined		
13	SETPEND (Interrupt109)	Undefined		
12	SETPEND (Interrupt108)	Undefined		
11	SETPEND (Interrupt107)	Undefined		
10	SETPEND (Interrupt106)	Undefined		
9	SETPEND (Interrupt105)	Undefined		
8	SETPEND (Interrupt104)	Undefined		
7	SETPEND (Interrupt103)	Undefined		
6	SETPEND (Interrupt102)	Undefined		
5	SETPEND (Interrupt101)	Undefined		
4	SETPEND (Interrupt100)	Undefined		
3	SETPEND (Interrupt99)	Undefined		
2	SETPEND (Interrupt98)	Undefined		
1	SETPEND (Interrupt97)	Undefined		
0	SETPEND (Interrupt96)	Undefined		

(e) Interrupt Set-Pending Register 4

Bit	Bit Symbol	After Reset	Type	Function
31	-	Undefined	R/W	Write as "0".
30	-	Undefined	R/W	Write as "0".
29	-	Undefined	R/W	Write as "0".
28	-	Undefined	R/W	Write as "0".
27	SETPEND (Interrupt155)	Undefined	R/W	[Write] 1: Pend interrupt [Read] 0: Not pending 1: Pending
26	SETPEND (Interrupt154)	Undefined		
25	SETPEND (Interrupt153)	Undefined		
24	SETPEND (Interrupt152)	Undefined		
23	SETPEND (Interrupt151)	Undefined		
22	SETPEND (Interrupt150)	Undefined		
21	SETPEND (Interrupt149)	Undefined		
20	SETPEND (Interrupt148)	Undefined		
19	SETPEND (Interrupt147)	Undefined		
18	SETPEND (Interrupt146)	Undefined		
17	SETPEND (Interrupt145)	Undefined		
16	SETPEND (Interrupt144)	Undefined		
15	SETPEND (Interrupt143)	Undefined		
14	SETPEND (Interrupt142)	Undefined		
13	SETPEND (Interrupt141)	Undefined		
12	SETPEND (Interrupt140)	Undefined		
11	SETPEND (Interrupt139)	Undefined		
10	-	Undefined	R/W	Write as "0".
9	-	Undefined	R/W	Write as "0".
8	SETPEND (Interrupt136)	Undefined	R/W	[Write] 1: Pend interrupt [Read] 0: Not pending 1: Pending
7	SETPEND (Interrupt135)	Undefined		
6	SETPEND (Interrupt134)	Undefined		
5	SETPEND (Interrupt133)	Undefined		
4	SETPEND (Interrupt132)	Undefined		
3	SETPEND (Interrupt131)	Undefined		
2	SETPEND (Interrupt130)	Undefined		
1	SETPEND (Interrupt129)	Undefined		
0	SETPEND (Interrupt128)	Undefined		

(f) Interrupt Set-Pending Register 5

Bit	Bit Symbol	After Reset	Type	Function
31:15	-	Undefined	R	Read as "0".
14	SETPEND (Interrupt174)	Undefined	R/W	[Write] 1: Pend interrupt [Read] 0: Not pending 1: Pending
13	SETPEND (Interrupt173)	Undefined		
12	SETPEND (Interrupt172)	Undefined		
11	SETPEND (Interrupt171)	Undefined		
10	SETPEND (Interrupt170)	Undefined		
9	SETPEND (Interrupt169)	Undefined		
8	SETPEND (Interrupt168)	Undefined		
7	-	Undefined	R/W	Write as "0".
6	-	Undefined	R/W	Write as "0".
5	-	Undefined	R/W	Write as "0".
4	-	Undefined	R/W	Write as "0".
3	-	Undefined	R/W	Write as "0".
2	-	Undefined	R/W	Write as "0".
1	-	Undefined	R/W	Write as "0".
0	-	Undefined	R/W	Write as "0".

5.6.5.4. Interrupt Clear-Pending Register

Each bit corresponds to the specified number of interrupt. It can clear pending interrupts and determines which interrupts are currently pending.
Writing "1" to a bit in this register clears the corresponding pending interrupt. However, writing "1" has no effect on an interrupt that is already being serviced. Writing "0" has no effect.
Reading the bit returns the current state of the corresponding interrupts.

(a) Interrupt Clear-Pending Register 0

Bit	Bit Symbol	After Reset	Type	function
31	CLRPEND (Interrupt31)	Undefined	R/W	[Write] 1: Clear pending interrupt [Read] 0: Not pending 1: Pending
30	CLRPEND (Interrupt30)	Undefined		
29	CLRPEND (Interrupt29)	Undefined		
28	CLRPEND (Interrupt28)	Undefined		
27	CLRPEND (Interrupt27)	Undefined		
26	CLRPEND (Interrupt26)	Undefined		
25	CLRPEND (Interrupt25)	Undefined		
24	CLRPEND (Interrupt24)	Undefined		
23	CLRPEND (Interrupt23)	Undefined		
22	CLRPEND (Interrupt22)	Undefined		
21	CLRPEND (Interrupt21)	Undefined		
20	CLRPEND (Interrupt20)	Undefined		
19	CLRPEND (Interrupt19)	Undefined		
18	CLRPEND (Interrupt18)	Undefined		
17	CLRPEND (Interrupt17)	Undefined		
16	CLRPEND (Interrupt16)	Undefined		
15	CLRPEND (Interrupt15)	Undefined		
14	CLRPEND (Interrupt14)	Undefined		
13	CLRPEND (Interrupt13)	Undefined		
12	CLRPEND (Interrupt12)	Undefined		
11	CLRPEND (Interrupt11)	Undefined		
10	CLRPEND (Interrupt10)	Undefined		
9	CLRPEND (Interrupt9)	Undefined		
8	CLRPEND (Interrupt8)	Undefined		
7	CLRPEND (Interrupt7)	Undefined		
6	CLRPEND (Interrupt6)	Undefined		
5	CLRPEND (Interrupt5)	Undefined		
4	CLRPEND (Interrupt4)	Undefined		
3	CLRPEND (Interrupt3)	Undefined		
2	CLRPEND (Interrupt2)	Undefined		
1	CLRPEND (Interrupt1)	Undefined		
0	CLRPEND (Interrupt0)	Undefined		

(b) Interrupt Clear-Pending Register 1

Bit	Bit Symbol	After Reset	Type	Function
31	CLRPEND (Interrupt63)	Undefined	R/W	[Write] 1: Clear pending interrupt [Read] 0: Not pending 1: Pending
30	CLRPEND (Interrupt62)	Undefined		
29	CLRPEND (Interrupt61)	Undefined		
28	CLRPEND (Interrupt60)	Undefined		
27	CLRPEND (Interrupt59)	Undefined		
26	CLRPEND (Interrupt58)	Undefined		
25	CLRPEND (Interrupt57)	Undefined		
24	CLRPEND (Interrupt56)	Undefined		
23	CLRPEND (Interrupt55)	Undefined		
22	CLRPEND (Interrupt54)	Undefined		
21	CLRPEND (Interrupt53)	Undefined		
20	CLRPEND (Interrupt52)	Undefined		
19	CLRPEND (Interrupt51)	Undefined		
18	CLRPEND (Interrupt50)	Undefined		
17	CLRPEND (Interrupt49)	Undefined		
16	CLRPEND (Interrupt48)	Undefined		
15	CLRPEND (Interrupt47)	Undefined		
14	CLRPEND (Interrupt46)	Undefined		
13	CLRPEND (Interrupt45)	Undefined		
12	CLRPEND (Interrupt44)	Undefined		
11	CLRPEND (Interrupt43)	Undefined		
10	CLRPEND (Interrupt42)	Undefined		
9	CLRPEND (Interrupt41)	Undefined		
8	CLRPEND (Interrupt40)	Undefined		
7	CLRPEND (Interrupt39)	Undefined		
6	CLRPEND (Interrupt38)	Undefined		
5	CLRPEND (Interrupt37)	Undefined		
4	CLRPEND (Interrupt36)	Undefined		
3	CLRPEND (Interrupt35)	Undefined		
2	CLRPEND (Interrupt34)	Undefined		
1	CLRPEND (Interrupt33)	Undefined		
0	CLRPEND (Interrupt32)	Undefined		

(c) Interrupt Clear-Pending Register 2

Bit	Bit Symbol	After Reset	Type	Function
31	CLRPEND (Interrupt95)	Undefined	R/W	[Write] 1: Clear pending interrupt [Read] 0: Not pending 1: Pending
30	CLRPEND (Interrupt94)	Undefined		
29	CLRPEND (Interrupt93)	Undefined		
28	CLRPEND (Interrupt92)	Undefined		
27	CLRPEND (Interrupt91)	Undefined		
26	CLRPEND (Interrupt90)	Undefined		
25	CLRPEND (Interrupt89)	Undefined		
24	CLRPEND (Interrupt88)	Undefined		
23	CLRPEND (Interrupt87)	Undefined		
22	CLRPEND (Interrupt86)	Undefined		
21	CLRPEND (Interrupt85)	Undefined		
20	CLRPEND (Interrupt84)	Undefined		
19	CLRPEND (Interrupt83)	Undefined		
18	CLRPEND (Interrupt82)	Undefined		
17	CLRPEND (Interrupt81)	Undefined		
16	CLRPEND (Interrupt80)	Undefined		
15	CLRPEND (Interrupt79)	Undefined		
14	CLRPEND (Interrupt78)	Undefined		
13	CLRPEND (Interrupt77)	Undefined		
12	CLRPEND (Interrupt76)	Undefined		
11	CLRPEND (Interrupt75)	Undefined		
10	CLRPEND (Interrupt74)	Undefined		
9	CLRPEND (Interrupt73)	Undefined		
8	CLRPEND (Interrupt72)	Undefined		
7	CLRPEND (Interrupt71)	Undefined		
6	CLRPEND (Interrupt70)	Undefined		
5	CLRPEND (Interrupt69)	Undefined		
4	CLRPEND (Interrupt68)	Undefined		
3	CLRPEND (Interrupt67)	Undefined		
2	CLRPEND (Interrupt66)	Undefined		
1	CLRPEND (Interrupt65)	Undefined		
0	CLRPEND (Interrupt64)	Undefined		

(d) Interrupt Clear-Pending Register 3

Bit	Bit Symbol	After Reset	Type	Function
31	CLRPEND (Interrupt127)	Undefined	R/W	[Write] 1: Clear pending interrupt [Read] 0: Not pending 1: Pending
30	CLRPEND (Interrupt126)	Undefined		
29	CLRPEND (Interrupt125)	Undefined		
28	CLRPEND (Interrupt124)	Undefined		
27	CLRPEND (Interrupt123)	Undefined		
26	CLRPEND (Interrupt122)	Undefined		
25	CLRPEND (Interrupt121)	Undefined		
24	CLRPEND (Interrupt120)	Undefined		
23	CLRPEND (Interrupt119)	Undefined		
22	CLRPEND (Interrupt118)	Undefined		
21	CLRPEND (Interrupt117)	Undefined		
20	CLRPEND (Interrupt116)	Undefined		
19	CLRPEND (Interrupt115)	Undefined		
18	CLRPEND (Interrupt114)	Undefined		
17	CLRPEND (Interrupt113)	Undefined		
16	CLRPEND (Interrupt112)	Undefined		
15	CLRPEND (Interrupt111)	Undefined		
14	CLRPEND (Interrupt110)	Undefined		
13	CLRPEND (Interrupt109)	Undefined		
12	CLRPEND (Interrupt108)	Undefined		
11	CLRPEND (Interrupt107)	Undefined		
10	CLRPEND (Interrupt106)	Undefined		
9	CLRPEND (Interrupt105)	Undefined		
8	CLRPEND (Interrupt104)	Undefined		
7	CLRPEND (Interrupt103)	Undefined		
6	CLRPEND (Interrupt102)	Undefined		
5	CLRPEND (Interrupt101)	Undefined		
4	CLRPEND (Interrupt100)	Undefined		
3	CLRPEND (Interrupt99)	Undefined		
2	CLRPEND (Interrupt98)	Undefined		
1	CLRPEND (Interrupt97)	Undefined		
0	CLRPEND (Interrupt96)	Undefined		

(e) Interrupt Clear-Pending Register 4

Bit	Bit Symbol	After Reset	Type	Function
31	-	Undefined	R/W	Write as "1".
30	-	Undefined	R/W	Write as "1".
29	-	Undefined	R/W	Write as "1".
28	-	Undefined	R/W	Write as "1".
27	CLRPEND (Interrupt155)	Undefined	R/W	[Write] 1: Clear pending interrupt [Read] 0: Not pending 1: Pending
26	CLRPEND (Interrupt154)	Undefined		
25	CLRPEND (Interrupt153)	Undefined		
24	CLRPEND (Interrupt152)	Undefined		
23	CLRPEND (Interrupt151)	Undefined		
22	CLRPEND (Interrupt150)	Undefined		
21	CLRPEND (Interrupt149)	Undefined		
20	CLRPEND (Interrupt148)	Undefined		
19	CLRPEND (Interrupt147)	Undefined		
18	CLRPEND (Interrupt146)	Undefined		
17	CLRPEND (Interrupt145)	Undefined		
16	CLRPEND (Interrupt144)	Undefined		
15	CLRPEND (Interrupt143)	Undefined		
14	CLRPEND (Interrupt142)	Undefined		
13	CLRPEND (Interrupt141)	Undefined		
12	CLRPEND (Interrupt140)	Undefined		
11	CLRPEND (Interrupt139)	Undefined		
10	-	Undefined	R/W	Write as "1".
9	-	Undefined	R/W	Write as "1".
8	CLRPEND (Interrupt136)	Undefined	R/W	[Write] 1: Clear pending interrupt [Read] 0: Not pending 1: Pending
7	CLRPEND (Interrupt135)	Undefined		
6	CLRPEND (Interrupt134)	Undefined		
5	CLRPEND (Interrupt133)	Undefined		
4	CLRPEND (Interrupt132)	Undefined		
3	CLRPEND (Interrupt131)	Undefined		
2	CLRPEND (Interrupt130)	Undefined		
1	CLRPEND (Interrupt129)	Undefined		
0	CLRPEND (Interrupt128)	Undefined		

(f) Interrupt Clear-Pending Register 5

Bit	Bit Symbol	After Reset	Type	Function
31:15	-	Undefined	R	Read as "0".
14	CLRPEND (Interrupt174)	Undefined	R/W	[Write] 1: Clear pending interrupt [Read] 0: Not pending 1: Pending
13	CLRPEND (Interrupt173)	Undefined		
12	CLRPEND (Interrupt172)	Undefined		
11	CLRPEND (Interrupt171)	Undefined		
10	CLRPEND (Interrupt170)	Undefined		
9	CLRPEND (Interrupt169)	Undefined		
8	CLRPEND (Interrupt168)	Undefined		
7	-	Undefined	R/W	Write as "1".
6	-	Undefined	R/W	Write as "1".
5	-	Undefined	R/W	Write as "1".
4	-	Undefined	R/W	Write as "1".
3	-	Undefined	R/W	Write as "1".
2	-	Undefined	R/W	Write as "1".
1	-	Undefined	R/W	Write as "1".
0	-	Undefined	R/W	Write as "1".

5.6.6. Interrupt Priority Register

Each interrupt is provided with eight bits of an Interrupt Priority Register.
The following shows the addresses of the Interrupt Priority Registers corresponding to interrupt numbers.

Address	31 24	23 16	15 8	7 0
0xE000E400	PRI_3	PRI_2	PRI_1	PRI_0
0xE000E404	PRI_7	PRI_6	PRI_5	PRI_4
0xE000E408	PRI_11	PRI_10	PRI_9	PRI_8
0xE000E40C	PRI_15	PRI_14	PRI_13	PRI_12
0xE000E410	PRI_19	PRI_18	PRI_17	PRI_16
0xE000E414	PRI_23	PRI_22	PRI_21	PRI_20
0xE000E418	PRI_27	PRI_26	PRI_25	PRI_24
0xE000E41C	PRI_31	PRI_30	PRI_29	PRI_28
0xE000E420	PRI_35	PRI_34	PRI_33	PRI_32
0xE000E424	PRI_39	PRI_38	PRI_37	PRI_36
0xE000E428	PRI_43	PRI_42	PRI_41	PRI_40
0xE000E42C	PRI_47	PRI_46	PRI_45	PRI_44
0xE000E430	PRI_51	PRI_50	PRI_49	PRI_48
0xE000E434	PRI_55	PRI_54	PRI_53	PRI_52
0xE000E438	PRI_59	PRI_58	PRI_57	PRI_56
0xE000E43C	PRI_63	PRI_62	PRI_61	PRI_60
0xE000E440	PRI_67	PRI_66	PRI_65	PRI_64
0xE000E444	PRI_71	PRI_70	PRI_69	PRI_68
0xE000E448	PRI_75	PRI_74	PRI_73	PRI_72
0xE000E44C	PRI_79	PRI_78	PRI_77	PRI_76
0xE000E450	PRI_83	PRI_82	PRI_81	PRI_80
0xE000E454	PRI_87	PRI_86	PRI_85	PRI_84
0xE000E458	PRI_91	PRI_90	PRI_89	PRI_88
0xE000E45C	PRI_95	PRI_94	PRI_93	PRI_92
0xE000E460	PRI_99	PRI_98	PRI_97	PRI_96
0xE000E464	PRI_103	PRI_102	PRI_101	PRI_100
0xE000E468	PRI_107	PRI_106	PRI_105	PRI_104
0xE000E46C	PRI_111	PRI_110	PRI_109	PRI_108
0xE000E470	PRI_115	PRI_114	PRI_113	PRI_112
0xE000E474	PRI_119	PRI_118	PRI_117	PRI_116
0xE000E478	PRI_123	PRI_122	PRI_121	PRI_120
0xE000E47C	PRI_127	PRI_126	PRI_125	PRI_124
0xE000E480	PRI_131	PRI_130	PRI_129	PRI_128
0xE000E484	PRI_135	PRI_134	PRI_133	PRI_132
0xE000E488	PRI_139	-	-	PRI_136
0xE000E48C	PRI_143	PRI_142	PRI_141	PRI_140
0xE000E490	PRI_147	PRI_146	PRI_145	PRI_144
0xE000E494	PRI_151	PRI_150	PRI_149	PRI_148
0xE000E498	PRI_155	PRI_154	PRI_153	PRI_152
0xE000E49C	-	-	-	-
0xE000E4A0	-	-	-	-
0xE000E4A4	-	-	-	-
0xE000E4A8	PRI_171	PRI_170	PRI_169	PRI_168
0xE000E4AC	-	PRI_174	PRI_173	PRI_172

The number of bits to be used for assigning a priority varies with each product. This product uses four bits for assigning a priority.
The following shows the fields of the Interrupt Priority Registers for interrupt numbers 0 to 3. The Interrupt Priority Registers for all other interrupt numbers have the identical fields. Unused bits return "0" when read, and writing to unused bits has no effect.

Bit	Bit Symbol	After Reset	Type	Function
31:28	PRI_3[3:0]	0000	R/W	Priority of interrupt number 3
27:24	-	0	R	Read as "0".
23:20	PRI_2[3:0]	0000	R/W	Priority of interrupt number 2
19:16	-	0	R	Read as "0".
15:12	PRI_1[3:0]	0000	R/W	Priority of interrupt number 1
11:8	-	0	R	Read as "0".
7:4	PRI_0[3:0]	0000	R/W	Priority of interrupt number 0
3:0	-	0	R	Read as "0".

5.6.7. Vector Table Offset Register

Bit	Bit Symbol	After Reset	Type	Function
31:7	TBLOFF[24:0]	0x0000000	R/W	Offset value Set the offset value from the address of 0x00000000. The offset must be aligned based on the number of exceptions in the table. This means that the minimum alignment is 32 words that you can use for up to 16 interrupts. For more interrupts, you must adjust the alignment by rounding up to the next power of two.
6:0	-	0	R	Read as "0".

5.6.8. Application Interrupt and Reset Control Register

Bit	Bit Symbol	After Reset	Type	Function
31:16	VECTKEY/ VECTKEYSTAT[15:0]	Undefined	W	Register key Writing to this register requires 0x5FA in the <VECTKEY> field.
			R	Register key Read as "0xFA05".
15	ENDIANESS	0	R/W	Endianness bit: (Note1) 1: Big endian 0: Little endian
14:11	-	0	R	Read as "0".
10:8	PRIGROUP[2:0]	000	R/W	Interrupt priority grouping 000: seven bits of pre-emption priority, one bit of sub priority 001: six bits of pre-emption priority, two bits of sub priority 010: five bits of pre-emption priority, three bits of sub priority 011: four bits of pre-emption priority, four bits of sub priority 100: three bits of pre-emption priority, five bits of sub priority 101: two bits of pre-emption priority, six bits of sub priority 110: one bit of pre-emption priority, seven bits of sub priority 111: no pre-emption priority, eight bits of sub priority The bit configuration to split the interrupt priority register <PRI_n> into pre-emption priority and sub priority.
7:3	-	0	R	Read as "0".
2	SYSRESETREQ	0	R/W	System Reset Request 1: CPU outputs a SYSRESETREQ signal. (Note2)
1	VECTCLRACTIVE	0	R/W	Clear active vector bit 1: Clear all state information for active NMI, fault, and interrupts. 0: Do not clear. This bit self-clears. It is the responsibility of the application to reinitialize the stack.
0	VECTRESET	0	R/W	System Reset bit 1: Reset system. 0: Do not reset system. Resets the system, with the exception of debug components (FPB, DWT and ITM) by setting "1" and this bit is also zero cleared.

Note 1: Little-endian is the default memory format for this product.

Note 2: When SYSRESETREQ is output, warm reset is performed on this product. <SYSRESETREQ> is cleared by the warm reset.

5.6.9. System Handler Priority Register

Each exception is provided with eight bits of a System Handler Priority Register.
The following shows the addresses of the System Handler Priority Registers corresponding to each exception.

Address	31 24	23 16	15 8	7 0
0xE000ED18	PRI_7	PRI_6 (Usage Fault)	PRI_5 (Bus Fault)	PRI_4 (Memory Management)
0xE000ED1C	PRI_11 (SVCall)	PRI_10	PRI_9	PRI_8
0xE000ED20	PRI_15 (SysTick)	PRI_14 (PendSV)	PRI_13	PRI_12 (Debug Monitor)

The number of bits to be used for assigning a priority varies with each product. This product uses four bits for assigning a priority.

The following shows the fields of the System Handler Priority Registers for Usage Fault, Bus Fault , and Memory Management. Unused bits return "0" when read, and writing to unused bits has no effect.

Bit	Bit Symbol	After Reset	Type	Function
31:28	PRI_7[3:0]	0000	R/W	Reserved.
27:24	-	0	R	Read as "0".
23:20	PRI_6[3:0]	0000	R/W	Priority of Usage Fault
19:16	-	0	R	Read as "0".
15:12	PRI_5[3:0]	0000	R/W	Priority of Bus Fault
11:8	-	0	R	Read as "0".
7:4	PRI_4[3:0]	0000	R/W	Priority of Memory Management
3:0	-	0	R	Read as "0".

5.6.10. System Handler Control and State Register

Bit	Bit Symbol	After Reset	Type	Function
31:19	-	0	R	Read as "0"
18	USGFAULT ENA	0	R/W	Usage Fault 0: Disabled. 1: Enabled.
17	BUSFAULT ENA	0	R/W	Bus Fault 0: Disabled. 1: Enabled.
16	MEMFAULT ENA	0	R/W	Memory Management 0: Disabled. 1: Enabled.
15	SVCALL PENDED	0	R/W	SVCall 0: Not pended. 1: Pended.
14	BUSFAULT PENDED	0	R/W	Bus Fault 0: Not pended. 1: Pended.
13	MEMFAULT PENDED	0	R/W	Memory Management 0: Not pended. 1: Pended.
12	USGFAULT PENDED	0	R/W	Usage fault 0: Not pended. 1: Pended.
11	SYSTICKACT	0	R/W	SysTick 0: Inactive 1: Active
10	PENDSVACT	0	R/W	PendSV 0: Inactive 1: Active
9	-	0	R	Read as "0".
8	MONITOR ACT	0	R/W	Debug Monitor 0: Inactive 1: Active
7	SVCALLACT	0	R/W	SVCall 0: Inactive 1: Active
6:4	-	0	R	Read as "0"
3	USGFAULT ACT	0	R/W	Usage Fault 0: Inactive 1: Active
2	-	0	R	Read as "0"
1	BUSFAULT ACT	0	R/W	Bus Fault 0: Inactive 1: Active
0	MEMFAULT ACT	0	R/W	Memory Management 0: Inactive 1: Active

Note: You must clear or set the active bits with extreme caution because clearing or setting these bits does not repair stack contents.

6. List of Interrupt Factors for Each Product

6.1. TMPM4GR/TMPM4GQ/TMPM4GN

Table 6.1 List of Interrupt Factors (1/12)

Interrupt No.	Interrupt Source	Interrupt Request	Interrupt Control Register	Interrupt Monitor Register	M4GR	M4GQ	M4GN
NMI Interrupt	INTLVD	LVD interrupt	***[IANIC00]***	***[IMNFLGNMI]*** <INT000FLG>	✓	✓	✓
	INTWDT0	WDT interrupt	***[IBNIC00]***	***[IMNFLGNMI]*** <INT016FLG>	✓	✓	✓
0	INT00	External interrupt 00a	***[IAIMC00]***	***[IMNFLG1]*** <INT032FLG>	✓	✓	✓
		External interrupt 00b	***[IAIMC01]***	***[IMNFLG1]*** <INT033FLG>	✓	✓	✓
1	INT01	External interrupt 01a	***[IAIMC02]***	***[IMNFLG1]*** <INT034FLG>	✓	✓	✓
		External interrupt 01b	***[IAIMC03]***	***[IMNFLG1]*** <INT035FLG>	✓	✓	-
2	INT02	External interrupt 02a	***[IAIMC04]***	***[IMNFLG1]*** <INT036FLG>	✓	✓	✓
		External interrupt 02b	***[IAIMC05]***	***[IMNFLG1]*** <INT037FLG>	✓	✓	-
3	INT03	External interrupt 03a	***[IAIMC06]***	***[IMNFLG1]*** <INT038FLG>	✓	✓	✓
		External interrupt 03b	***[IAIMC07]***	***[IMNFLG1]*** <INT039FLG>	✓	-	-
4	INT04	External interrupt 04a	***[IAIMC08]***	***[IMNFLG1]*** <INT040FLG>	✓	✓	✓
		External interrupt 04b	***[IAIMC09]***	***[IMNFLG1]*** <INT041FLG>	✓	✓	✓
5	INT05	External interrupt 05a	***[IAIMC10]***	***[IMNFLG1]*** <INT042FLG>	✓	✓	✓
		External interrupt 05b	***[IAIMC11]***	***[IMNFLG1]*** <INT043FLG>	✓	✓	✓
6	INT06	External interrupt 06a	***[IAIMC12]***	***[IMNFLG1]*** <INT044FLG>	✓	✓	✓
		External interrupt 06b	***[IAIMC13]***	***[IMNFLG1]*** <INT045FLG>	✓	-	-
7	INT07	External interrupt 07a	***[IAIMC14]***	***[IMNFLG1]*** <INT046FLG>	✓	✓	✓
		External interrupt 07b	***[IAIMC15]***	***[IMNFLG1]*** <INT047FLG>	✓	-	-
8	INT08	External interrupt 08a	***[IAIMC16]***	***[IMNFLG1]*** <INT048FLG>	✓	✓	✓
		External interrupt 08b	***[IAIMC17]***	***[IMNFLG1]*** <INT049FLG>	✓	-	-
9	INT09	External interrupt 09a	***[IAIMC18]***	***[IMNFLG1]*** <INT050FLG>	✓	✓	✓
		External interrupt 09b	***[IAIMC19]***	***[IMNFLG1]*** <INT051FLG>	✓	-	-
10	INT10	External interrupt 10a	***[IAIMC20]***	***[IMNFLG1]*** <INT052FLG>	✓	✓	✓
		External interrupt 10b	***[IAIMC21]***	***[IMNFLG1]*** <INT053FLG>	✓	✓	✓

Note: ✓: Available, -: N/A

Table 6.2 List of Interrupt Factors (2/12)

Interrupt No.	Interrupt Source	Interrupt Request	Interrupt Control Register	Interrupt Monitor Register	M4GR	M4GQ	M4GN
11	INT11	External interrupt 11a	*[IAIMC22]*	*[IMNFLG1]* <INT054FLG>	✓	✓	✓
		External interrupt 11b	*[IAIMC23]*	*[IMNFLG1]* <INT055FLG>	✓	✓	✓
12	INT12	External interrupt 12a	*[IAIMC24]*	*[IMNFLG1]* <INT056FLG>	✓	✓	-
		External interrupt 12b	*[IAIMC25]*	*[IMNFLG1]* <INT057FLG>	✓	-	-
13	INT13	External interrupt 13a	*[IAIMC26]*	*[IMNFLG1]* <INT058FLG>	✓	✓	-
		External interrupt 13b	*[IAIMC27]*	*[IMNFLG1]* <INT059FLG>	✓	-	-
14	INT14	External interrupt 14a	*[IAIMC28]*	*[IMNFLG1]* <INT060FLG>	✓	✓	-
		External interrupt 14b	*[IAIMC29]*	*[IMNFLG1]* <INT061FLG>	✓	✓	-
15	INT15	External interrupt 15a	*[IAIMC30]*	*[IMNFLG1]* <INT062FLG>	✓	✓	-
		External interrupt 15b	*[IAIMC31]*	*[IMNFLG1]* <INT063FLG>	✓	✓	-
16	INTRTC	RTC interrupt	*[IAIMC49]*	*[IMNFLG2]* <INT081FLG>	✓	✓	✓
17	INTCEC0RX	CEC ch0 reception interrupt	*[IAIMC50]*	*[IMNFLG2]* <INT082FLG>	✓	✓	✓
18	INTCEC0TX	CEC ch0 transmission interrupt	*[IAIMC51]*	*[IMNFLG2]* <INT083FLG>	✓	✓	✓
19	INTISDA	ISD unit A interrupt	*[IAIMC52]*	*[IMNFLG2]* <INT084FLG>	✓	✓	✓
20	INTISDB	ISD unit B interrupt	*[IAIMC53]*	*[IMNFLG2]* <INT085FLG>	✓	✓	-
21	INTISDC	ISD unit C interrupt	*[IAIMC54]*	*[IMNFLG2]* <INT086FLG>	✓	-	-
22	INTRMC0	RMC ch0 Remote controller interrupt	*[IAIMC55]*	*[IMNFLG2]* <INT087FLG>	✓	✓	✓
23	INTRMC1	RMC ch1 Remote controller interrupt	*[IAIMC56]*	*[IMNFLG2]* <INT088FLG>	✓	✓	-
24	INTLTTMR0	LTTMR ch0 interrupt	*[IAIMC57]*	*[IMNFLG2]* <INT089FLG>	✓	✓	✓
25	INTHDMAATC	HDMA unit A transfer end			✓	✓	✓
26	INTHDMAAERR	HDMA unit A transfer error			✓	✓	✓
27	INTHDMABTC	HDMA unit B transfer end			✓	✓	✓
28	INTHDMABERR	HDMA unit B transfer error			✓	✓	✓
29	INTMDMAATC	MDMA unit A transfer end			✓	✓	✓
30	INTT32A00_A_CT	T32A ch0 Timer A match, overflow, and underflow	*[IBIMC000]*	*[IMNFLG3]* <INT096FLG>	✓	✓	✓
		T32A ch0 Timer A capture 0	*[IBIMC001]*	*[IMNFLG3]* <INT097FLG>	✓	✓	✓
		T32A ch0 Timer A capture 1	*[IBIMC002]*	*[IMNFLG3]* <INT098FLG>	✓	✓	✓
		T32A ch0 Timer C match, overflow, and underflow	*[IBIMC006]*	*[IMNFLG3]* <INT102FLG>	✓	✓	✓

Note: ✓: Available, -: N/A

Table 6.3 List of Interrupt Factors (3/12)

Interrupt No.	Interrupt Source	Interrupt Request	Interrupt Control Register	Interrupt Monitor Register	M4GR	M4GQ	M4GN
31	INTT32A00_B_C01_CPC	T32A ch0 Timer B match, overflow, and underflow	***[IBIMC003]***	***[IMNFLG3]*** <INT099FLG>	✓	✓	✓
		T32A ch0 Timer B capture 0	***[IBIMC004]***	***[IMNFLG3]*** <INT100FLG>	✓	✓	✓
		T32A ch0 Timer B capture 1	***[IBIMC005]***	***[IMNFLG3]*** <INT101FLG>	✓	✓	✓
		T32A ch0 Timer C capture 0	***[IBIMC007]***	***[IMNFLG3]*** <INT103FLG>	✓	✓	✓
		T32A ch0 Timer C capture 1	***[IBIMC008]***	***[IMNFLG3]*** <INT104FLG>	✓	✓	✓
		T32A ch0 Timer C pulse count	***[IBIMC009]***	***[IMNFLG3]*** <INT105FLG>	✓	✓	✓
32	INTT32A01_A_CT	T32A ch1 Timer A match, overflow, and underflow	***[IBIMC010]***	***[IMNFLG3]*** <INT106FLG>	✓	✓	✓
		T32A ch1 Timer A capture 0	***[IBIMC011]***	***[IMNFLG3]*** <INT107FLG>	✓	✓	✓
		T32A ch1 Timer A capture 1	***[IBIMC012]***	***[IMNFLG3]*** <INT108FLG>	✓	✓	✓
		T32A ch1 Timer C match, overflow, and underflow	***[IBIMC016]***	***[IMNFLG3]*** <INT112FLG>	✓	✓	✓
33	INTT32A01_B_C01_CPC	T32A ch1 Timer B match, overflow, and underflow	***[IBIMC013]***	***[IMNFLG3]*** <INT109FLG>	✓	✓	✓
		T32A ch1 Timer B capture 0	***[IBIMC014]***	***[IMNFLG3]*** <INT110FLG>	✓	✓	✓
		T32A ch1 Timer B capture 1	***[IBIMC015]***	***[IMNFLG3]*** <INT111FLG>	✓	✓	✓
		T32A ch1 Timer C capture 0	***[IBIMC017]***	***[IMNFLG3]*** <INT113FLG>	✓	✓	✓
		T32A ch1 Timer C capture 1	***[IBIMC018]***	***[IMNFLG3]*** <INT114FLG>	✓	✓	✓
		T32A ch1 Timer C pulse count	***[IBIMC019]***	***[IMNFLG3]*** <INT115FLG>	✓	✓	✓
34	INTT32A02_A_CT	T32A ch2 Timer A match, overflow, and underflow	***[IBIMC020]***	***[IMNFLG3]*** <INT116FLG>	✓	✓	✓
		T32A ch2 Timer A capture 0	***[IBIMC021]***	***[IMNFLG3]*** <INT117FLG>	✓	✓	✓
		T32A ch2 Timer A capture 1	***[IBIMC022]***	***[IMNFLG3]*** <INT118FLG>	✓	✓	✓
		T32A ch2 Timer C match, overflow, and underflow	***[IBIMC026]***	***[IMNFLG3]*** <INT122FLG>	✓	✓	✓
35	INTT32A02_B_C01_CPC	T32A ch2 Timer B match, overflow, and underflow	***[IBIMC023]***	***[IMNFLG3]*** <INT119FLG>	✓	✓	✓
		T32A ch2 Timer B capture 0	***[IBIMC024]***	***[IMNFLG3]*** <INT120FLG>	✓	✓	✓
		T32A ch2 Timer B capture 1	***[IBIMC025]***	***[IMNFLG3]*** <INT121FLG>	✓	✓	✓
		T32A ch2 Timer C capture 0	***[IBIMC027]***	***[IMNFLG3]*** <INT123FLG>	✓	✓	✓
		T32A ch2 Timer C capture 1	***[IBIMC028]***	***[IMNFLG3]*** <INT124FLG>	✓	✓	✓
		T32A ch2 Timer C pulse count	***[IBIMC029]***	***[IMNFLG3]*** <INT125FLG>	✓	✓	✓

Note: ✓: Available, -: N/A

Table 6.4 List of Interrupt Factors (4/12)

Interrupt No.	Interrupt Source	Interrupt Request	Interrupt Control Register	Interrupt Monitor Register	M4GR	M4GQ	M4GN
36	INTT32A03_A_CT	T32A ch3 Timer A match, overflow, and underflow	***[IBIMC030]***	***[IMNFLG3]*** <INT126FLG>	✓	✓	✓
		T32A ch3 Timer A capture 0	***[IBIMC031]***	***[IMNFLG3]*** <INT127FLG>	✓	✓	✓
		T32A ch3 Timer A capture 1	***[IBIMC032]***	***[IMNFLG4]*** <INT128FLG>	✓	✓	✓
		T32A ch3 Timer C match, overflow, and underflow	***[IBIMC036]***	***[IMNFLG4]*** <INT132FLG>	✓	✓	✓
37	INTT32A03_B_C01_CPC	T32A ch3 Timer B match, overflow, and underflow	***[IBIMC033]***	***[IMNFLG4]*** <INT129FLG>	✓	✓	✓
		T32A ch3 Timer B capture 0	***[IBIMC034]***	***[IMNFLG4]*** <INT130FLG>	✓	✓	✓
		T32A ch3 Timer B capture 1	***[IBIMC035]***	***[IMNFLG4]*** <INT131FLG>	✓	✓	✓
		T32A ch3 Timer C capture 0	***[IBIMC037]***	***[IMNFLG4]*** <INT133FLG>	✓	✓	✓
		T32A ch3 Timer C capture 1	***[IBIMC038]***	***[IMNFLG4]*** <INT134FLG>	✓	✓	✓
		T32A ch3 Timer C pulse count	***[IBIMC039]***	***[IMNFLG4]*** <INT135FLG>	✓	✓	✓
38	INTT32A04_A_CT	T32A ch4 Timer A match, overflow, and underflow	***[IBIMC040]***	***[IMNFLG4]*** <INT136FLG>	✓	✓	✓
		T32A ch4 Timer A capture 0	***[IBIMC041]***	***[IMNFLG4]*** <INT137FLG>	✓	✓	✓
		T32A ch4 Timer A capture 1	***[IBIMC042]***	***[IMNFLG4]*** <INT138FLG>	✓	✓	✓
		T32A ch4 Timer C match, overflow, and underflow	***[IBIMC046]***	***[IMNFLG4]*** <INT142FLG>	✓	✓	✓
39	INTT32A04_B_C01_CPC	T32A ch4 Timer B match, overflow, and underflow	***[IBIMC043]***	***[IMNFLG4]*** <INT139FLG>	✓	✓	✓
		T32A ch4 Timer B capture 0	***[IBIMC044]***	***[IMNFLG4]*** <INT140FLG>	✓	✓	✓
		T32A ch4 Timer B capture 1	***[IBIMC045]***	***[IMNFLG4]*** <INT141FLG>	✓	✓	✓
		T32A ch4 Timer C capture 0	***[IBIMC047]***	***[IMNFLG4]*** <INT143FLG>	✓	✓	✓
		T32A ch4 Timer C capture 1	***[IBIMC048]***	***[IMNFLG4]*** <INT144FLG>	✓	✓	✓
		T32A ch4 Timer C pulse count	***[IBIMC049]***	***[IMNFLG4]*** <INT145FLG>	✓	✓	✓
40	INTT32A05_A_CT	T32A ch5 Timer A match, overflow, and underflow	***[IBIMC050]***	***[IMNFLG4]*** <INT146FLG>	✓	✓	✓
		T32A ch5 Timer A capture 0	***[IBIMC051]***	***[IMNFLG4]*** <INT147FLG>	✓	✓	✓
		T32A ch5 Timer A capture 1	***[IBIMC052]***	***[IMNFLG4]*** <INT148FLG>	✓	✓	✓
		T32A ch5 Timer C match, overflow, and underflow	***[IBIMC056]***	***[IMNFLG4]*** <INT152FLG>	✓	✓	✓

Note: ✓: Available, -: N/A

Table 6.5 List of Interrupt Factors (5/12)

Interrupt No.	Interrupt Source	Interrupt Request	Interrupt Control Register	Interrupt Monitor Register	M4GR	M4GQ	M4GN
41	INTT32A05_B_C01_CPC	T32A ch5 Timer B match, overflow, and underflow	***[IBIMC053]***	***[IMNFLG4]*** <INT149FLG>	✓	✓	✓
		T32A ch5 Timer B capture 0	***[IBIMC054]***	***[IMNFLG4]*** <INT150FLG>	✓	✓	✓
		T32A ch5 Timer B capture 1	***[IBIMC055]***	***[IMNFLG4]*** <INT151FLG>	✓	✓	✓
		T32A ch5 Timer C capture 0	***[IBIMC057]***	***[IMNFLG4]*** <INT153FLG>	✓	✓	✓
		T32A ch5 Timer C capture 1	***[IBIMC058]***	***[IMNFLG4]*** <INT154FLG>	✓	✓	✓
		T32A ch5 Timer C pulse count	***[IBIMC059]***	***[IMNFLG4]*** <INT155FLG>	✓	✓	✓
42	INTT32A06_A_CT	T32A ch6 Timer A match, overflow, and underflow	***[IBIMC060]***	***[IMNFLG4]*** <INT156FLG>	✓	✓	✓
		T32A ch6 Timer A capture 0	***[IBIMC061]***	***[IMNFLG4]*** <INT157FLG>	✓	✓	✓
		T32A ch6 Timer A capture 1	***[IBIMC062]***	***[IMNFLG4]*** <INT158FLG>	✓	✓	✓
		T32A ch6 Timer C match, overflow, and underflow	***[IBIMC066]***	***[IMNFLG5]*** <INT162FLG>	✓	✓	✓
43	INTT32A06_B_C01_CPC	T32A ch6 Timer B match, overflow, and underflow	***[IBIMC063]***	***[IMNFLG4]*** <INT159FLG>	✓	✓	✓
		T32A ch6 Timer B capture 0	***[IBIMC064]***	***[IMNFLG5]*** <INT160FLG>	✓	✓	✓
		T32A ch6 Timer B capture 1	***[IBIMC065]***	***[IMNFLG5]*** <INT161FLG>	✓	✓	✓
		T32A ch6 Timer C capture 0	***[IBIMC067]***	***[IMNFLG5]*** <INT163FLG>	✓	✓	✓
		T32A ch6 Timer C capture 1	***[IBIMC068]***	***[IMNFLG5]*** <INT164FLG>	✓	✓	✓
		T32A ch6 Timer C pulse count	***[IBIMC069]***	***[IMNFLG5]*** <INT165FLG>	✓	✓	✓
44	INTT32A07_A_CT	T32A ch7 Timer A match, overflow, and underflow	***[IBIMC070]***	***[IMNFLG5]*** <INT166FLG>	✓	✓	✓
		T32A ch7 Timer A capture 0	***[IBIMC071]***	***[IMNFLG5]*** <INT167FLG>	✓	✓	✓
		T32A ch7 Timer A capture 1	***[IBIMC072]***	***[IMNFLG5]*** <INT168FLG>	✓	✓	✓
		T32A ch7 Timer C match, overflow, and underflow	***[IBIMC076]***	***[IMNFLG5]*** <INT172FLG>	✓	✓	✓
45	INTT32A07_B_C01_CPC	T32A ch7 Timer B match, overflow, and underflow	***[IBIMC073]***	***[IMNFLG5]*** <INT169FLG>	✓	✓	✓
		T32A ch7 Timer B capture 0	***[IBIMC074]***	***[IMNFLG5]*** <INT170FLG>	✓	✓	✓
		T32A ch7 Timer B capture 1	***[IBIMC075]***	***[IMNFLG5]*** <INT171FLG>	✓	✓	✓
		T32A ch7 Timer C capture 0	***[IBIMC077]***	***[IMNFLG5]*** <INT173FLG>	✓	✓	✓
		T32A ch7 Timer C capture 1	***[IBIMC078]***	***[IMNFLG5]*** <INT174FLG>	✓	✓	✓
		T32A ch7 Timer C pulse count	***[IBIMC079]***	***[IMNFLG5]*** <INT175FLG>	✓	✓	✓

Note: ✓: Available, -: N/A

Table 6.6 List of Interrupt Factors (6/12)

Interrupt No.	Interrupt Source	Interrupt Request	Interrupt Control Register	Interrupt Monitor Register	M4GR	M4GQ	M4GN
46	INTT32A08_A_CT	T32A ch8 Timer A match, overflow, and underflow	***[IBIMC080]***	***[IMNFLG5]*** <INT176FLG>	✓	✓	✓
		T32A ch8 Timer A capture 0	***[IBIMC081]***	***[IMNFLG5]*** <INT177FLG>	✓	✓	✓
		T32A ch8 Timer A capture 1	***[IBIMC082]***	***[IMNFLG5]*** <INT178FLG>	✓	✓	✓
		T32A ch8 Timer C match, overflow, and underflow	***[IBIMC086]***	***[IMNFLG5]*** <INT182FLG>	✓	✓	✓
47	INTT32A08_B_C01_CPC	T32A ch8 Timer B match, overflow, and underflow	***[IBIMC083]***	***[IMNFLG5]*** <INT179FLG>	✓	✓	✓
		T32A ch8 Timer B capture 0	***[IBIMC084]***	***[IMNFLG5]*** <INT180FLG>	✓	✓	✓
		T32A ch8 Timer B capture 1	***[IBIMC085]***	***[IMNFLG5]*** <INT181FLG>	✓	✓	✓
		T32A ch8 Timer C capture 0	***[IBIMC087]***	***[IMNFLG5]*** <INT183FLG>	✓	✓	✓
		T32A ch8 Timer C capture 1	***[IBIMC088]***	***[IMNFLG5]*** <INT184FLG>	✓	✓	✓
		T32A ch8 Timer C pulse count	***[IBIMC089]***	***[IMNFLG5]*** <INT185FLG>	✓	✓	✓
48	INTT32A09_A_CT	T32A ch9 Timer A match, overflow, and underflow	***[IBIMC090]***	***[IMNFLG5]*** <INT186FLG>	✓	✓	✓
		T32A ch9 Timer A capture 0	***[IBIMC091]***	***[IMNFLG5]*** <INT187FLG>	✓	✓	✓
		T32A ch9 Timer A capture 1	***[IBIMC092]***	***[IMNFLG5]*** <INT188FLG>	✓	✓	✓
		T32A ch9 Timer C match, overflow, and underflow	***[IBIMC096]***	***[IMNFLG6]*** <INT192FLG>	✓	✓	✓
49	INTT32A09_B_C01_CPC	T32A ch9 Timer B match, overflow, and underflow	***[IBIMC093]***	***[IMNFLG5]*** <INT189FLG>	✓	✓	✓
		T32A ch9 Timer B capture 0	***[IBIMC094]***	***[IMNFLG5]*** <INT190FLG>	✓	✓	✓
		T32A ch9 Timer B capture 1	***[IBIMC095]***	***[IMNFLG5]*** <INT191FLG>	✓	✓	✓
		T32A ch9 Timer C capture 0	***[IBIMC097]***	***[IMNFLG6]*** <INT193FLG>	✓	✓	✓
		T32A ch9 Timer C capture 1	***[IBIMC098]***	***[IMNFLG6]*** <INT194FLG>	✓	✓	✓
		T32A ch9 Timer C pulse count	***[IBIMC099]***	***[IMNFLG6]*** <INT195FLG>	✓	✓	✓
50	INTT32A10_A_CT	T32A ch10 Timer A match, overflow, and underflow	***[IBIMC100]***	***[IMNFLG6]*** <INT196FLG>	✓	✓	✓
		T32A ch10 Timer A capture 0	***[IBIMC101]***	***[IMNFLG6]*** <INT197FLG>	✓	✓	✓
		T32A ch10 Timer A capture 1	***[IBIMC102]***	***[IMNFLG6]*** <INT198FLG>	✓	✓	✓
		T32A ch10 Timer C match, overflow, and underflow	***[IBIMC106]***	***[IMNFLG6]*** <INT202FLG>	✓	✓	✓

Note: ✓: Available, -: N/A

Table 6.7 List of Interrupt Factors (7/12)

Interrupt No.	Interrupt Source	Interrupt Request	Interrupt Control Register	Interrupt Monitor Register	M4GR	M4GQ	M4GN
51	INTT32A10_B_C01_CPC	T32A ch10 Timer B match, overflow, and underflow	***[IBIMC103]***	***[IMNFLG6]*** <INT199FLG>	✓	✓	✓
		T32A ch10 Timer B capture 0	***[IBIMC104]***	***[IMNFLG6]*** <INT200FLG>	✓	✓	✓
		T32A ch10 Timer B capture 1	***[IBIMC105]***	***[IMNFLG6]*** <INT201FLG>	✓	✓	✓
		T32A ch10 Timer C capture 0	***[IBIMC107]***	***[IMNFLG6]*** <INT203FLG>	✓	✓	✓
		T32A ch10 Timer C capture 1	***[IBIMC108]***	***[IMNFLG6]*** <INT204FLG>	✓	✓	✓
		T32A ch10 Timer C pulse count	***[IBIMC109]***	***[IMNFLG6]*** <INT205FLG>	✓	✓	✓
52	INTT32A11_A_CT	T32A ch11 Timer A match, overflow, and underflow	***[IBIMC110]***	***[IMNFLG6]*** <INT206FLG>	✓	✓	✓
		T32A ch11 Timer A capture 0	***[IBIMC111]***	***[IMNFLG6]*** <INT207FLG>	✓	✓	✓
		T32A ch11 Timer A capture 1	***[IBIMC112]***	***[IMNFLG6]*** <INT208FLG>	✓	✓	✓
		T32A ch11 Timer C match, overflow, and underflow	***[IBIMC116]***	***[IMNFLG6]*** <INT212FLG>	✓	✓	✓
53	INTT32A11_B_C01_CPC	T32A ch11 Timer B match, overflow, and underflow	***[IBIMC113]***	***[IMNFLG6]*** <INT209FLG>	✓	✓	✓
		T32A ch11 Timer B capture 0	***[IBIMC114]***	***[IMNFLG6]*** <INT210FLG>	✓	✓	✓
		T32A ch11 Timer B capture 1	***[IBIMC115]***	***[IMNFLG6]*** <INT211FLG>	✓	✓	✓
		T32A ch11 Timer C capture 0	***[IBIMC117]***	***[IMNFLG6]*** <INT213FLG>	✓	✓	✓
		T32A ch11 Timer C capture 1	***[IBIMC118]***	***[IMNFLG6]*** <INT214FLG>	✓	✓	✓
		T32A ch11 Timer C pulse count	***[IBIMC119]***	***[IMNFLG6]*** <INT215FLG>	✓	✓	✓
54	INTT32A12_A_CT	T32A ch12 Timer A match, overflow, and underflow	***[IBIMC120]***	***[IMNFLG6]*** <INT216FLG>	✓	✓	✓
		T32A ch12 Timer A capture 0	***[IBIMC121]***	***[IMNFLG6]*** <INT217FLG>	✓	✓	✓
		T32A ch12 Timer A capture 1	***[IBIMC122]***	***[IMNFLG6]*** <INT218FLG>	✓	✓	✓
		T32A ch12 Timer C match, overflow, and underflow	***[IBIMC126]***	***[IMNFLG6]*** <INT222FLG>	✓	✓	✓
55	INTT32A12_B_C01_CPC	T32A ch12 Timer B match, overflow, and underflow	***[IBIMC123]***	***[IMNFLG6]*** <INT219FLG>	✓	✓	✓
		T32A ch12 Timer B capture 0	***[IBIMC124]***	***[IMNFLG6]*** <INT220FLG>	✓	✓	✓
		T32A ch12 Timer B capture 1	***[IBIMC125]***	***[IMNFLG6]*** <INT221FLG>	✓	✓	✓
		T32A ch12 Timer C capture 0	***[IBIMC127]***	***[IMNFLG6]*** <INT223FLG>	✓	✓	✓
		T32A ch12 Timer C capture 1	***[IBIMC128]***	***[IMNFLG7]*** <INT224FLG>	✓	✓	✓
		T32A ch12 Timer C pulse count	***[IBIMC129]***	***[IMNFLG7]*** <INT225FLG>	✓	✓	✓

Note: ✓: Available, -: N/A

Table 6.8 List of Interrupt Factors (8/12)

Interrupt No.	Interrupt Source	Interrupt Request	Interrupt Control Register	Interrupt Monitor Register	M4GR	M4GQ	M4GN
56	INTT32A13_A_CT	T32A ch13 Timer A match, overflow, and underflow	***[IBIMC130]***	***[IMNFLG7]*** <INT226FLG>	✓	✓	✓
		T32A ch13 Timer A capture 0	***[IBIMC131]***	***[IMNFLG7]*** <INT227FLG>	✓	✓	✓
		T32A ch13 Timer A capture 1	***[IBIMC132]***	***[IMNFLG7]*** <INT228FLG>	✓	✓	✓
		T32A ch13 Timer C match, overflow, and underflow	***[IBIMC136]***	***[IMNFLG7]*** <INT232FLG>	✓	✓	✓
57	INTT32A13_B_C01_CPC	T32A ch13 Timer B match, overflow, and underflow	***[IBIMC133]***	***[IMNFLG7]*** <INT229FLG>	✓	✓	✓
		T32A ch13 Timer B capture 0	***[IBIMC134]***	***[IMNFLG7]*** <INT230FLG>	✓	✓	✓
		T32A ch13 Timer B capture 1	***[IBIMC135]***	***[IMNFLG7]*** <INT231FLG>	✓	✓	✓
		T32A ch13 Timer C capture 0	***[IBIMC137]***	***[IMNFLG7]*** <INT233FLG>	✓	✓	✓
		T32A ch13 Timer C capture 1	***[IBIMC138]***	***[IMNFLG7]*** <INT234FLG>	✓	✓	✓
		T32A ch13 Timer C pulse count	***[IBIMC139]***	***[IMNFLG7]*** <INT235FLG>	✓	✓	✓
58	INTEMG0	A-PMD ch0 EMG interrupt			✓	✓	✓
59	INTOVV0	A-PMD ch0 OVV interrupt			✓	✓	✓
60	INTPWM0	A-PMD ch0 PWM interrupt			✓	✓	✓
61	INTT0RX	TSPI ch0 reception interrupt			✓	✓	✓
62	INTT0TX	TSPI ch0 transmission interrupt			✓	✓	✓
63	INTT0ERR	TSPI ch0 error interrupt			✓	✓	✓
64	INTT1RX	TSPI ch1 reception interrupt			✓	✓	✓
65	INTT1TX	TSPI ch1 transmission interrupt			✓	✓	✓
66	INTT1ERR	TSPI ch1 error interrupt			✓	✓	✓
67	INTT2RX	TSPI ch2 reception interrupt			✓	✓	✓
68	INTT2TX	TSPI ch2 transmission interrupt			✓	✓	✓
69	INTT2ERR	TSPI ch2 error interrupt			✓	✓	✓
70	INTT3RX	TSPI ch3 reception interrupt			✓	✓	✓
71	INTT3TX	TSPI ch3 transmission interrupt			✓	✓	✓
72	INTT3ERR	TSPI ch3 error interrupt			✓	✓	✓
73	INTT4RX	TSPI ch4 reception interrupt			✓	✓	✓
74	INTT4TX	TSPI ch4 transmission interrupt			✓	✓	✓
75	INTT4ERR	TSPI ch4 error interrupt			✓	✓	✓
76	INTT5RX	TSPI ch5 reception interrupt			✓	✓	-
77	INTT5TX	TSPI ch5 transmission interrupt			✓	✓	-
78	INTT5ERR	TSPI ch5 error interrupt			✓	✓	-
79	INTT6RX	TSPI ch6 reception interrupt			✓	✓	-
80	INTT6TX	TSPI ch6 transmission interrupt			✓	✓	-
81	INTT6ERR	TSPI ch6 error interrupt			✓	✓	-

Note: ✓: Available, -: N/A

Table 6.9 List of Interrupt Factors (9/12)

Interrupt No.	Interrupt Source	Interrupt Request	Interrupt Control Register	Interrupt Monitor Register	M4GR	M4GQ	M4GN
82	INTT7RX	TSPI ch7 reception interrupt			✓	✓	-
83	INTT7TX	TSPI ch7 transmission interrupt			✓	✓	-
84	INTT7ERR	TSPI ch7 error interrupt			✓	✓	-
85	INTT8RX	TSPI ch8 reception interrupt			✓	-	-
86	INTT8TX	TSPI ch8 transmission interrupt			✓	-	-
87	INTT8ERR	TSPI ch8 error interrupt			✓	-	-
88	INTSMI0	SMI ch0 interrupt			✓	✓	✓
89	INTUART0RX	UART ch0 reception interrupt			✓	✓	✓
90	INTUART0TX	UART ch0 transmission interrupt			✓	✓	✓
91	INTUART0ERR	UART ch0 error interrupt			✓	✓	✓
92	INTUART1RX	UART ch1 reception interrupt			✓	✓	✓
93	INTUART1TX	UART ch1 transmission interrupt			✓	✓	✓
94	INTUART1ERR	UART ch1 error interrupt			✓	✓	✓
95	INTUART2RX	UART ch2 reception interrupt			✓	✓	✓
96	INTUART2TX	UART ch2 transmission interrupt			✓	✓	✓
97	INTUART2ERR	UART ch2 error interrupt			✓	✓	✓
98	INTUART3RX	UART ch3 reception interrupt			✓	✓	-
99	INTUART3TX	UART ch3 transmission interrupt			✓	✓	-
100	INTUART3ERR	UART ch3 error interrupt			✓	✓	-
101	INTUART4RX	UART ch4 reception interrupt			✓	✓	-
102	INTUART4TX	UART ch4 transmission interrupt			✓	✓	-
103	INTUART4ERR	UART ch4 error interrupt			✓	✓	-
104	INTUART5RX	UART ch5 reception interrupt			✓	-	-
105	INTUART5TX	UART ch5 transmission interrupt			✓	-	-
106	INTUART5ERR	UART ch5 error interrupt			✓	-	-
107	INTFUART0	FUART ch0 Transmission/Reception error interrupt			✓	✓	✓
108	INTFUART1	FUART ch1 Transmission/Reception error interrupt			✓	✓	-
109	INTI2C0NST (Note)	I2C ch0 interrupt / EI2C ch0 status interrupt			✓	✓	✓
110	INTI2C0ATX (Note)	I2C ch0 arbitration lost detection interrupt / EI2C ch0 transmit buffer empty interrupt			✓	✓	✓
111	INTI2C0BRX (Note)	I2C ch0 bus free detection interrupt / EI2C ch0 receive buffer empty interrupt			✓	✓	✓
112	INTI2C0NA	I2C ch0 NACK detection interrupt			✓	✓	✓
113	INTI2C1NST (Note)	I2C ch1 interrupt / EI2C ch1 status interrupt			✓	✓	✓
114	INTI2C1ATX (Note)	I2C ch1 arbitration lost detection interrupt / EI2C ch1 transmit buffer empty interrupt			✓	✓	✓
115	INTI2C1BRX (Note)	I2C ch1 bus free detection interrupt / EI2C ch1 receive buffer empty interrupt			✓	✓	✓
116	INTI2C1NA	I2C ch1 NACK detection interrupt			✓	✓	✓

✓: Available, -: N/A

Note: Please refer to "4.4.1. Joint interruption".

Table 6.10 List of Interrupt Factors (10/12)

Interrupt No.	Interrupt Source	Interrupt Request	Interrupt Control Register	Interrupt Monitor Register	M4GR	M4GQ	M4GN
117	INTI2C2NST (Note)	I2C ch2 interrupt / EI2C ch2 status interrupt			✓	✓	✓
118	INTI2C2ATX (Note)	I2C ch2 arbitration lost detection interrupt / EI2C ch2 transmit buffer empty interrupt			✓	✓	✓
119	INTI2C2BRX (Note)	I2C ch2 bus free detection interrupt / EI2C ch2 receive buffer empty interrupt			✓	✓	✓
120	INTI2C2NA	I2C ch2 NACK detection interrupt			✓	✓	✓
121	INTI2C3NST (Note)	I2C ch3 interrupt / EI2C ch3 status interrupt			✓	✓	-
122	INTI2C3ATX (Note)	I2C ch3 arbitration lost detection interrupt / EI2C ch3 transmit buffer empty interrupt			✓	✓	-
123	INTI2C3BRX (Note)	I2C ch3 bus free detection interrupt / EI2C ch3 receive buffer empty interrupt			✓	✓	-
124	INTI2C3NA	I2C ch3 NACK detection interrupt			✓	✓	-
125	INTI2C4NST (Note)	I2C ch4 interrupt / EI2C ch4 status interrupt			✓	✓	-
126	INTI2C4ATX (Note)	I2C ch4 arbitration lost detection interrupt / EI2C ch4 transmit buffer empty interrupt			✓	✓	-
127	INTI2C4BRX (Note)	I2C ch4 bus free detection interrupt / EI2C ch4 receive buffer empty interrupt			✓	✓	-
128	INTI2C4NA	I2C ch4 NACK detection interrupt			✓	✓	-
129	INTADACP0	ADC unit A monitor function interrupt 0			✓	✓	✓
130	INTADACP1	ADC unit A monitor function interrupt 1			✓	✓	✓
131	INTADATRG	ADC unit A general purpose trigger interrupt			✓	✓	✓
132	INTADASGL	ADC unit A single conversion interrupt			✓	✓	✓
133	INTADACNT	ADC unit A Continuous conversion interrupt			✓	✓	✓
134	INTADAHP	ADC unit A highest priority conversion completion interrupt			✓	✓	✓
135	INTFLDRDY	Data FLASH Ready interrupt			✓	✓	✓
136	INTFLCRDY	Code FLASH Ready interrupt			✓	✓	✓
137	Reserved.						
138	Reserved.						
139	INTMDMAABERR	MDMAC unit A bus error interrupt	***[IBIMC140]***	***[IMNFLG7]*** <INT236FLG>	✓	✓	✓
140	INTMDMAADERR	MDMAC unit A descriptor error interrupt	***[IBIMC141]***	***[IMNFLG7]*** <INT237FLG>	✓	✓	✓

✓: Available, -: N/A

Note: Please refer to "4.4.1. Joint interruption".

Table 6.11 List of Interrupt Factors (11/12)

Interrupt No.	Interrupt Source	Interrupt Request	Interrupt Control Register	Interrupt Monitor Register	M4GR	M4GQ	M4GN
141	INTI2S0SI	I2S ch0 reception data transfer request interrupt			✓	✓	✓
142	INTI2S0SIERR	I2S ch0 reception error interrupt			✓	✓	✓
143	INTI2S0SO	I2S ch0 transmission data transfer request interrupt			✓	✓	✓
144	INTI2S0SOERR	I2S ch0 transmission error interrupt			✓	✓	✓
145	INTI2S1SI	I2S ch1 reception data transfer request interrupt			✓	✓	✓
146	INTI2S1SIERR	I2S ch1 reception error interrupt			✓	✓	✓
147	INTI2S1SO	I2S ch1 transmission data transfer request interrupt			✓	✓	✓
148	INTI2S1SOERR	I2S ch1 transmission error interrupt			✓	✓	✓
149	INTFIR	FIR interrupt			✓	✓	✓
150	INTTSSI0RX	TSSI ch0 receive interrupt			✓	✓	✓
151	INTTSSI0TX	TSSI ch0 transmission interrupt			✓	✓	✓
152	INTTSSI0ERR	TSSI ch0 error interrupt			✓	✓	✓
153	INTTSSI1RX	TSSI ch1 receive interrupt			✓	-	-
154	INTTSSI1TX	TSSI ch1 transmission interrupt			✓	-	-
155	INTTSSI1ERR	TSSI ch1 error interrupt			✓	-	-
156	Reserved						
157	Reserved						
158	Reserved						
159	Reserved						
160	Reserved						
161	Reserved						
162	Reserved						
163	Reserved						
164	Reserved						
165	Reserved						
166	Reserved						
167	Reserved						
168	INTT32A14_A	T32A ch14 Timer A match, overflow, and underflow	***[IBIMC145]***	***[IMNFLG7]*** <INT241FLG>	✓	✓	✓
		T32A ch14 Timer A capture 0	***[IBIMC146]***	***[IMNFLG7]*** <INT242FLG>	✓	✓	✓
		T32A ch14 Timer A capture 1	***[IBIMC147]***	***[IMNFLG7]*** <INT243FLG>	✓	✓	✓
169	INTT32A14_B	T32A ch14 Timer B match, overflow, and underflow	***[IBIMC148]***	***[IMNFLG7]*** <INT244FLG>	✓	✓	✓
		T32A ch14 Timer B capture 0	***[IBIMC149]***	***[IMNFLG7]*** <INT245FLG>	✓	✓	✓
		T32A ch14 Timer B capture 1	***[IBIMC150]***	***[IMNFLG7]*** <INT246FLG>	✓	✓	✓
170	INTT32A14_CT	T32A ch14 Timer C match, overflow, and underflow			✓	✓	✓

✓: Available, -: N/A

Table 6.12 List of Interrupt Factors (12/12)

Interrupt No.	Interrupt Source	Interrupt Request	Interrupt Control Register	Interrupt Monitor Register	M4GR	M4GQ	M4GN
171	INTT32A15_A	T32A ch15 Timer A match, overflow, and underflow	***[IBIMC151]***	***[IMNFLG7]*** <INT247FLG>	✓	✓	✓
		T32A ch15 Timer A capture 0	***[IBIMC152]***	***[IMNFLG7]*** <INT248FLG>	✓	✓	✓
		T32A ch15 Timer A capture 1	***[IBIMC153]***	***[IMNFLG7]*** <INT249FLG>	✓	✓	✓
172	INTT32A15_B	T32A ch15 Timer B match, overflow, and underflow	***[IBIMC154]***	***[IMNFLG7]*** <INT250FLG>	✓	✓	✓
		T32A ch15 Timer B capture 0	***[IBIMC155]***	***[IMNFLG7]*** <INT251FLG>	✓	✓	✓
		T32A ch15 Timer B capture 1	***[IBIMC156]***	***[IMNFLG7]*** <INT252FLG>	✓	✓	✓
173	INTT32A15_C	T32A ch15 Timer C match, overflow, and underflow	***[IBIMC157]***	***[IMNFLG7]*** <INT253FLG>	✓	✓	✓
		T32A ch15 Timer C capture 0	***[IBIMC158]***	***[IMNFLG7]*** <INT254FLG>	✓	✓	✓
		T32A ch15 Timer C capture 1	***[IBIMC159]***	***[IMNFLG7]*** <INT255FLG>	✓	✓	✓
174	INTMDMAADS	MDMAC unit A descriptor completion interrupt			✓	✓	✓

✓: Available, -: N/A

7. Revision History

Table 7.1 Revision History

Revision	Date	Description
1.0	2020-11-02	First release

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