32-bit RISC Microcontroller

TXZ+ Family

Reference Manual
I²S Interface
(I2S-A)

Revision 1.0

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TOSHIBA ELECTRONIC DEVICES & STORAGE CORPORATION

Table of Contents

List of Figures

List of Tables

Preface

Rerated Documents

Document name
Product Information
Exception
Clock Control and Operation Mode
Input/Output Ports
Multi-Function DMA Controller
FIR calculation Circuit

Conventions in this document

- The numerical values are expressed as follows.
  Hexadecimal number: 0xABC
  Decimal number: 123 or 0d123 (only when it needs to be explicitly shown that they are decimal numbers)
  Binary number: 0b111 (It is possible to omit the "0b" when the number of bit can be distinctly understood from a sentence.)
- "_N" is added to the end of signal names to indicate low active signals.
- It is called "assert" that a signal moves to its active level, "deassert" to its inactive level.
- When two or more signal names are referred, they are described like as [3:0].
  [3:0] shows four signal names 3, 2, 1, and 0 together.
- The characters surrounded by [] defines the register.
  Example: ***[ABCD]***
- "n" substitutes suffix number of two or more same kind of registers, fields, and bit names.
  Example: ***[XYZ1], [XYZ2], [XYZ3] to [XYZn]***
- The bit range of a register is written like as [3:0].
  Example: Bit[3:0] expresses the range of bits 3 to 0.
- The configuration value of a register is expressed by either the hexadecimal number or the binary number.
  Example: [ABCD].EFG = 0x01 (hexadecimal), ***[XYZn]***.VW = 1 (binary)
- Word and Byte represent the following bit length.
  Byte: 8-bit
  Half word: 16-bit
  Word: 32-bit
  Double word: 64-bit
- Unless otherwise specified, register access supports only word access.
- The register defined as reserved must not be rewritten. Moreover, don't use the read value.
- Properties of each bit in a register are expressed as follows.
  R: Read only
  W: Write only
  W1C: Write 1 Clear (The corresponding bit is cleared (=0) when "1" is written to this bit.)
  W1S: Write 1 Set (The corresponding bit is set (=1) when "1" is written to this bit.)
  R/W: Read and Write are possible.
  R/W0C: Read/Write 0 Clear
  R/W1C: Read/Write 1 Clear
  R/W1S: Read/Write 1 Set
  RS/WC: Read Set/Write Clear (Set after read operation, cleared after write operation)
- The value read from the bit having default value of "—" is unknown.
- When a register containing both of writable bits and read-only bits is written, read-only bits should be written with their default value. In the cases that default is "—", follow the definition of each register.
- Reserved bits of the Write-only register should be written with their default value. In the cases that default is "—", follow the definition of each register.

All other company names, product names, and service names mentioned herein may be trademarks of their respective companies.

Terms and Abbreviations

It is part of the terms and abbreviations used in this specification.

DMA	Direct Memory Access
DMAC	Direct Memory Access Controller
FIFO	First-In First-Out
FIR	Finite Impulse Response
I2S	Inter-IC Sound
PCM	Pulse Code Modulation

1. Outlines

Each channel of the I2S module can operate as either a transmitter or a receiver of audio data. The list of the functions is shown in the following table.

Function category	Function	Operation
Master clock	ΦT0 division	ΦT0 division clock output: 1/2, 1/3 to 1/254, and 1/255 are selectable.
	Master clock selection	Selection of the source of the master clock (the internal clock of the ΦT0 division clock output or the input clock from the external pin MCKIO).
	Master clock output	The master clock can be output from the MCKIO pin in the master device mode.
Communication speed control	Bit clock (BCK)	The BCK is generated by the output of 1/1, 1/2 to 1/254, or 1/255 division of the master clock. The LRCK and the SDATA (DO/DI) are synchronous with the BCK.
	LR clock (LRCK)	The LRCK is generated by counting the BCK.
	Master/Slave	Master or Slave is selectable.
Communication format	Audio data format	I2S stereo, LR stereo, or PCM monaural is selectable.
	BCK frequency	Stereo: 32fs or 64fs Monaural: 16fs or 32fs
	Sampling frequency (fs)	Stereo: 192 kHz at maximum Monaural: 384 kHz at maximum
	Frame size	16 cycles or 32 cycles
	Data length	One of 8, 16, 24, and 32 bits is selectable per audio data (each one of L channel and R channel for the stereo mode).
	Right justification/Left justification	Left justification
	Data transfer direction	MSB first
	Clock edge	Synchronization timing is selectable between the LRCK/SDATA and the BCK (the rising edge or the falling edge).
Transmission control/ Reception control	FIFO	Transmit FIFO: 256 bytes Receive FIFO: 256 bytes
	Data storage format	The data storage format is selectable (Refer to Table 3.6).
	Mute function	ON/OFF switching of the mute function
Interlocking control	Interrupt	Transmission: Transmission data transfer request interrupt and Transmission error interrupt Factor of Data transfer request interrupt: Data transfer request Factor of Error interrupt: LRCK error and Underrun error
		Reception: Reception data transfer request interrupt and Reception error interrupt Factor of Data transfer request interrupt: Data transfer request Factor of Error interrupt: LRCK error and Overrun error
	DMA request	Setting is enabled for the transmission and the reception, respectively.
	FIR linkage	For the details, refer to “Product Information” in the Reference manual.

2. Configuration

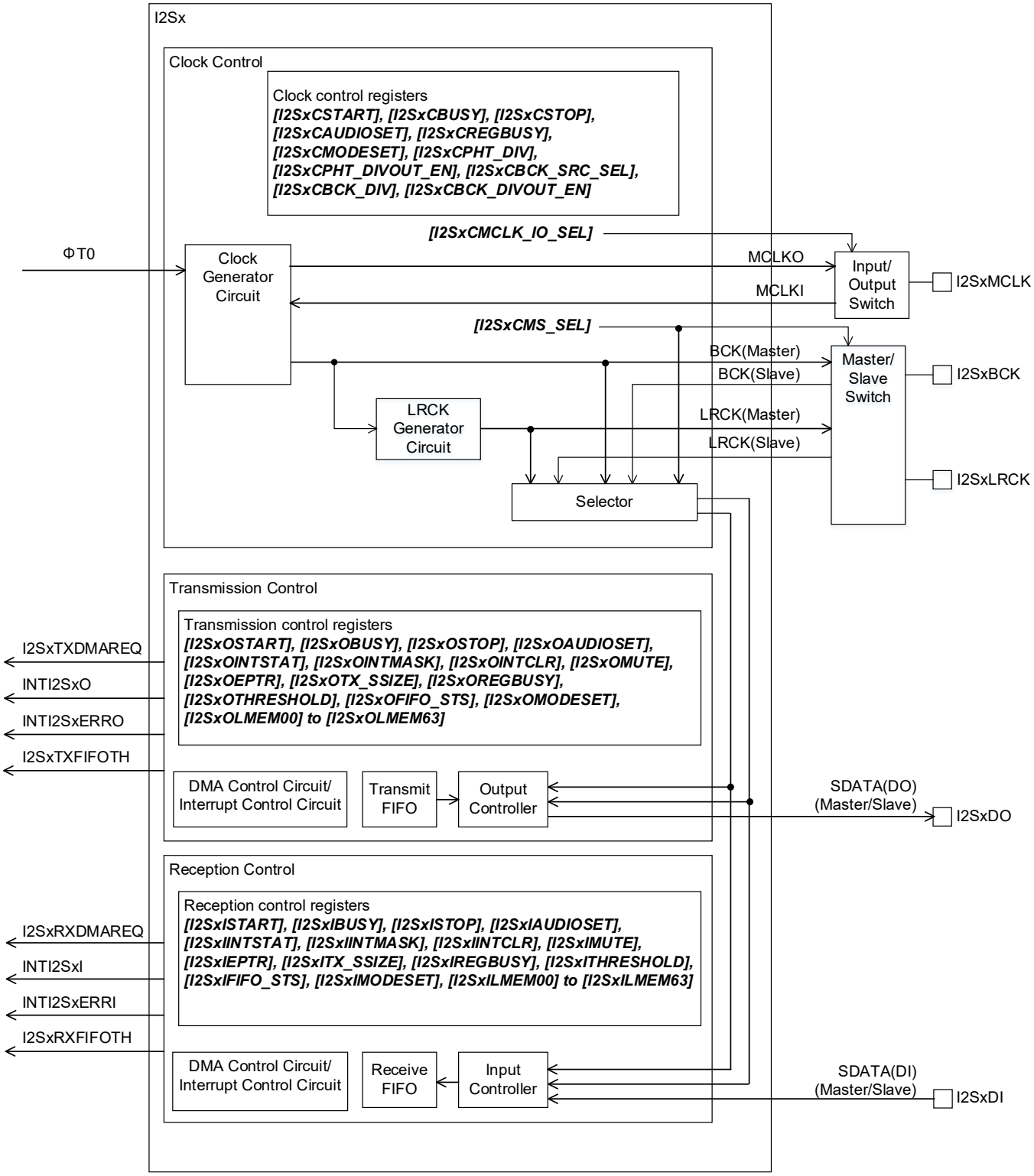


Figure 2.1 Configuration chart of I2Sx interface

Table 2.1 List of signals

No.	Signal symbol	Signal name	I/O	Reference manual
1	ΦT0	System clock	Input	"Clock Control and Operation Mode"
2	I2SxBCK	Bit clock	Input/Output	"Product Information", "Input/Output Ports"
3	I2SxLRCK	LR clock (LRCK)	Input/Output	"Product Information", "Input/Output Ports"
4	I2SxDI	Audio input serial data	Input	"Product Information", "Input/Output Ports"
5	I2SxDO	Audio output serial data	Output	"Product Information", "Input/Output Ports"
6	I2SxMCLK	External master clock	Input/Output	"Product Information", "Input/Output Ports"
7	INTI2SxSO	Transmission data transfer request interrupt	Output	"Exception"
8	INTI2SxSOERR	Transmission error interrupt	Output	"Exception"
9	INTI2SxSI	Reception data transfer request interrupt	Output	"Exception"
10	INTI2SxSIERR	Reception error interrupt	Output	"Exception"
11	I2SxTXDMAREQ	Transmission DMA request	Output	"Product Information"
12	I2SxRXDMAREQ	Reception DMA request	Output	"Product Information"
13	I2SxTXFIFOTH	Transmit FIFO threshold value signal	Output	"Product Information"
14	I2SxRXFIFOTH	Receive FIFO threshold value signal	Output	"Product Information"

3. Function and Operation

3.1. Clock Supply

When the I2Sx is used, the corresponding clock enable bits should be set to "1" (Clock supply) in fsys supply stop register A (***[CGFSYSENA]*** and ***[CGFSYSMENA]***), fsys supply stop register B (***[CGFSYSENB]*** and ***[CGFSYSMENB]***), fsys supply stop register C (***[CGFSYSMENC]***), and fc supply stop register (***[CGFCEN]***).
The corresponding registers and the bit locations depend on a product. Some products do not have all registers. For the details, refer to "Clock Control and Operation Mode" in the Reference manual.

3.2. Audio Signal

The interface of each I2S channel consists of the BCK, the LRCK, and the SDATA (DI/DO).
The sampling frequency (fs) is determined by the frequency of the LRCK. And the bit count (Frame size) of the data which can be stored in one audio data is determined by the frequency of the BCK.

The frequency of the BCK is an integral multiple of the frequency of the LRCK. When the integer is 32, the frequency of the BCK is represented as 32fs, and when, 64, it is done as 64fs.

3.3. Master/Slave

When ***[I2SxCMS_SEL]***<SEL> is cleared to "0", the I2Sx operates as a master device.
When ***[I2SxCMS_SEL]***<SEL> is set to "1" (Default value), the I2Sx operates as a slave device.

When ***[I2SxCMS_SEL]***<SEL> is "1", the transmission control circuit and the reception control circuit transfer audio serial data using the synchronization clock (BCK/LRCK) which is supplied by an external source.
When the audio serial transfer is done using an internally generated clock, ***[I2SxCMS_SEL]***<SEL> is cleared to "0".
The setting value of ***[I2SxCMS_SEL]***<SEL> is used as the output enable signal of the I2SxBCK/ I2SxLRCK pin.

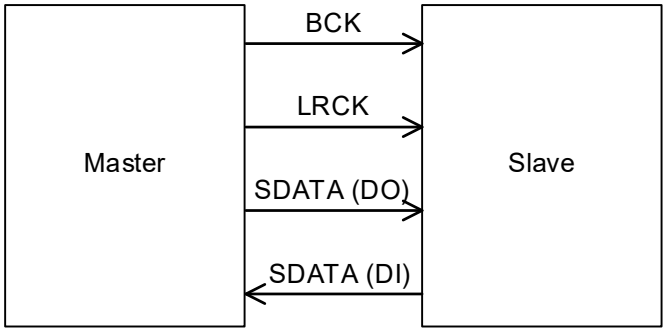
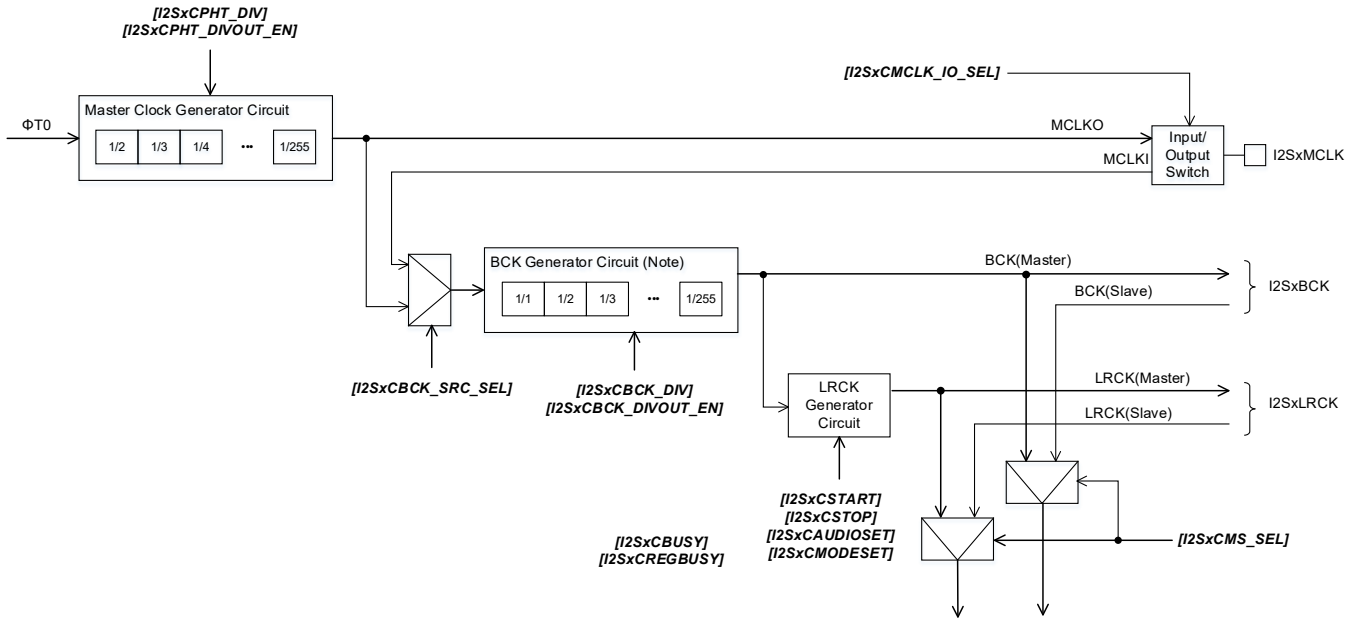


Figure 3.1 Example of connection between Master and Slave

The BCK and the LRCK are supplied by the master device.
The SDATA (DI/DO) has two directions; data is transmitted by the Master and received by the Slave, and transmitted by the Slave and received by the Master.

3.4. Clock Generation



Note: When the clock selected by ***[I2SxCBCK_SRC_SEL]***<SEL> is the MCLKI (External clock), the BCK generator is selectable 1/2 to 1/255 division ratio. When the clock is the MCLKO (Internal clock), set the BCK generator to 1/1 division ratio.

Figure 3.2 I2Sx clock control

3.4.1. Master Clock

The master clock generator generates the internal master clock (MCLKO) by dividing the ΦT0 clock into 1/2 to 1/255.
The division ratio of the ΦT0 is set in ***[I2SxCPHT_DIV]***<PSCAL[7:0]>, and the output of the master clock generator is enabled by setting "1" to ***[I2SxCPHT_DIVOUT_EN]***<EN>.
When ***[I2SxCPHT_DIVOUT_EN]***<EN> is "1", do not change a setting value of ***[I2SxCPHT_DIV]***<PSCAL[7:0]>.
If the division ratio in the master clock generator is odd, the duty of the generated clock is not 50 %. When the duty of 50 % is required, the division ratio should be set to an even value.

3.4.2. Bit Clock (BCK)

When the I2Sx operates as a master device (***[I2SxCMS_SEL]***<SEL> = 0), the bit clock generator generates the BCK by dividing the master clock.
The master clock is selected between the MCLKO (Internal clock) and the MCLKI (External clock).
The selection of the master clock is done by ***[I2SxCBCK_SRC_SEL]***<SEL>, and the division ratio is set in ***[I2SxCBCK_DIV]***<PSCAL[7:0]>.
When ***[I2SxCBCK_SRC_SEL]***<SEL> is "0" (External clock), ***[I2SxCBCK_DIV]***<PSCAL[7:0]> is set to "0x01" to "0xFE" (1/2 to 1/255 division).When ***[I2SxCBCK_SRC_SEL]***<SEL> is "1" (Internal clock), ***[I2SxCBCK_DIV]***<PSCAL[7:0]> is set to "0x00" (1/1 division).

The output of the bit clock generator is enabled by setting "1" to ***[I2SxCBCK_DIVOUT_EN]***<EN>.
When ***[I2SxCBCK_DIVOUT_EN]***<EN> is "1", do not change ***[I2SxCBCK_SRC_SEL]***<SEL> and ***[I2SxCBCK_DIV]***<PSCAL[7:0]>.

If the division ratio in the BCK generator is odd, the duty of the generated clock is not 50 %. When the duty of 50 % is required, the division ratio should be set to an even value. The setting example of the BCK is refer to "Table 3.1".

Table 3.1 Setting example for BCK (Duty 50%) in Master device (*[I2SxCMS_SEL]*<SEL> = 0)

[I2SxCMCLK_IO_SEL] <SEL>	*[I2SxCBCK_SRC_SEL]* <SEL>	*[I2SxCPHT_DIV]* <PSCAL[7:0]>	*[I2SxCBCK_DIV]* <PSCAL[7:0]>	MCLKI frequency (MHz)	ΦT0 frequency (MHz)	BCK frequency (MHz)
0	0	-	0x01 (1/2 division)	1.536	-	0.768
0	0	-	0x03 (1/4 division)	3.072	-	0.768
0	0	-	0x01 (1/2 division)	3.072	-	1.536
0	0	-	0x03 (1/4 division)	6.144	-	1.536
0	0	-	0x01 (1/2 division)	6.144	-	3.072
0	0	-	0x03 (1/4 division)	12.288	-	3.072
0	0	-	0x01 (1/2 division)	12.288	-	6.144
0	0	-	0x03 (1/4 division)	24.576	-	6.144
0	0	-	0x01 (1/2 division)	24.576	-	12.288
0	0	-	0x03 (1/4 division)	49.152	-	12.288
-	1	0x03 (1/4 division)	0x00 (1/1 division)	-	3.072	0.768
-	1	0x07 (1/8 division)	0x00 (1/1 division)	-	6.144	0.768
-	1	0x03 (1/4 division)	0x00 (1/1 division)	-	6.144	1.536
-	1	0x0F (1/16 division)	0x00 (1/1 division)	-	24.576	1.536
-	1	0x07 (1/8 division)	0x00 (1/1 division)	-	24.576	3.072
-	1	0x0F (1/16 division)	0x00 (1/1 division)	-	49.152	3.072
-	1	0x03 (1/4 division)	0x00 (1/1 division)	-	24.576	6.144
-	1	0x07 (1/8 division)	0x00 (1/1 division)	-	49.152	6.144
-	1	0x03 (1/4 division)	0x00 (1/1 division)	-	49.152	12.288
-	1	0x0F (1/16 division)	0x00 (1/1 division)	-	196.608	12.288

3.4.3. LR Clock (LRCK)

When the I2Sx operates as a master device (***[I2SxCMS_SEL]***<SEL> = 0), the LRCK generator generates the LRCK.
The cycle count per channel of the sampling data is set by the BCK and the ***[I2SxCAUDIOSET]***<SCLKtoWS> value which are supplied to the LRCK generator.
The LRCK is generated by the setting "1" to ***[I2SxCSTART]***<Start> after ***[I2SxCAUDIOSET]*** <SCLKtoWS>, <WordLen[5:0]>, and ***[I2SxCMODESET]*** <WS[2:0]> have been set.
The output timing of the LRCK is set to ***[I2SxCAUDIOSET]***<Edge>.

The Low level of the LRCK corresponds to the L channel, and the High level, the R channel. The sampling frequency (fs) is determined by the LRCK frequency. The SDATA (DO/DI) is output or input synchronously with the BCK/LRCK.

3.5. Audio Data Format

The I2Sx supports the following audio data formats.
When the data length is not enough using the BCK frequency, it supports "left justification" in which the valid data is output first and "0" dummy data follows, and "MSB-first" which outputs the data from MSB. If "right justification" and "LSB-first" are necessary, software should perform them.

- I2S stereo
- LR stereo
- PCM monaural

The I2S stereo format assigns each phase of the LRCK to the L channel and the R channel, respectively. An offset of one bit clock cycle is inserted at the beginning of the data.

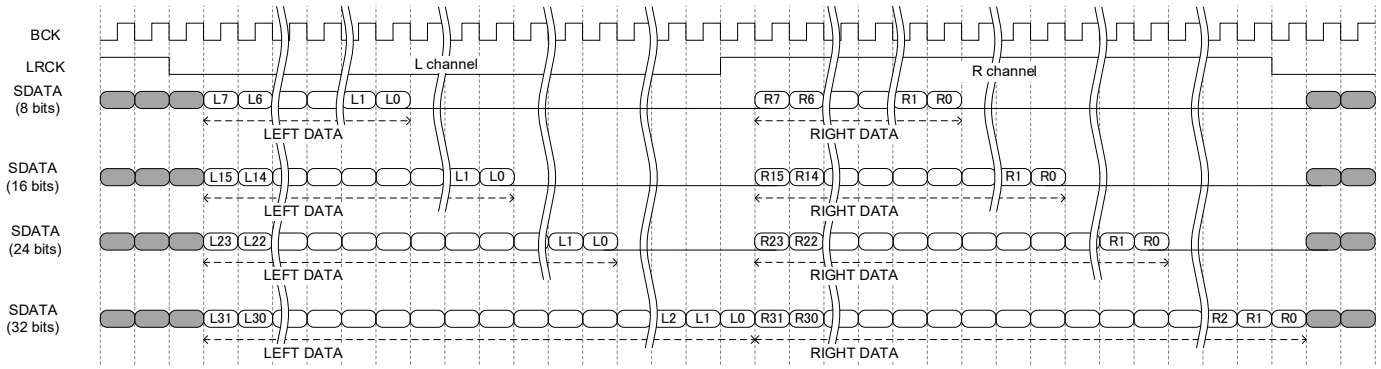


Figure 3.3 Example of I2S stereo format (Stereo 64fs)

The LR stereo format assigns each phase of the LRCK to the L channel and the R channel, respectively. It does not have any offsets as the "Figure 3.3".

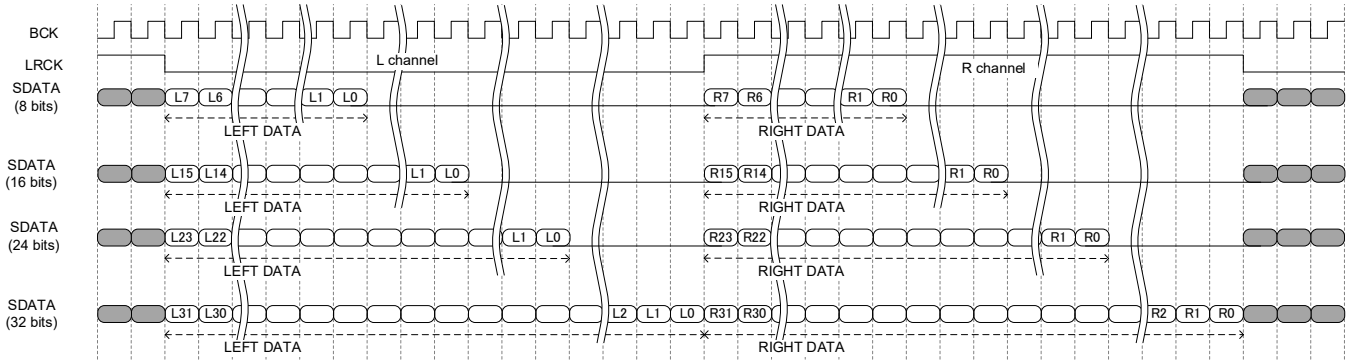


Figure 3.4 Example of LR stereo format (Stereo 64fs)

The PCM monaural format uses the LRCK as an enable signal to start the data. It does not distinguish the L channel and the R channel.

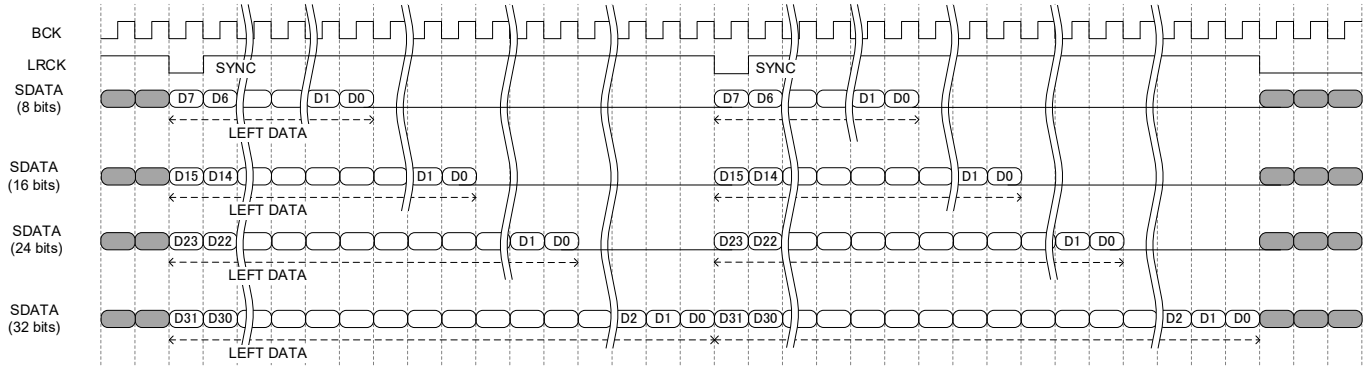


Figure 3.5 Example of PCM monaural format (Monaural 32fs)

3.5.1. Selection of Audio Data Format

The audio data format is set in ***[I2SxCMODESET]***<WS[2:0]>, ***[I2SxIMODESET]***<WS[2:0]>, and ***[I2SxOMODESET]***<WS[2:0]>.

The frequency of the BCK is an integral multiple of the frequency of the LRCK. When the BCK frequency is 32 times the LRCK frequency, the frequency of BCK is written as 32fs, and when, 64 times is written as 64fs.
For the I2S stereo format and the LR stereo format, the BCK frequency can be selected between 32fs and 64fs. For the PCM monaural format, the BCK frequency can be selected between 16fs and 32fs. The setting of the sampling frequency (fs) is shown in Table 3.5.

Table 3.2 Register setting of Audio format

Audio format	BCK frequency	***[I2SxCMODESET]*<WS[2:0]>** ***[I2SxIMODESET]*<WS[2:0]>** ***[I2SxOMODESET]*<WS[2:0]>**
I2S stereo	32fs/64fs	000
LR stereo (Low level of LRCK is for L channel.)		010
LR stereo (High level of LRCK is for L channel.)		011
PCM monaural (Synchronized with Low of LRCK.)	16fs/32fs	100
PCM monaural (Synchronized with High of LRCK.)		101

3.5.2. Setting of Frame Size of SDATA (DI/DO)

A frame size means a BCK cycle count per audio channel.
For the I2S stereo format and the LR stereo format, a 1-frame-period is a half of a 1-sampling-cycle because 1 sampling data consists of 2 channels (L channel and R channel).
For the PCM monaural format, a 1-frame-period is a 1-sampling-cycle.
The frame size of the SDATA (DI/DO) should be set to 16 cycles or 32 cycles in ***[I2SxCAUDIOSET]***<SCLKtoWS>, ***[I2SxIAUDIOSET]***<SCLKtoWS>, and ***[I2SxOAUDIOSET]***<SCLKtoWS>.

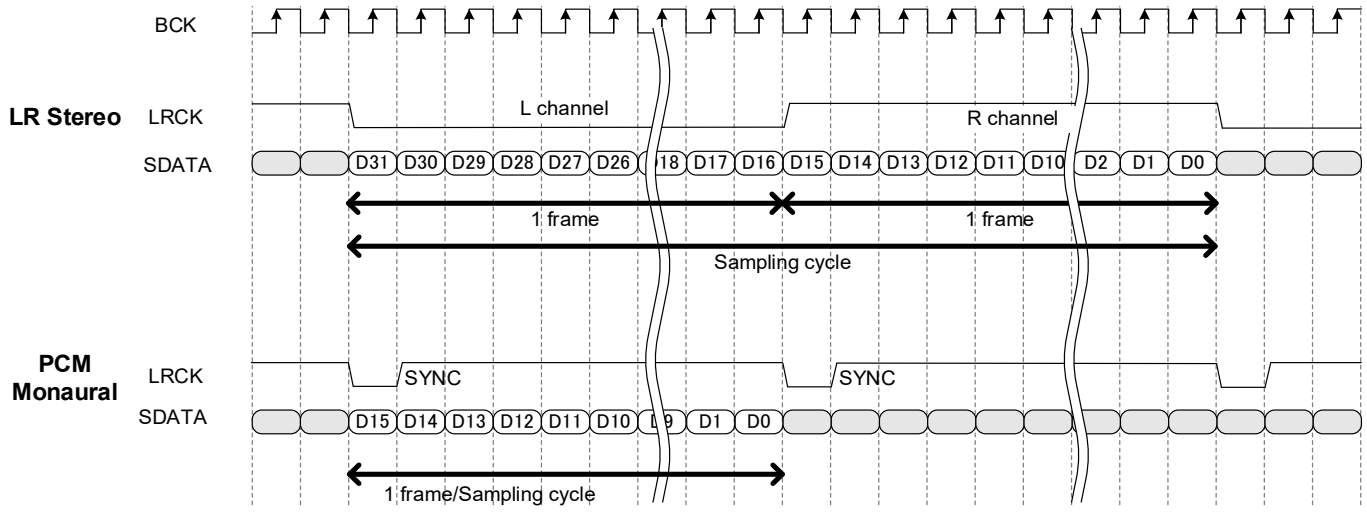


Figure 3.6 Example of Frame size (for 16 cycles)

3.5.3. Data Length

For the I2S stereo and the LR stereo formats, the data length means the bit count of the SDATA per sampling of each of the L and R channel. For the PCM monaural format, it means the bit count of the SDATA per sampling. The data length can be selected from among 8, 16, 24, and 32 bits for the I2S stereo, the LR stereo, and the PCM monaural formats, using ***[I2SxCAUDIOSET]***<WordLen[5:0]>, ***[I2SxIAUDIOSET]***<WordLen[5:0]>, and ***[I2SxOAUDIOSET]***<WordLen[5:0]>.

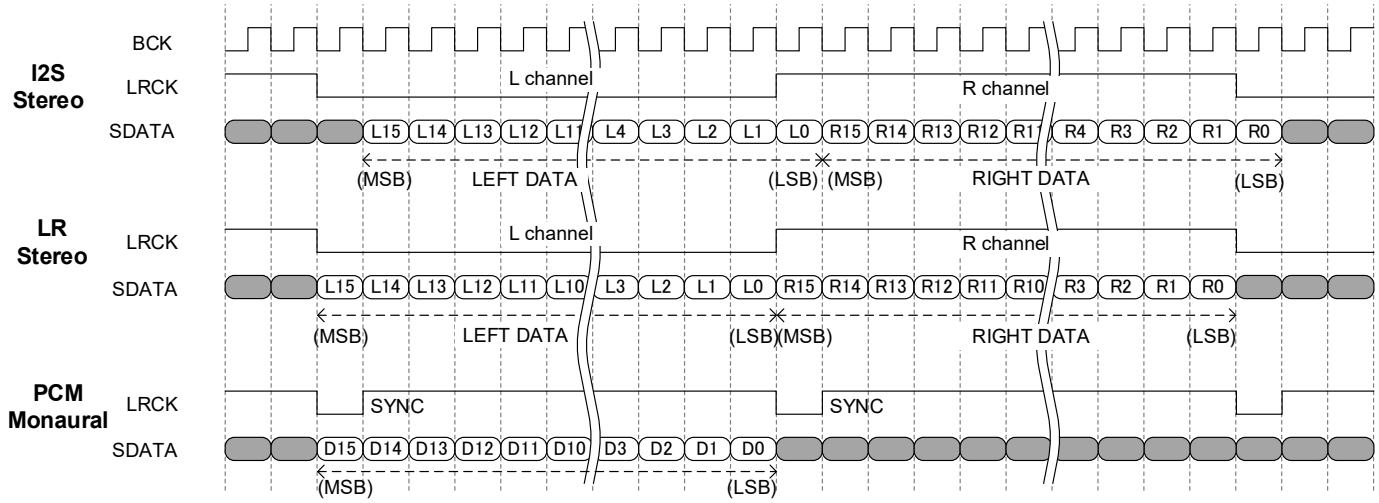


Figure 3.7 Audio formats for 16-bit data length (for Stereo 32fs/Monaural 16fs)

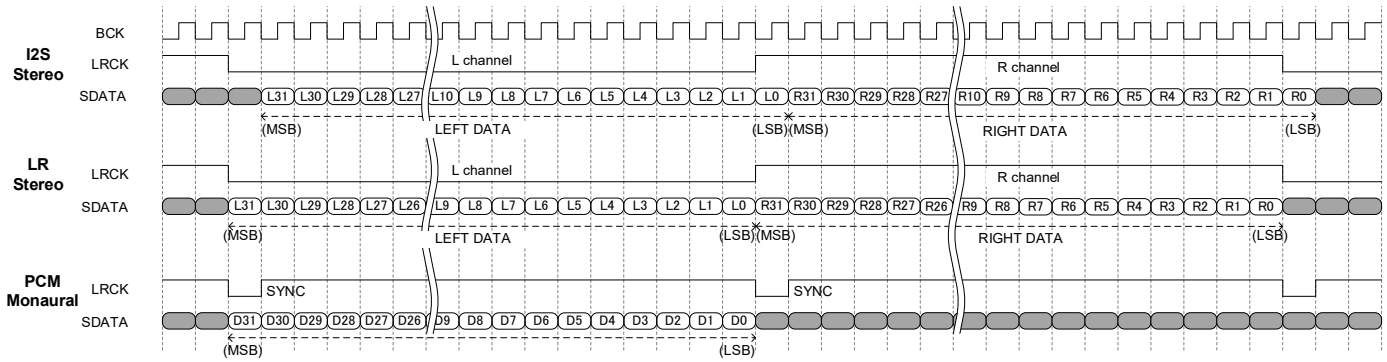


Figure 3.8 Audio formats for 32-bit data length (for Stereo 64fs/Monaural 32fs)

Table 3.3 shows examples of the setting of each audio format.

Table 3.3 Register setting examples of Audio format

Audio format	BCK frequency	Data length [bit]	*[I2SxCMODESET] [I2SxIMODESET] [I2SxOMODESET]*	*[I2SxCAUDIOSET] [I2SxIAUDIOSET] [I2SxOAUDIOSET]*	*[I2SxCAUDIOSET] [I2SxIAUDIOSET] [I2SxOAUDIOSET]*
			<WS[2:0]>	<SCLKtoWS>	<WordLen[5:0]>
I2S stereo	32fs	8	000	0	001000
		16			010000
	64fs	8		1	001000
		16			010000
		24			011000
		32			100000
LR stereo	32fs	8	010	0	001000
		16			010000
	64fs	8		1	001000
		16			010000
		24			011000
		32			100000
PCM monaural	16fs	8	100	0	001000
		16			010000
	32fs	8		1	001000
		16			010000
		24			011000
		32			100000

3.5.4. Clock Edge

The LRCK and the SDATA are synchronous with the rising edge or the falling edge of the BCK.

The output timing of the LRCK from the clock control circuit should be set in ***[I2SxCAUDIOSET]***<Edge>.
The input timings of the LRCK for the transmission control and the reception control should be set in ***[I2SxOAUDIOSET]***<Edge> and ***[I2SxIAUDIOSET]***<Edge>, respectively.

The output timing of the SDATA from the transmission control circuit should be set in ***[I2SxOAUDIOSET]***<SDEdge>, and the input timing of the SDATA into the reception control circuit should be set in ***[I2SxIAUDIOSET]***<SDEdge>.

- Rising edge mode:
  The LRCK and the SDATA are latched with the rising edge of the BCK (Reception: Sampling timing).
  The LRCK and the SDATA change at the falling edge of the BCK (Transmission: Output timing).

- Falling edge mode:
  The LRCK and the SDATA are latched with the falling edge of the BCK. The LRCK and the SDATA change at the rising edge of the BCK.

Table 3.4 Clock edge setting

Device operation	Mode	Clock control *[I2SxCAUDIOSET]*	Transmission control *[I2SxOAUDIOSET]*	Reception control *[I2SxIAUDIOSET]*
Master	Rising edge	<Edge> = 0	<Edge> = 1	<Edge> = 1
		<SDEdge>: Setting is unnecessary.	<SDEdge> = 0	<SDEdge> = 1
	Falling edge	<Edge> = 1	<Edge> = 0	<Edge> = 0
		<SDEdge>: Setting is unnecessary.	<SDEdge> = 1	<SDEdge> = 0
Slave	Rising edge	-	<Edge> = 1	<Edge> = 1
		-	<SDEdge> = 0	<SDEdge> = 1
	Falling edge	-	<Edge> = 0	<Edge> = 0
		-	<SDEdge> = 1	<SDEdge> = 0

The rising edge mode or the falling edge mode should be selected properly according to a connected device.

Figure 3.9 and Figure 3.10 show the waveforms of the rising edge mode and the falling edge mode, respectively.

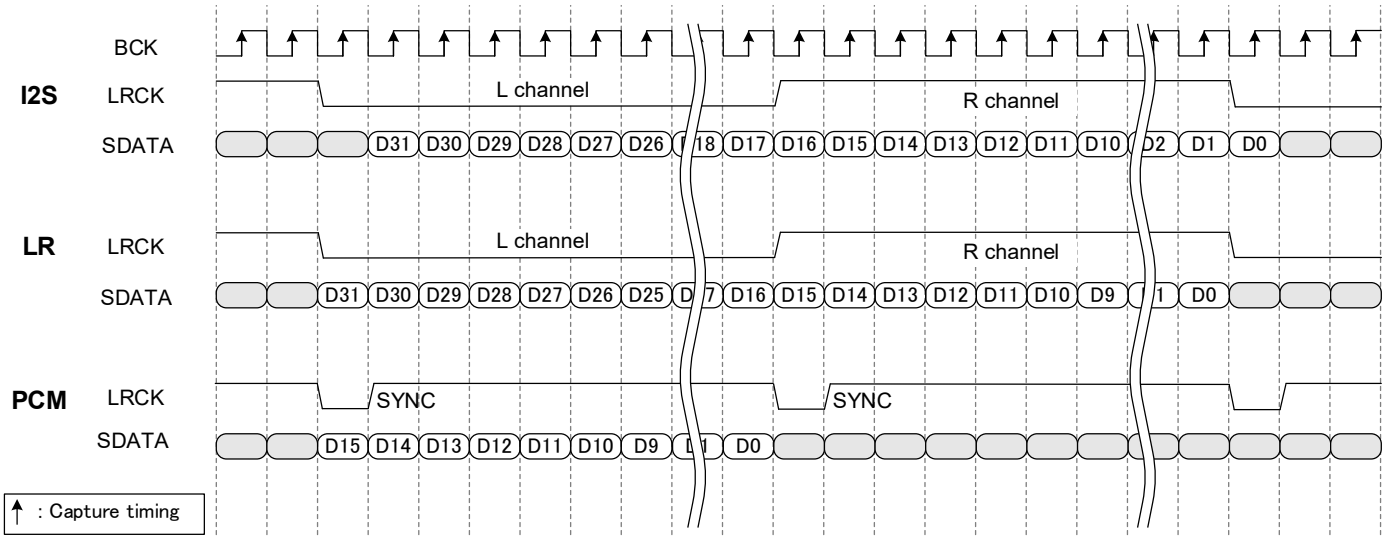


Figure 3.9 Timing of Rising edge mode

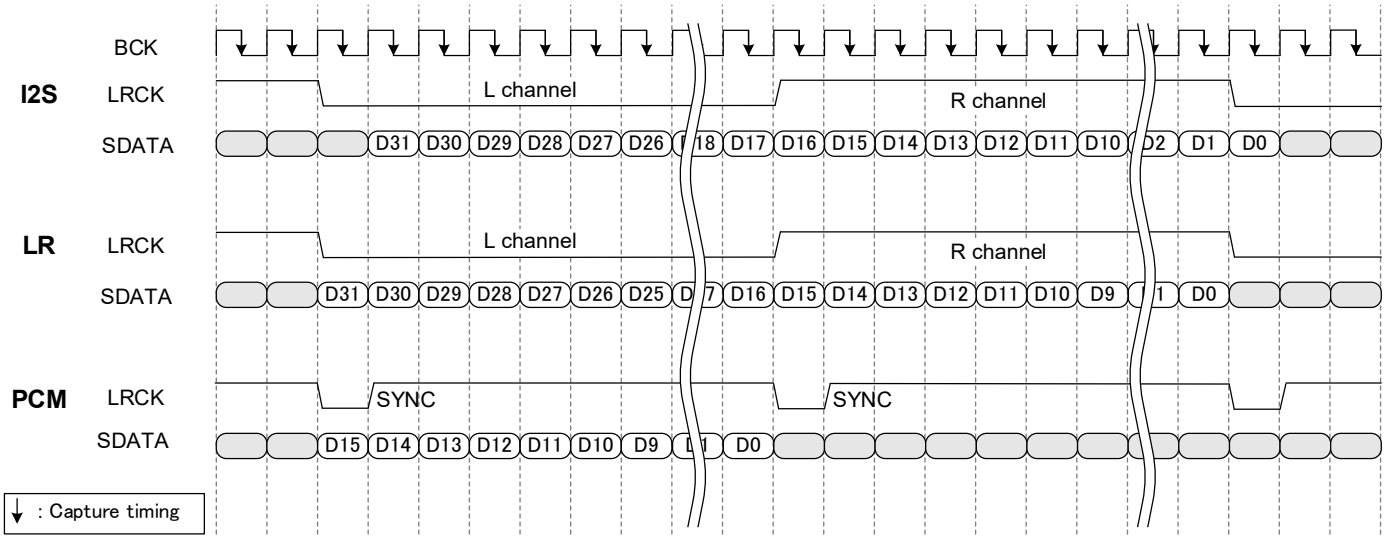


Figure 3.10 Timing of Falling edge mode

3.5.5. Sampling Frequency

The sampling frequency is one cycle of the LRCK for the I2S stereo and the LR stereo formats. And for the PCM monaural format, it is the cycle time from the SYNC to another SYNC of the LRCK.

Table 3.5 shows examples of the sampling frequency and the register setting.
For the frequency setting of the output master clock, refer to Table 3.1.

Table 3.5 Setting examples of Sampling frequency

Sampling frequency (kHz)	BCK frequency (Stereo/Monaural)	*[I2SxIAUDIOSET]*<SCLKtoWS> *[I2SxOAUDIOSET]*<SCLKtoWS>	Master clock frequency (MHz)
48	32fs/16fs	0 (16 cycles)	0.768
96	32fs/16fs	0 (16 cycles)	1.536
192	32fs/16fs	0 (16 cycles)	3.072
48	64fs/32fs	1 (32 cycles)	1.536
96	64fs/32fs	1 (32 cycles)	3.072
192	64fs/32fs	1 (32 cycles)	6.144

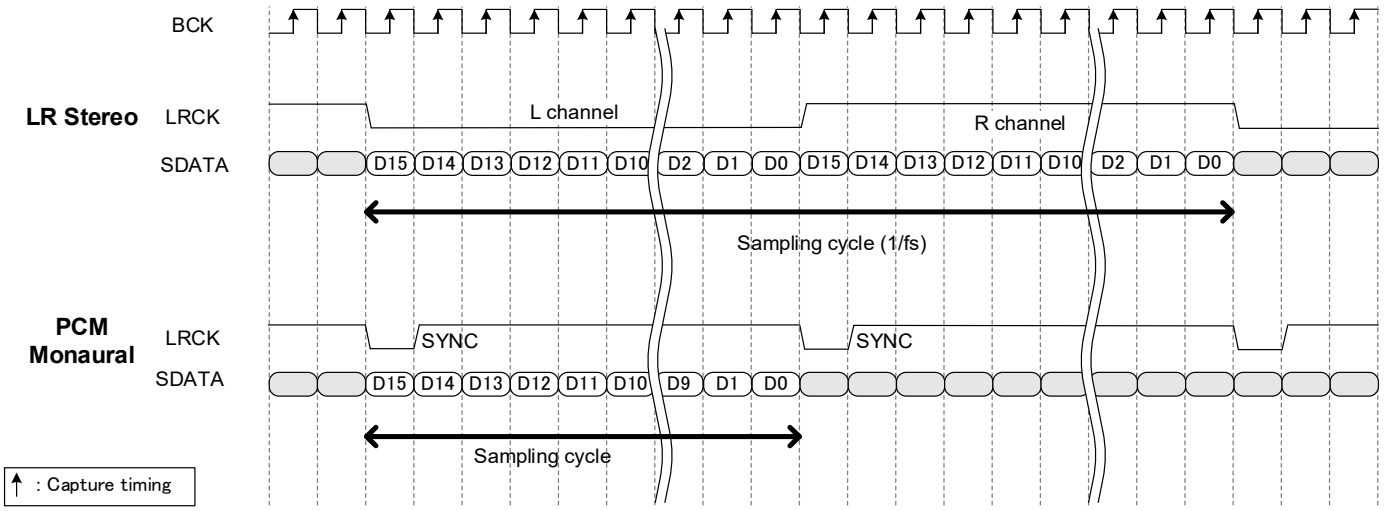


Figure 3.11 Example of Sampling cycle at <SCLKtoWS> = 0

3.6. Reception Buffer and Transmission Buffer

The reception data and the transmission data are stored in the reception buffer and the transmission buffer, respectively.
The reception buffer consists of a shift register, a receive FIFO, and reception data registers (***[I2SxILMEM00]*** to ***[I2SxILMEM63]***).

The transmission buffer consists of a transmission shift register, a transmit FIFO, and transmission data registers (***[I2SxOLMEM00]*** to ***[I2SxOLMEM63]***).

Both the receive FIFO and the transmit FIFO have 64 stages.

The width of one entry in the FIFO is 32 bits. One write access to the reception data register or the transmission data register writes data to one entry of the FIFO. And one read access to the register reads one entry of the FIFO. Therefore, 8-bit unit and 16-bit unit accesses cannot be done.

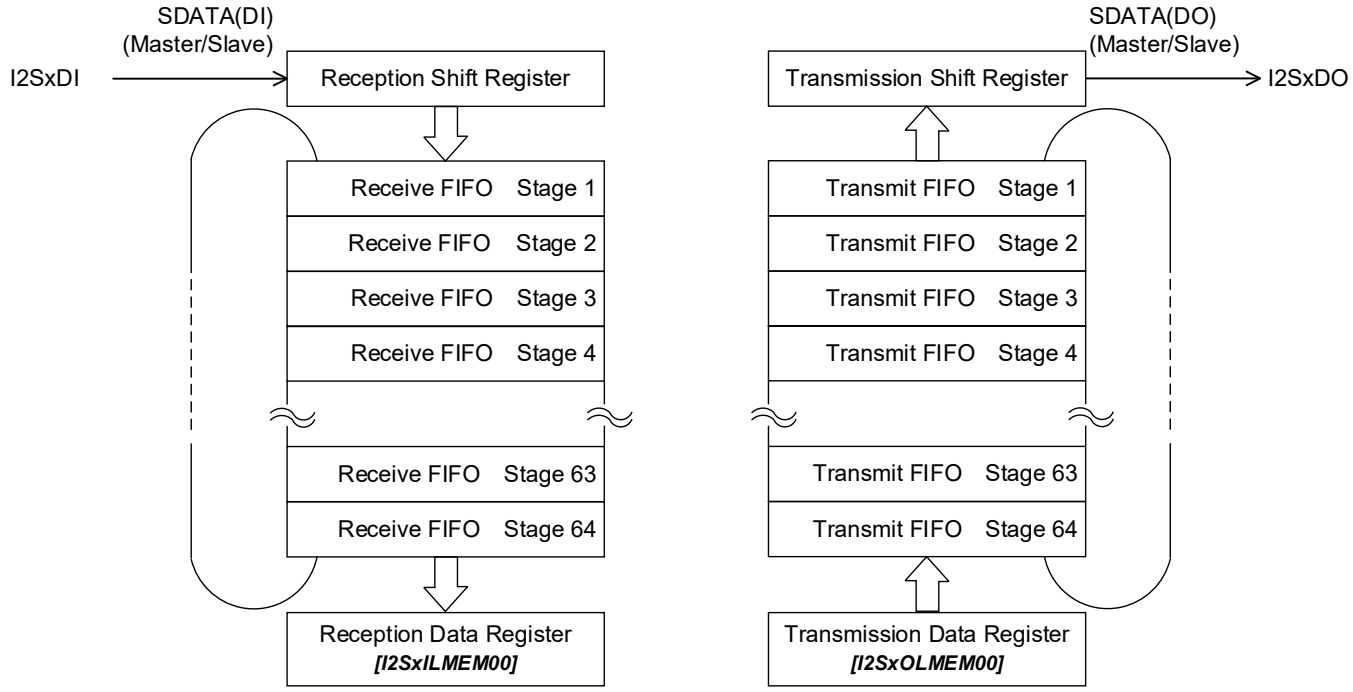


Figure 3.12 Configuration of Reception buffer and Transmission buffer

3.6.1. Receive FIFO

When all bits (1 frame) of the input data from the I2SxDI pin are stored into the reception shift register, the data is transferred to the receive FIFO. The reception write pointer moves to indicate the next stage. When the receive FIFO is read, the receive read pointer moves to indicate the next stage. The data in the receive FIFO can be read from the reception data registers (***[I2SxILMEM00]*** to ***[I2SxILMEM63]***).

During data reception, a read from any one of the reception data registers (***[I2SxILMEM00]*** to ***[I2SxILMEM63]***) obtains the data in the start stage of the FIFO.

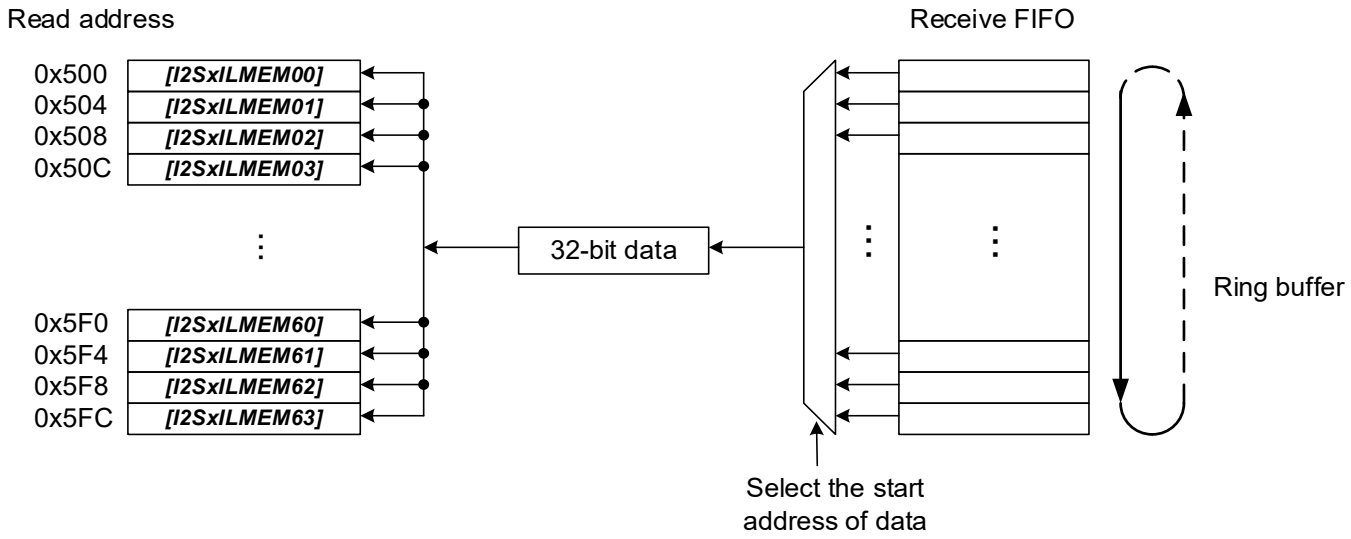


Figure 3.13 Access of Receive FIFO

3.6.2. Transmit FIFO

When data is written to the transmission shift register, it is stored to the transmit FIFO. The transmission write pointer moves to indicate the next stage. When data transmission is enabled, the transmission data is transferred from the transmit FIFO to the corresponding transmission data registers (***[I2SxOLMEM00]*** to ***[I2SxOILMEM63]***), and eventually, is output on the I2SxDO pin.
The stored data count of the transmit FIFO can be checked with ***[I2SxOFIFO_STS]***<FIFOStatus[6:0]>.
When ***[I2SxOSTART]***<SpkStart> is set to "1", the interrupt which notifies that the FIFO is empty is issued as well as a DMA request.

During data transmission, even when any one of the transmission data registers (***[I2SxOLMEM00]*** to ***[I2SxOILMEM63]***) is written, the data is stored at the stage next to the last in the FIFO. Therefore, continuous writes to one register, ***[I2SxOLMEM00]***, for example, and sequential writes from ***[I2SxOLMEM00]*** to ***[I2SxOLMEM63]*** result in the same.

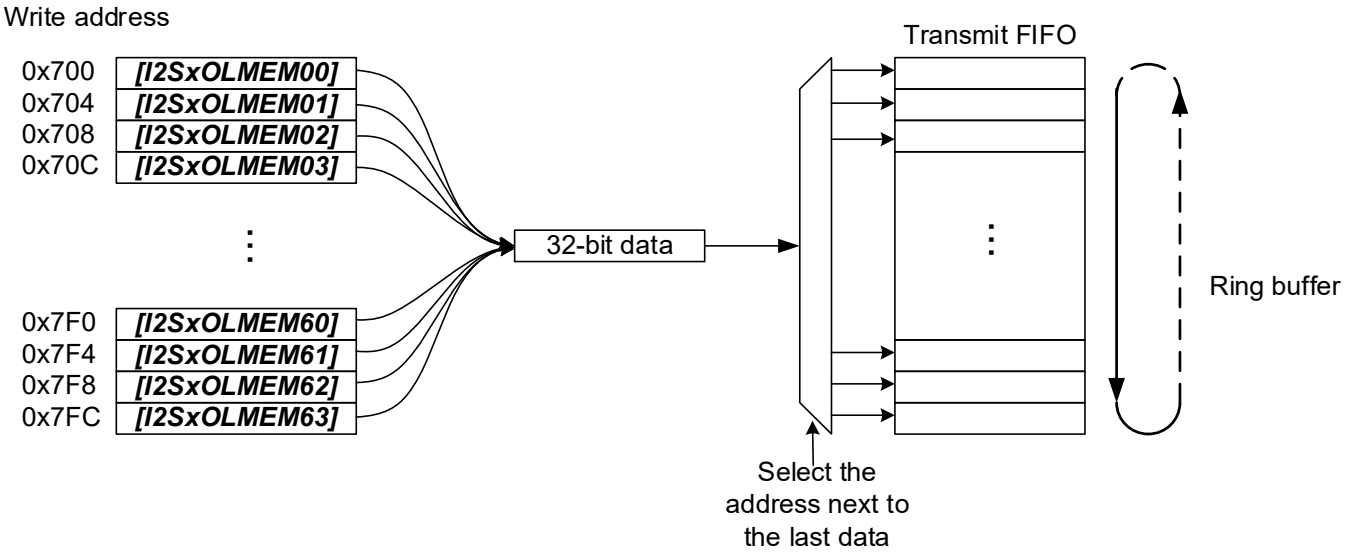


Figure 3.14 Access of Transmit FIFO

3.6.3. Transmission Start Threshold Value (*[I2SxOTX_SSIZE]*)

The I2Sx has a function that starts serial transfer after a specified count of data are written to the transmit FIFO. Only the transmission circuit supports the function. The transmit FIFO is empty at first and data is stored to the transmit FIFO. When the count of the stored data exceed the specified value, the serial transfer can start automatically. Owing to this function, an underrun error may hardly occur because a specified amount of data are in the FIFO before the serial transfer starts.

The transmission of the SDATA starts after the stored data count exceeds the specified value in the buffer. This setting affects the first data output after ***[I2SxOSTART]***<SpkStart> is set to "1".

When the access to the transmit FIFO is completed and the entry count in the transmit FIFO becomes the value in ***[I2SxOTX_SSIZE]***<TxStartSize> or more, the data transmission starts with the next frame (LR frame).

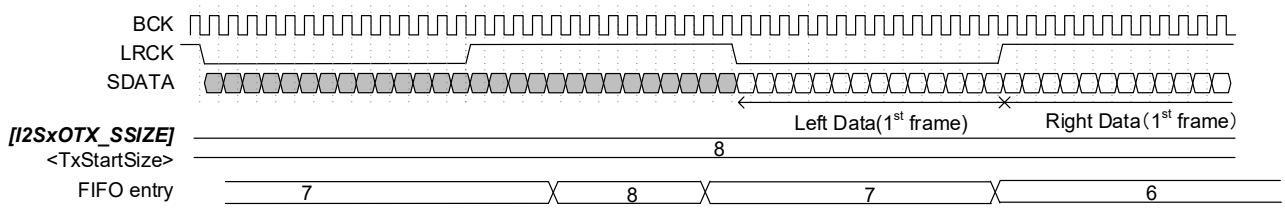


Figure 3.15 Data transfer at *[I2SxOTX_SSIZE]*<TxStartSize> = 8

3.6.4. Data storage format

The transmission data registers (***[I2SxOLMEM00]*** to ***[I2SxOLMEM63]***) and the reception data registers (***[I2SxILMEM00]*** to ***[I2SxILMEM63]***) are accessed with the units of 32 bits. If the SDATA (DI/DO) length is less than 32 bits, a data storage format can be selected for the data registers.

The data length should be set to ***[I2SxIAUDIOSET]***<WordLen[5:0]> for reception and to ***[I2SxOAUDIOSET]***<WordLen[5:0]> for transmission.
The data storage format type should be set to ***[I2SxIAUDIOSET]***<DTFmt> for reception and to ***[I2SxOAUDIOSET]***<DTFmt> for transmission.

Table 3.6 Setting of Data storage format

Data length	Data length setting <WordLen[5:0]>	Data storage format setting <DTFmt>	Data storage format
32 bits	100000	-	<DTFmt> does not affect.
24 bits	011000	0	(LSB justification) Lower 24 bits are valid.
		1	(MSB justification) Upper 24 bits are valid.
16 bits	010000	0	(Lower-first) Output: LSB is output first. Input: The first input data is stored in the LSB.
		1	(Upper-first) Output: MSB is output first. Input: The first input data is stored in the MSB.
8 bits	001000	0	(Lower-first) Output: LSB is output first. Input: The first input data is stored in the LSB.
		1	(Upper-first) Output: MSB is output first. Input: The first input data is stored in the MSB.

Note: If "right justification" and "LSB-first" are necessary, software should perform them.

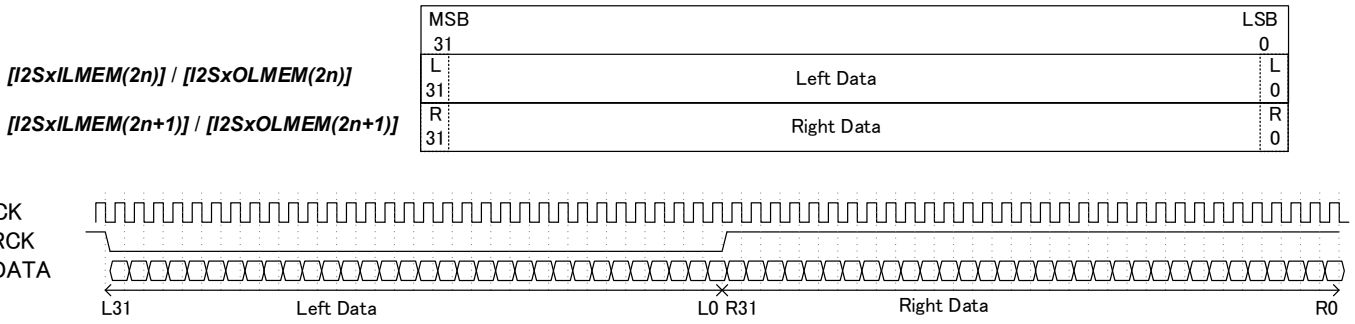


Figure 3.16 Data storage format and Audio format for 32-bit data length

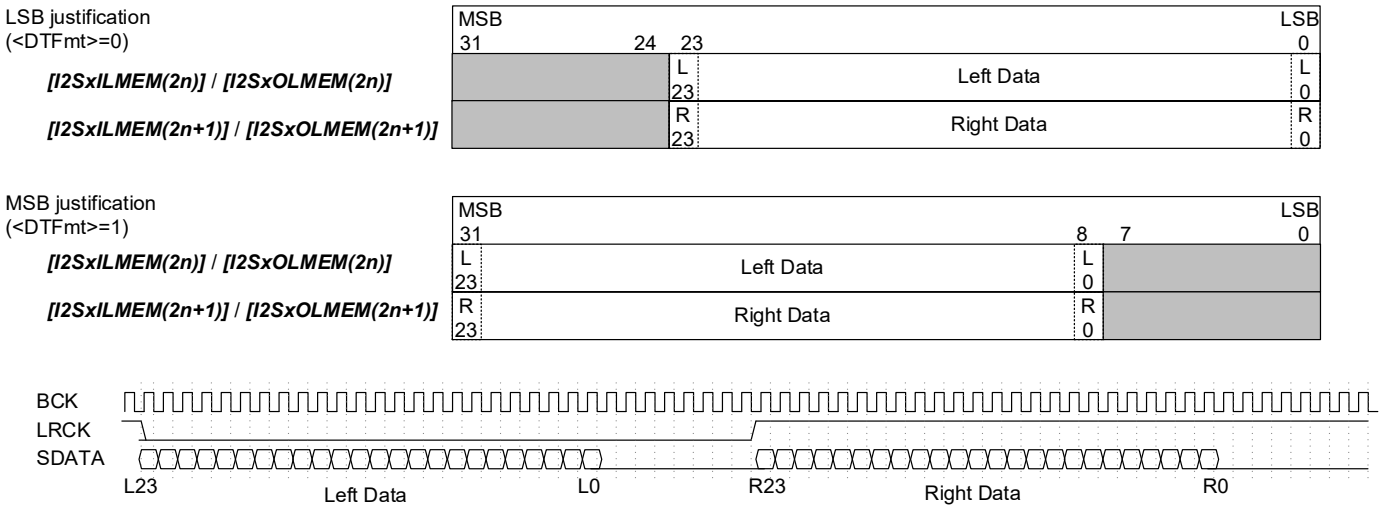


Figure 3.17 Data storage format and Audio format for 24-bit data length

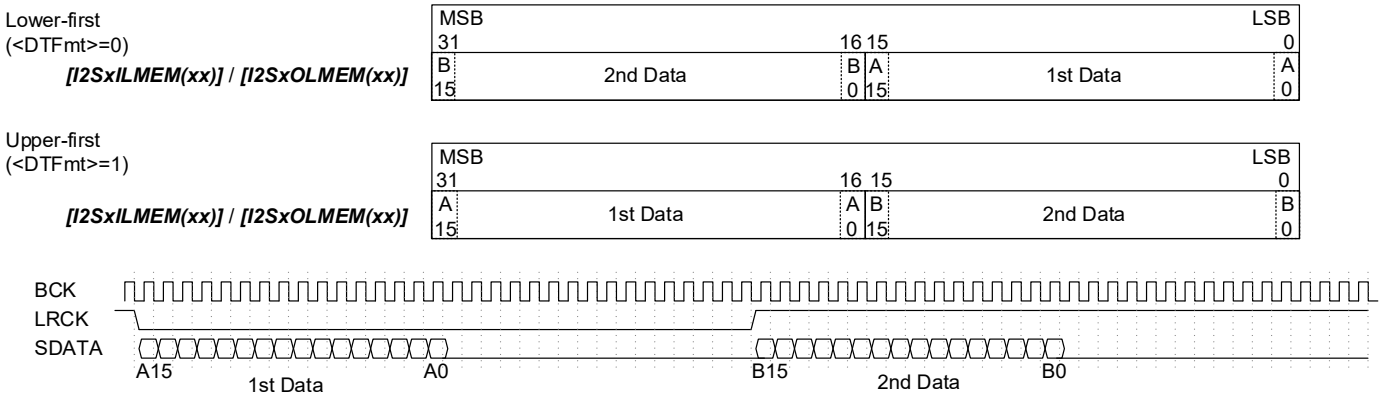


Figure 3.18 Data storage format and Audio format for 16-bit data length

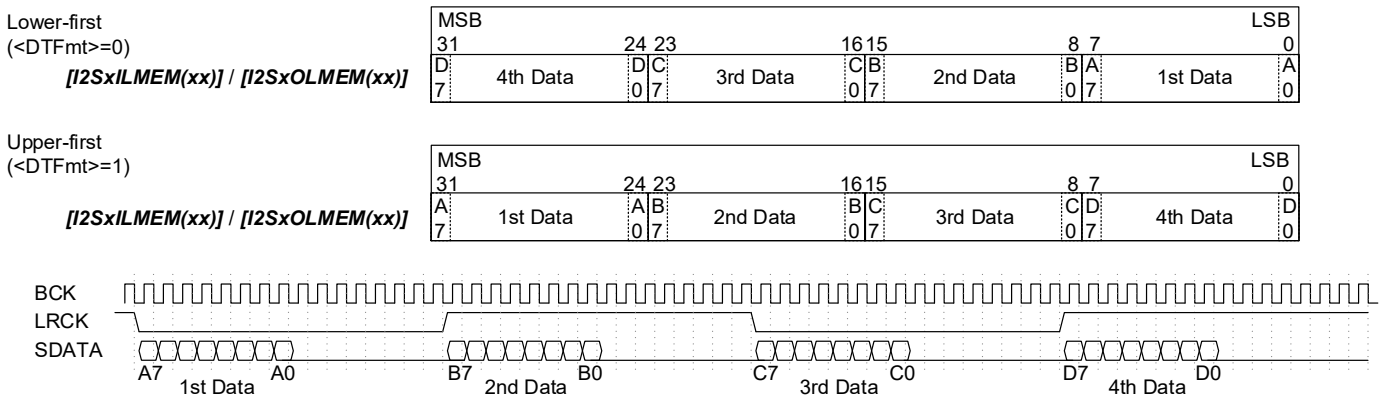


Figure 3.19 Data storage format and Audio format for 8-bit data length

3.6.5. *[I2SxITHRESHOLD]* and *[I2SxOTHRESHOLD]* Registers

The data transfer request timing can be set to issue the INTI2SxSI interrupt, the INTI2SxSO interrupt, and the DMA request. And the notification timing can be set for the data transfer request to the FIR.

(1) Setting of Data transfer request timing

During data reception, when the stored data in the receive FIFO becomes the value of ***[I2SxITHRESHOLD]***<threshold[4:0]> +1 or more, the INTI2SxSI interrupt and the reception DMA request are asserted. Then, the CPU or the DMA reads the receive FIFO. In order to generate the next interrupt, the FIFO should be read ***[I2SxITHRESHOLD]***<threshold[4:0]> +1 times.

During data transmission, when the empty stage becomes ***[I2SxOTHRESHOLD]***<threshold[4:0]> +1 or more, the INTI2SxSO interrupt and the transmission DMA request are asserted. Then, the CPU or the DMA writes the transmit FIFO. In order to generate the next interrupt, the FIFO should be written ***[I2SxITHRESHOLD]***<threshold[4:0]> +1 times.

(2) Setting of Notification timing to the FIR

When the receive FIFO stores the data of the ***[I2SxITHRESHOLD]***<threshold[4:0]>+1 or more, or the transmit FIFO has the empty stages of the ***[I2SxOTHRESHOLD]***<threshold[4:0]>+1 or more, the FIR is notified of proper information.

3.7. Interrupt

The reception interrupts are the INTI2SxSIERR interrupt and the INTI2SxSI interrupt. The transmission interrupts are the INTI2SxSOERR interrupt and the INTI2SxSO interrupt.
The factors of the INTI2SxSIERR interrupt and the INTI2SxSOERR interrupt are an LRCK error, an underrun error, and an overrun error.
The factor of the INTI2SxSI interrupt and the INTI2SxSO interrupt is a data transfer request. The data transfer request also causes to generate the DMA request (I2SxRXDMAREQ and I2SxTXDMAREQ) to the DMAC. It is necessary to mask one of the transmission/reception data completion interrupt and the transmission/reception DMA request.

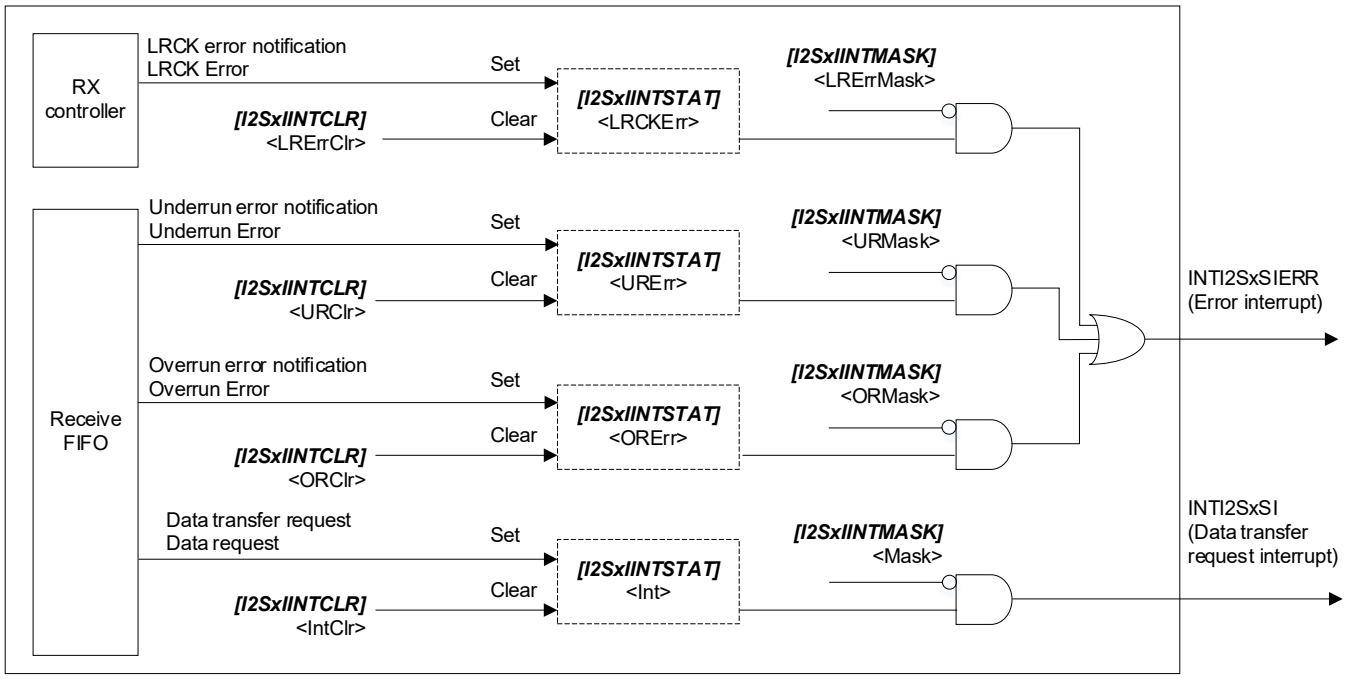


Figure 3.20 Reception interrupt control

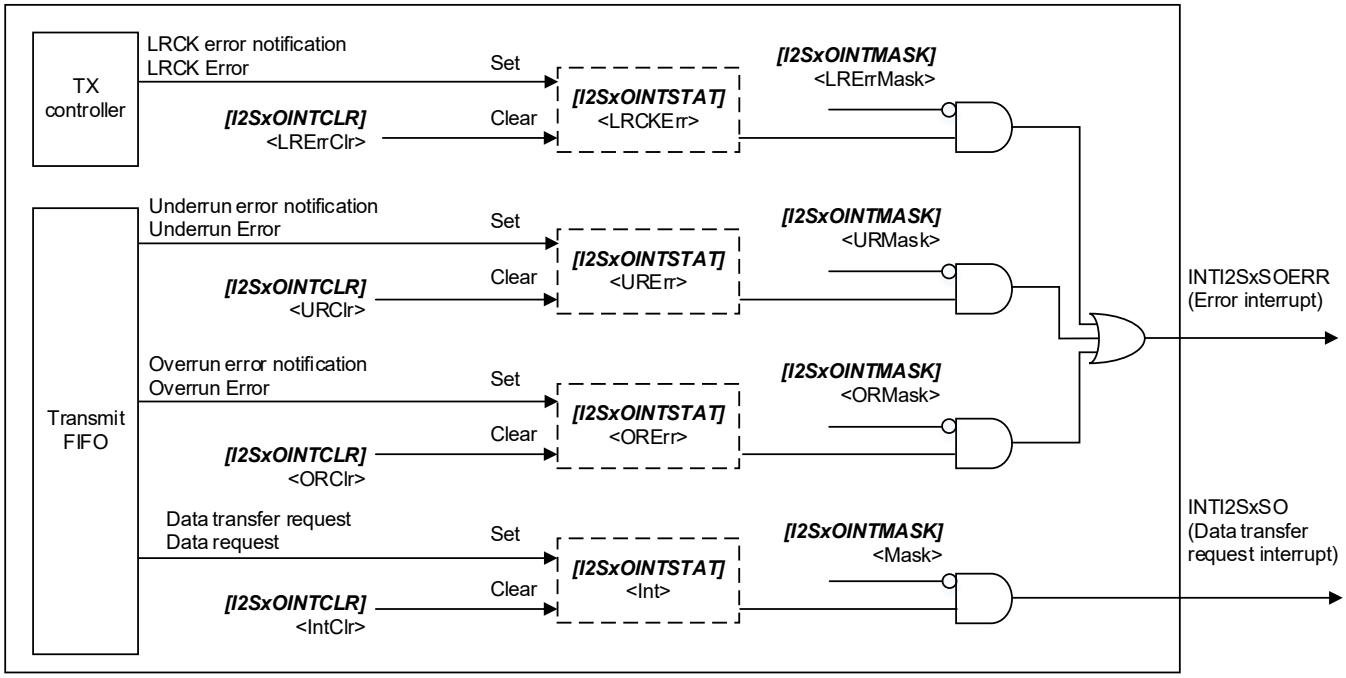


Figure 3.21 Transmission interrupt control

When an interrupt factor is detected, the corresponding bit is set to "1" in the ***[I2SxIINTSTAT]*** and the ***[I2SxOINTSTAT]*** registers.
When proper bits in the ***[I2SxIINTMASK]*** and ***[I2SxOINTMASK]*** registers are set to "1", the corresponding interrupt is masked and is not generated. Even though the mask is set, the occurrence of the factor can be checked in the ***[I2SxIINTSTAT]*** and the ***[I2SxOINTSTAT]*** registers.
The interrupt factor in the ***[I2SxIINTSTAT]*** and ***[I2SxOINTSTAT]*** can be cleared by setting "1" to the corresponding bits in the ***[I2SxIINTCLR]*** and ***[I2SxOINTCLR]*** registers.

Table 3.7 Interrupt factor and register

Module	Interrupt signal	Interrupt factor	Interrupt status register	Interrupt factor clear register	Interrupt mask register
Reception control	INTI2SxSI	Data transfer request	***[I2SxIINTSTAT]*** <Int>	***[I2SxIINTCLR]*** <IntClr>	***[I2SxIINTMASK]*** <Mask>
	INTI2SxSIERR	FIFO overrun	***[I2SxIINTSTAT]*** <OREr>	***[I2SxIINTCLR]*** <ORClr>	***[I2SxIINTMASK]*** <ORMask>
		FIFO underrun	***[I2SxIINTSTAT]*** <URErr>	***[I2SxIINTCLR]*** <URClr>	***[I2SxIINTMASK]*** <URMask>
		LRCK error	***[I2SxIINTSTAT]*** <LRCKErr>	***[I2SxIINTCLR]*** <LRErrClr>	***[I2SxIINTMASK]*** <LRErrMask>
Transmission control	INTI2SxSO	Data transfer request	***[I2SxOINTSTAT]*** <Int>	***[I2SxOINTCLR]*** <IntClr>	***[I2SxOINTMASK]*** <Mask>
	INTI2SxSOERR	FIFO overrun	***[I2SxOINTSTAT]*** <OREr>	***[I2SxOINTCLR]*** <ORClr>	***[I2SxOINTMASK]*** <ORMask>
		FIFO underrun	***[I2SxOINTSTAT]*** <URErr>	***[I2SxOINTCLR]*** <URClr>	***[I2SxOINTMASK]*** <URMask>
		LRCK error	***[I2SxOINTSTAT]*** <LRCKErr>	***[I2SxOINTCLR]*** <LRErrClr>	***[I2SxOINTMASK]*** <LRErrMask>

3.7.1. INTI2SxSI Interrupt and INTI2SxSO Interrupt

The factor of the INTI2SxSI and INTI2SxSO interrupts is a data transfer request. The data transfer request is generated when the receive FIFO or the transmit FIFO is ready to transfer data.

The reception control generates the data transfer request when the receive FIFO stores data equal to or more than ***[I2SxITHRESHOLD]***<threshold[4:0]> +1, and ***[I2SxIINTSTAT]***<Int> is set to "1". When ***[I2SxIINTSTAT]***<Int> is "0", the data in the FIFO cannot be read.
The transmission control generates the data transfer request when the transmit FIFO has empty stages equal to or more than ***[I2SxOTHRESHOLD]***<threshold[4:0]> +1, and ***[I2SxOINTSTAT]***<Int> is set to "1". When ***[I2SxOINTSTAT]***<Int> is "0", any data cannot be write to the FIFO.

When the data transfer request is cleared, ***[I2SxIINTCLR]*** <IntClr> and ***[I2SxOINTCLR]*** <IntClr> should be set to "1".

When the interrupt status register is set to "1" and the corresponding mask bit is "0", the INTI2SxSI interrupt or the INTI2SxSO interrupt is generated.

When the data transfer request is used as the factor of the transmission DMAC request and the reception DMAC request, ***[I2SxIINTCLR]***<IntClr> and ***[I2SxOINTCLR]***<IntClr> should not be set to "1". And the transmission and reception data transfer request interrupts should be masked. (For the transmission and reception DMA requests, refer to "3.8. DMA".)

3.7.2. INTI2SxSIERR Interrupt and INTI2SxSOERR Interrupt

The factors of the INTI2SxSIERR and the INTI2SxSOERR interrupts are an LRCK error, an underrun error, and an overrun error.

The LRCK error occurs when the change timing of the LRCK signal is different from the setting. When it occurs, ***[I2SxIINTSTAT]***<LRCKErr> = 1 and ***[I2SxOINTSTAT]***<LRCKErr> = 1 are set. In order to clear the LRCK error, ***[I2SxIINTCLR]***<LRErrClr> and ***[I2SxOINTCLR]***<LRErrClr> should be set to "1".

The underrun error occurs when data read is done from the FIFO which has no read data. When it occurs, ***[I2SxIINTSTAT]***<URErr> = 1 and ***[I2SxOINTSTAT]***<URErr> = 1 are set. In order to clear the underrun error, ***[I2SxIINTCLR]***<URClr> and ***[I2SxOINTCLR]***<URClr> should be set to "1". The error address is stored in the ***[I2SxOEPTR]*** register.

The overrun error occurs when data write is done to the FIFO which has no empty entries. When it occurs, ***[I2SxIINTSTAT]***<ORErr> = 1 and ***[I2SxOINTSTAT]***<ORErr> = 1 are set. In order to clear the overrun error, ***[I2SxIINTCLR]***<ORClr> and ***[I2SxOINTCLR]***<ORClr> should be set to "1". The error address is stored in the ***[I2SxIEPTR]*** register.

The factors of the error interrupts can be masked by setting <LRErrMask>, <URMask>, and <ORMask> in the ***[I2SxIINTMASK]*** and ***[I2SxOINTMASK]*** registers.

The INTI2SxSIERR interrupt or the INTI2SxSOERR interrupt is generated when one of the LRCK error, the underrun error, and the overrun error bits in the interrupt status register is "1" and the corresponding bit of the mask register is "0".

3.8. DMA Request

The I2Sx transmission control and reception control can reduce CPU load at communication because a transfer request can be issued directly to the DMAC.

The DMAC accesses the transmit FIFO or the receive FIFO by reading or writing ***[I2SxILMEM00]*** to ***[I2SxILMEM63]*** / ***[I2SxOLMEM00]*** to ***[I2SxOLMEM63]*** registers.
In the transmission control, the transmission DMA request (I2SxTXDMAREQ) is issued when the transmit FIFO has the space of N entries or more. In the reception control, the reception DMA request (I2SxRXDMAREQ) is issued when the receive FIFO has the data of N entries or more. The DMAC receives the transfer request and starts the access to the FIFO.
The value N is a threshold value of the data transfer request. The value should be set in the ***[I2SxITHRESHOLD]*** or ***[I2SxOTHRESHOLD]*** register; N is the setting value +1. For example, ***[I2SxITHRESHOLD]***<threshold[4:0]> = 31 means N = 32(128 bytes).

The cause factor of the DMA request (I2SxRXDMAREQ or I2SxTXDMAREQ) is a data transfer request. The data transfer request is a cause factor of the INTI2SxSI and the INTI2SxSO interrupts. When the DMA request (I2SxRXDMAREQ or I2SxTXDMAREQ) is issued, the INTI2SxSI and the INTI2SxSO interrupts should be masked using ***[I2SxIINTMASK]*** <Mask> and ***[I2SxOINTMASK]***<Mask>.

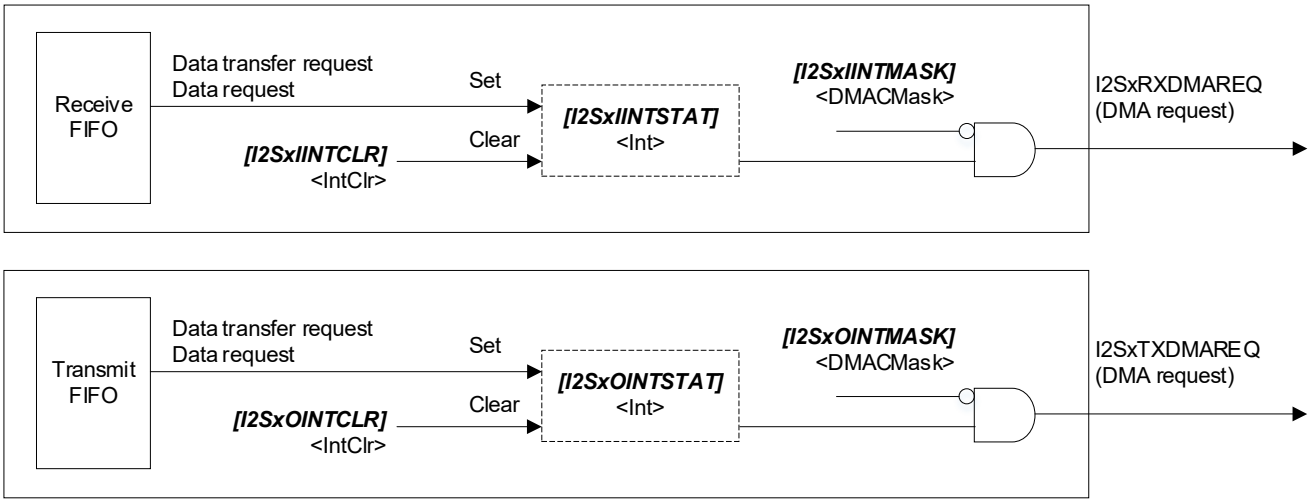
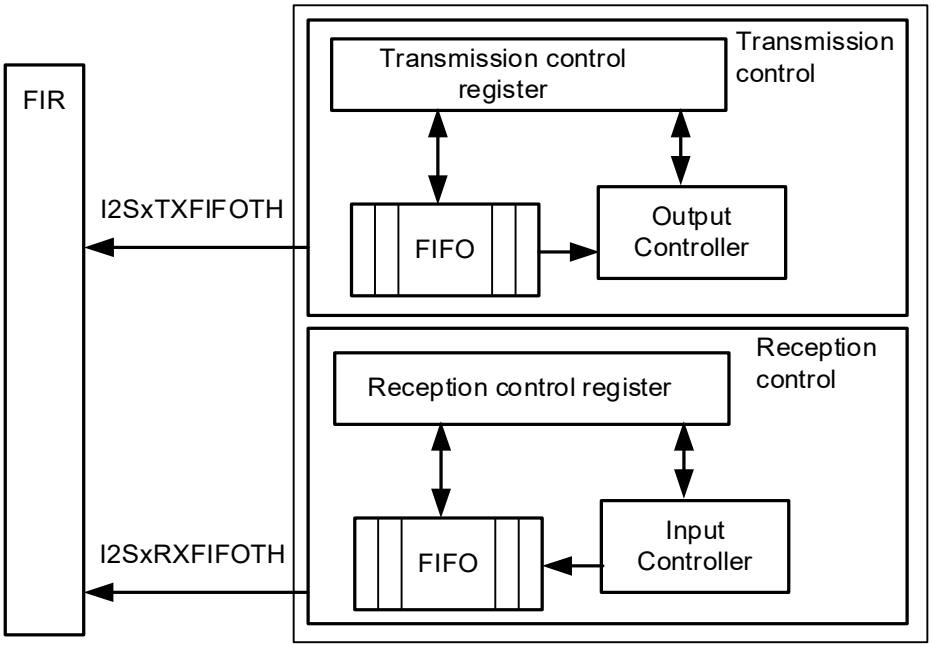


Figure 3.22 DMA request

3.9. FIR Linkage

When the transmit FIFO has the space of N entries or more, or when the receive FIFO has the data of N entries or more, the FIR is notified. The values N is a threshold value of the data transfer request. It is set to the ***[I2SxITHRESHOLD]*** or ***[I2SxOTHRESHOLD]*** register.

Using the notification from the I2Sx, the FIR can do the link operation with the I2Sx. For the details, refer to "FIR calculation Circuit" in the Reference manual.



Note: For the connections of each product, refer to "Product Information".

Figure 3.23 Example of connection with FIR

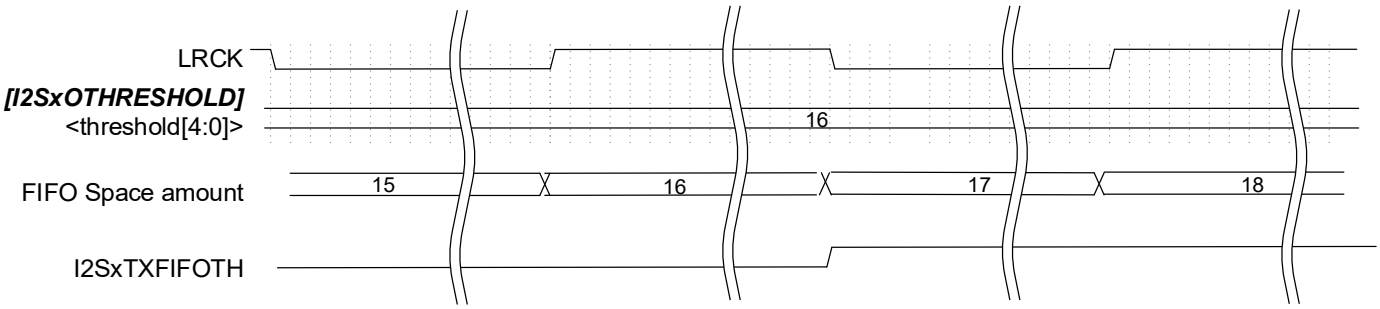


Figure 3.24 I2SxTXFIFOTH issue timing at *[I2SxOTHRESHOLD]*<threshold[4:0]> = 16 (for Transmission)

3.10. Mute Function

3.10.1. Mute by Register Setting

The mute ON and OFF can be switched during operation by writing the mute registers ***[I2SxIMUTE]***<MuteN> and ***[I2SxOMUTE]***<MuteN>.
The mute state is valid at the beginning of the LR channels after the register is set and its internal process is done.
When the mute is set to ON, the data transfer of the transmission or the reception continues, but the data is forcibly converted to "0".

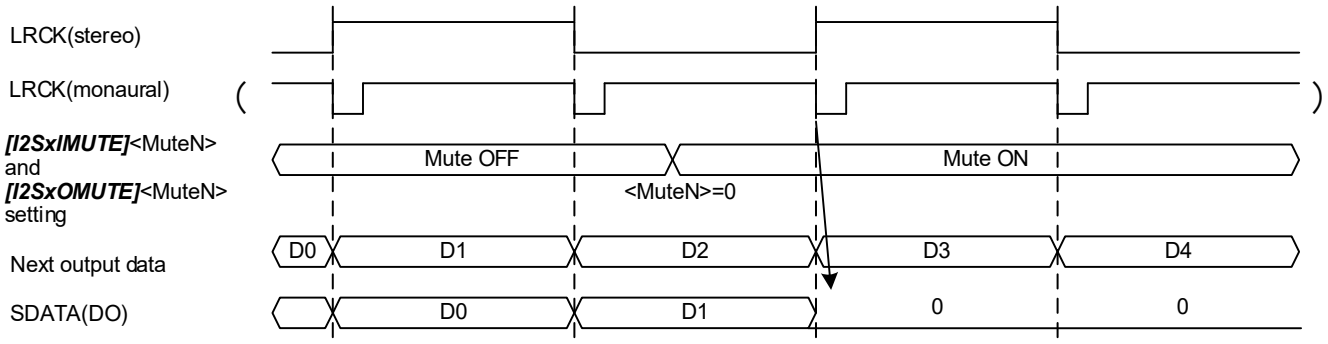


Figure 3.25 Mute setting (OFF to ON)

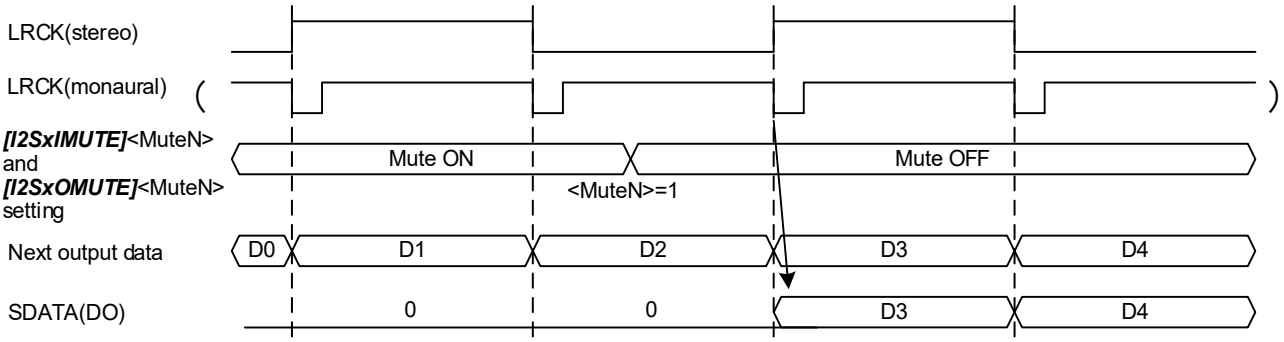


Figure 3.26 Mute setting (ON to OFF)

3.10.2. Forced Mute at Underrun

When a buffer underrun occurs, the next channel data and the subsequent data are forced to be "0". For the details of the process for the underrun occurrence, refer to "5.1.4.1. Overrun Error or Underrun Error Interrupt Occurrence".

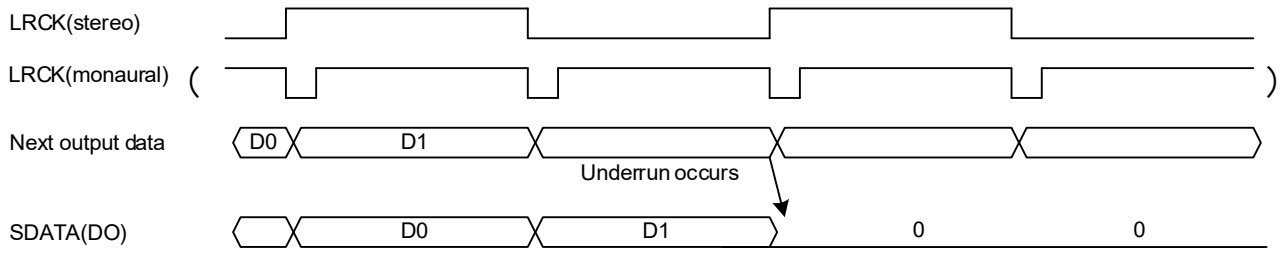


Figure 3.27 Forced mute

4. Registers

4.1. List of Registers

The control registers and their addresses are shown in the following table.

Function		channel/unit	Base address		
			Type1	Type2	Type3
I^2S interface	I2S	ch0	-	0x400D0000	-
		ch1	-	0x400D0800	-

Note: The base address type are different by products. For the details, refer to "Product Information" in the Reference manual.

(1) Clock control registers

Register Name		Address (Base+)
LRCK Generating Start Register	***[I2SxCSTART]***	0x0004
LRCK Generating Status Register	***[I2SxCBUSY]***	0x0008
LRCK Generation Stop Register	***[I2SxCSTOP]***	0x000C
AUDIOSET Register	***[I2SxCAUDIOSET]***	0x0010
REGBUSY Register	***[I2SxCREGBUSY]***	0x0040
Audio Data Format Setting Register	***[I2SxCMODESET]***	0x00F8
Master / Slave Select Register	***[I2SxCMS_SEL]***	0x0200
MCLK pin Input/Output select Register	***[I2SxCMCLK_IO_SEL]***	0x0204
ΦT0 Dividing Setting Register	***[I2SxCPHT_DIV]***	0x0214
ΦT0 Dividing Clock Output Enable Register	***[I2SxCPHT_DIVOUT_EN]***	0x0218
BCK Source Clock Select Register	***[I2SxCBCK_SRC_SEL]***	0x0220
BCK Dividing Setting Register	***[I2SxCBCK_DIV]***	0x0224
BCK Output Enable Register	***[I2SxCBCK_DIVOUT_EN]***	0x0228

(2) Reception Control Registers

Register Name		Address (Base+)
Reception Control Start Register	***[I2SxISTART]***	0x0404
Reception Operation Status Register	***[I2SxIBUSY]***	0x0408
Stopping Reception Data Register	***[I2SxISTOP]***	0x040C
Reception AUDIOSET Register	***[I2SxIAUDIOSET]***	0x0410
Reception Control Interrupt Source Status Register	***[I2SxIINTSTAT]***	0x0414
Reception Control Interrupt Mask Register	***[I2SxIINTMASK]***	0x0418
Reception Control Interrupt source Clear Register	***[I2SxIINTCLR]***	0x041C
Reception Mute Setting Register	***[I2SxIMUTE]***	0x0424
Reception Control Error Occurrence Pointer Stored Register	***[I2SxIEPTR]***	0x0428
Reception REGBUSY Register	***[I2SxIREGBUSY]***	0x0440
Reception Threshold Setting Register	***[I2SxITHRESHOLD]***	0x0450
Reception FIFO Status Register	***[I2SxIFIFO_STS]***	0x0454
Reception Audio Data Format Setting Register	***[I2SxIMODESET]***	0x04F8
Reception Data Register 00 to 63	***[I2SxILMEM00] to [I2SxILMEM63]***	0x0500 to 0x05FC

(3) Transmission Control Registers

Register Name		Address (Base+)
Transmission Control Start Register	***[I2SxOSTART]***	0x0604
Transmission Operation Status Register	***[I2SxOBUSY]***	0x0608
Stopping Transmission Data Register	***[I2SxOSTOP]***	0x060C
Transmission AUDIOSET Register	***[I2SxOAUDIOSET]***	0x0610
Transmission Control Interrupt Source Status Register	***[I2SxOINTSTAT]***	0x0614
Transmission Control Interrupt Mask Register	***[I2SxOINTMASK]***	0x0618
Transmission Control Interrupt Source Clear Register	***[I2SxOINTCLR]***	0x061C
Transmission Mute Setting Register	***[I2SxOMUTE]***	0x0624
Transmission Control Error Occurrence Pointer Stored Register	***[I2SxOEPTR]***	0x0628
TX_SSIZE Register	***[I2SxOTX_SSIZE]***	0x0630
Transmission REGBUSY Register	***[I2SxOREGBUSY]***	0x0640
Transmission Threshold Setting Register	***[I2SxOTHRESHOLD]***	0x0650
Transmission FIFO Status Register	***[I2SxOFIFO_STS]***	0x0654
Transmission Audio Data Format Setting Register	***[I2SxOMODESET]***	0x06F8
Transmission Data Register 00 to 63	***[I2SxOLMEM00] to [I2SxOLMEM63]***	0x0700 to 0x07FC

"x" is Channel number.

4.2. Details of Clock Control Registers

4.2.1. *[I2SxCSTART]* (LRCK Generating Start Register)

Bit	Bit Symbol	After Reset	Type	Function
31:9	-	0	R	Read as "0".
8	Start	0	R/W	LRCK generating start setting 0: Ignored 1: LRCK generating start. When setting the <Start> to "1", the LRCK generating start. When the ***[I2SxCBUSY]***<Busy> is "0", writing "1" in this bit is valid.
7:1	-	0	R	Read as "0".
0	-	0	R/W	Write as "0".

Note1: When restart the transfer after transmission / reception stop, set <Start> to "1", after reading ***[I2SxCSTOP]*** and confirming that the stop processing is completed (***[I2SxCSTOP]***<I2S_STOP> = 0).

Note2: Confirm that the ***[I2SxCREGBUSY]*** is "0x00000000", before setting "1" to the <Start> bit.

Note3: Continuous access to the ***[I2SxCSTART]*** is prohibit. It is ignored even if it sets the ***[I2SxCSTART]***.

4.2.2. *[I2SxCBUSY]* (LRCK Generating Status Register)

Bit	Bit Symbol	After Reset	Type	Function
31:18	-	0	R	Read as "0".
17	-	0	R	Read as "0".
16	-	0	R	Read as "0".
15:9	-	0	R	Read as "0".
8	Busy	0	R	Status of LRCK generating operation 0: Stop 1: Operating
7:2	-	0	R	Read as "0".
1	-	0	R	Read as "0".
0	-	0	R	Read as "0".

4.2.3. *[I2SxCSTOP]* (LRCK Generation Stop Register)

Bit	Bit Symbol	After Reset	Type	Function
31:1	-	0	R	Read as "0".
0	I2S_STOP	0	R	Internal process status of stop operation. 0: Stop operation completed 1: Stop operation processing After setting "1" in <I2S_STOP>, this register returns "1" as a read data during processing the stop operation. This register returns "0" as a read data after completion of the stop operation.
			W	LRCK generation stop control 0: Ignored 1: Stop the LRCK generation The LRCK generation can be stopped by writing "1" to this register and cleared the internal status execpt setting registers and error interrupt status.

Note1: This register should be written "1" during the LRCK generation - when ***[I2SxCBUSY]***<Busy> is "1".

Note2: After setting <I2S_STOP> to "1", don't set <I2S_STOP> to "1" again during the stop processing operation. When set to "1", setting is ignored.

4.2.4. *[I2SxCAUDIOSET]* (AUDIOSET Register)

Bit	Bit Symbol	After Reset	Type	Function
31:17	-	0	R	Read as "0".
16	-	0	R/W	Write as "0".
15:13	-	0	R	Read as "0".
12	-	0	R/W	Write as "0".
11	Edge	0	R/W	LRCK sampling edge 0: The BCK falling edge. 1: The BCK rising edge. For settings, refer to Table 3.4.
10:9	-	0	R	Read as "0".
8	SCLKtoWS	0	R/W	Frame size of the SDATA 0: 16 cycles 1: 32 cycles A frame size means a BCK cycle count per audio channel. For the PCM monaural format, a 1-frame-period is a 1-sampling-cycle. For the I2S stereo format and the LR stereo format, a 1-frame -period is a half of a 1-sampling-cycle because one sampling-data consists of two channels (Left and Right). The word length specified by <WordLen[5:0]> cannot exceed this frame size.
7:6	-	0	R	Read as "0".
5:0	WordLen [5:0]	000000	R/W	Word length Specify number of the Audio data bits 100000: 32 bits 011000: 24 bits 010000: 16 bits 001000: 8 bits Others: Reserved

Note: This register should not be written continuously, when ***[I2SxCREGBUSY]*** is not "0x00000000".

4.2.5. *[I2SxCREGBUSY]* (REGBUSY Register)

Bit	Bit Symbol	After Reset	Type	Function
31:20	-	0	R	Read as "0".
19	MODESET Pend	0	R	Internal pending status of ***[I2SxCMODESET]*** register update. 0: Not busy 1: Pending
18	-	0	R	Read as "0".
17	-	0	R	Read as "0".
16	AUDIOSET Pend	0	R	Internal pending status of ***[I2SxCAUDIOSET]*** register update. 0: Not busy 1: Pending
15:4	-	0	R	Read as "0".
3	MODESET Busy	0	R	Processing status of ***[I2SxCMODESET]*** register update. 0: Not busy 1: Processing
2	-	0	R	Read as "0".
1	-	0	R	Read as "0".
0	AUDIOSET Busy	0	R	Processing status of ***[I2SxCAUDIOSET]*** register update. 0: Not busy 1: Processing

4.2.6. *[I2SxCMODESET]* (Audio Data Format Setting Register)

Bit	Bit Symbol	After Reset	Type	Function
31:3	-	0	R	Read as "0".
2:0	WS[2:0]	000	R/W	Audio signal type selection 000: I2S stereo 001: Reserved 010: LR stereo (Low period of LRCK is L channel.) 011: LR stereo (High period of LRCK is L channel.) 100: PCM monaural (Synchronized with Low of LRCK.) 101: PCM monaural (Synchronized with High of LRCK.) 110: Reserved 111: Reserved

Note: This register should not be written continuously, when the ***[I2SxCREGBUSY]*** is not "0x00000000".

4.2.7. *[I2SxCMS_SEL]* (Master / Slave Select Register)

Bit	Bit Symbol	After Reset	Type	Function
31:1	-	0	R	Read as "0".
0	SEL	1	R/W	Master / Slave selection 0: Master Output the BCK and LRCK 1: Slave Input the BCK and LRCK

Note: The PORT setting is required, refer to "Input/Output Ports" in the Reference manual.

4.2.8. *[I2SxCMCLK_IO_SEL]* (MCLK pin Input/Output select Register)

Bit	Bit Symbol	After Reset	Type	Function
31:1	-	0	R	Read as "0".
0	SEL	0	R/W	MCLK input /output selection 0: Input (MCLKI) 1: Output (MCLKO)

Note: The PORT setting is required, refer to "Input/Output Ports" in the Reference manual.

4.2.9. *[I2SxCPHT_DIV]* (ΦT0 Dividing Setting Register)

Bit	Bit Symbol	After Reset	Type	Function
31:8	-	0	R	Read as "0".
7:0	PSCAL[7:0]	0x00	R/W	ΦT0 dividing setting 0x00: Reserved 0x01: 1/2 0x02: 1/3 . . . 0xFE: 1/255 0xFF: Reserved When the ***[I2SxCPHT_DIVOUT_EN]***<EN> is "1" (clock output), don't change a set value.

Note: When the duty of 50 % is required, this bit should be set to an even division ratio.

4.2.10. *[I2SxCPHT_DIVOUT_EN]* (ΦT0 Dividing Clock Output Enable Register)

Bit	Bit Symbol	After Reset	Type	Function
31:1	-	0	R	Read as "0".
0	EN	0	R/W	Enable / Disable ΦT0 division clock output 0: Output disable 1: Output enable When using ΦT0 dividing clock as the BCK source clock, set "1" to this bit.

4.2.11. *[I2SxCBCK_SRC_SEL]* (BCK Source Clock Select Register)

Bit	Bit Symbol	After Reset	Type	Function
31:1	-	0	R	Read as "0".
0	SEL	0	R/W	Select the BCK Source 0: I2SxMCLK pin input 1: ΦT0 division clock When the ***[I2SxCBCK_DIVOUT_EN]***<EN> is "1" (clock output), don't change a set value.

4.2.12. *[I2SxCBCK_DIV]* (BCK Dividing Setting Register)

Bit	Bit Symbol	After Reset	Type	Function
31:8	-	0	R	Read as "0".
7:0	PSCAL[7:0]	0x00	R/W	Set the BCK division - ***[I2SxCBCK_SRC_SEL]***<SEL>=0: Set "0x01" to "0xFE" - ***[I2SxCBCK_SRC_SEL]***<SEL>=1: Set "0x00"

<PSCAL[7:0]> setting	*[I2SxCBCK_SRC_SEL]*	
	<SEL>=0 (I2SxMCLK pin input)	<SEL>=1 (ΦT0)
0x00	Setting prohibit	1/1
0x01	1/2	Setting prohibit
0x02	1/3	
. . .	. . .	
0xFE	1/255	
0xFF	Setting prohibit	

When the ***[I2SxCBCK_DIVOUT_EN]***<EN> is "1" (clock output), don't change a set value.

Note: When the duty of 50 % is required, this bit should be set to an even division ratio.

4.2.13. *[I2SxCBCK_DIVOUT_EN]* (BCK Output Enable Register)

Bit	Bit Symbol	After Reset	Type	Function
31:1	-	0	R	Read as "0".
0	EN	0	R/W	Enable / Disable the BCK output 0: Output disable 1: Output enable

Note: The PORT setting is required, refer to "Input/Output Ports" in the Reference manual.

4.3. Details of Reception Control Registers

4.3.1. *[I2SxISTART]* (Reception Control Start Register)

Bit	Bit Symbol	After Reset	Type	Function
31:9	-	0	R	Read as "0".
8	Start	0	R/W	Reception control operation start setting 0: Ignored 1: Start reception control operation When set to "1", reception control operation starts. When the ***[I2SxIBUSY]***<Busy> is "0", writing "1" in this bit is valid.
7:1	-	0	R	Read as "0".
0	MicStart	0	R/W	Serial transfer start setting 0: Ignored 1: Start the serial reception(input) operation When set the <MicStart> to "1", the serial transfer starts. When the ***[I2SxIBUSY]***<MicBusy> is "0", writing "1" in this bit is valid.

Note1: When restart the transfer after reception stops, set <Start> to "1", after reading ***[I2SxISTOP]*** and confirming that the stop processing is completed (***[I2SxISTOP]***<I2S_STOP> = 0).

Note2: Confirm the ***[I2SxIREGBUSY]*** register is "0x00000000", before setting "1" to the <Start>.

Note3: Continuous access to the ***[I2SxISTART]*** is prohibit. It is ignored even if it sets the ***[I2SxISTART]***.

4.3.2. *[I2SxIBUSY]* (Reception Operation Status Register)

Bit	Bit Symbol	After Reset	Type	Function
31:18	-	0	R	Read as "0".
17	LRErrBusy	0	R	Internal process status of LRCK error 0: Internal process is finished. 1: Internal process is operating.
16	ErrBusy	0	R	Internal process status of Underrun/Overrun error 0: Internal process is finished. 1: Internal process is operating.
15:9	-	0	R	Read as "0".
8	-	0	R	Read as "0".
7:2	-	0	R	Read as "0".
1	SeriBusy	0	R	Mute status 0: Mute 1: Not mute
0	MicBusy	0	R	Input operation status of SDATA(DI) 0: Stop 1: Operating

4.3.3. *[I2SxISTOP]* (Stopping Reception Data Register)

Bit	Bit Symbol	After Reset	Type	Function
31:1	-	0	R	Read as "0".
0	I2S_STOP	0	R	Internal process status of stop operation. 0: Stop operation finished 1: Stop operation processing After writing "1", this register returns "1" as a read data during processing the stop operation. This register returns "0" as a read data after completion of the stop operation.
			W	Data reception stop control 0: Ignored 1: Stop the data reception The Data reception can be stopped by writing "1" to this register and cleared the internal status execpt setting registers and error interrupt status.

Note1: This register should be written "1" during the Data reception - when ***[I2SxIBUSY]***<MicBusy> is "1".

Note2: After setting <I2S_STOP> to "1", don't set <I2S_STOP> to "1" again during the stop processing operation. When set to "1", setting is ignored.

4.3.4. *[I2SxIAUDIOSET]* (Reception AUDIOSET Register)

Bit	Bit Symbol	After Reset	Type	Function
31:17	-	0	R	Read as "0".
16	DTFmt	0	R/W	Data storage format In case of 8 or 16-bit length data: 0: Lower-first 1: Upper-first In case of 24-bit length data: 0: LSB justification 1: MSB justification Select the data alignment when reading or writing to the FIFO of 32-bits width.
15:13	-	0	R	Read as "0".
12	SDEdge	0	R/W	Sampling edge of SDATA(DI) 0: The BCK falling edge. 1: The BCK rising edge. For settings, refer to Table 3.4.
11	Edge	0	R/W	LRCK sampling edge 0: The BCK falling edge. 1: The BCK rising edge. For settings, refer to Table 3.4.
10:9	-	0	R	Read as "0".
8	SCLKtoWS	0	R/W	Frame size specification of SDATA(DI) 0: 16 cycles 1: 32 cycles A frame size means a BCK cycle count per audio channel. For the PCM monaural format, a 1-frame-period is a 1-sampling-cycle. For the I2S stereo format and the LR stereo format, a 1-frame period is a half of a 1-sampling cycle because one sampling-data consists of two channels (Left and Right). The word length specified by <WordLen[5:0]> cannot exceed this frame size.
7:6	-	0	R	Read as "0".
5:0	WordLen [5:0]	000000	R/W	Word length Set the bit count for audio data. 100000: 32 bits 011000: 24 bits 010000: 16 bits 001000: 8 bits Others: Reserved

Note: This register should not be written continuously, when ***[I2SxIREGBUSY]*** is not "0x00000000".

4.3.5. *[I2SxIINTSTAT]* (Reception Control Interrupt Source Status Register)

Bit	Bit Symbol	After Reset	Type	Function
31:4	-	0	R	Read as "0".
3	LRCKErr	0	R	LRCK Error status 0: No LRCK Error 1: LRCK Error occurred When an abnormality is detected in the LRCK cycle, this bit is set to "1". This bit shows the status before masking. Writing "1" to ***[I2SxIINTCLR]***<LRErrClr>, this bit is cleared to "0".
2	URErr	0	R	Underrun Error status 0: No Underrun Error 1: Underrun Error occurred When an Underrun error occurs, this bit is set to "1". This bit shows the status before masking. Writing "1" to ***[I2SxIINTCLR]***<URClr>, this bit is cleared to "0".
1	ORErr	0	R	Overrun Error status 0: No Overrun Error 1: Overrun Error occurred When an Overrun error occurs, this bit is set to "1". This bit shows the status before masking. Writing "1" to ***[I2SxIINTCLR]***<ORClr>, this bit is cleared to "0".
0	Int	0	R	Reception data transfer request status 0: No reception data transfer request 1: Reception data transfer request occurred This bit indicates that the FIFO has one word (4 bytes) data or more. This bit shows a status of before masking. The timing that this bit is cleared to "0" is below; - Writing "1" to the ***[I2SxIINTCLR]***<IntClr> - Receiving DMA acknowledgement when the DMAC request is enabled (***[I2SxIINTMASK]***<DMACMSK> is "0") - Overrun or Underrun occurred - Operating the stop process by the ***[I2SxISTOP]***.

4.3.6. *[I2SxIINTMASK]* (Reception Control Interrupt Mask Register)

Bit	Bit Symbol	After Reset	Type	Function
31:17	-	0	R	Read as "0".
16	DMACMSK	0	R/W	Mask selection of DMA request (Note) 0: Don't mask 1: Mask This bit masks the data request signal to the DMAC. When use the DMAC, set "0" in this bit.
15:4	-	0	R	Read as "0".
3	LRErrMask	1	R/W	Mask selection of LRCK Error 0: Don't mask 1: Mask This bit masks the LRCK Error (LRCKErr) interrupt.
2	URMask	1	R/W	Mask selection of Underrun Error 0: Don't mask 1: Mask This bit masks the Underrun Error (URErr) interrupt.
1	ORMask	1	R/W	Mask selection of Overrun Error 0: Don't mask 1: Mask This bit masks the Overrun Error (ORErr) interrupt.
0	Mask	1	R/W	Mask selection of Data transfer request interrupt(Note) 0: Don't mask 1: Mask Mask the data transfer request interrupt. This bit does not mask the data transfer request for DMAC.

Note: Data transfer request interrupt can be masked by <Mask>, and DMA request can be masked by <DMACMSK>. Mask either <Mask> or <DMACMSK>.

4.3.7. *[I2SxIINTCLR]* (Reception Control Interrupt Source Clear Register)

Bit	Bit Symbol	After Reset	Type	Function
31:4	-	0	R	Read as "0".
3	LRErrClr	0	W	Clear the LRCK Error status 0: Ignored 1: Clear The ***[I2SxIINTSTAT]***<LRCKErr> is cleared to "0" by writing "1" to this bit. Writing "0" is ignored. When read this bit, always returned "0".
2	URClr	0	W	Clear the Underrun Error status 0: Ignored 1: Clear The ***[I2SxIINTSTAT]***<URErr> is cleared to "0" by writing "1" to this bit. Writing "0" is ignored. When read this bit, always returned "0".
1	ORClr	0	W	Clear the Overrun Error status 0: Ignored 1: Clear The ***[I2SxIINTSTAT]***<ORErr> is cleared to "0" by writing "1" to this bit. Writing "0" is ignored. When read this bit, always returned "0".
0	IntClr	0	W	Clear the Data transfer request status 0: Ignored 1: Clear The ***[I2SxIINTSTAT]***<Int> is cleared to "0" by writing "1" to this bit. Writing "0" is ignored. When read this bit, always returned "0". Don't set "1" to the ***[I2SxIINTCLR]***<IntClr>, when the Data transfer request is used as the source of the DMAC request.

4.3.8. *[I2SxIMUTE]* (Reception Mute Setting Register)

Bit	Bit Symbol	After Reset	Type	Function
31:1	-	0	R	Read as "0".
0	MuteN	0	R/W	Mute setting 0: Mute ON 1: Mute OFF

Note: This register should not be written continuously, when ***[I2SxIREGBUSY]*** is not "0x00000000".

4.3.9. *[I2SxIEPTR]* (Reception Control Error Occurrence Pointer Stored Register)

Bit	Bit Symbol	After Reset	Type	Function
31:6	-	0	R	Read as "0".
5:0	ErrPointer [5:0]	000000	R	Error Pointer <ErrPointer[5:0]> is indicated the address that overrun error or underrun error occurs.

4.3.10. *[I2SxIREGBUSY]* (Reception REGBUSY Register)

Bit	Bit Symbol	After Reset	Type	Function
31:20	-	0	R	Read as "0".
19	MODESET Pend	0	R	Internal pending status of ***[I2SxIMODESET]*** register update. 0: Not busy 1: Pending
18	-	0	R	Read as "0".
17	MutePend	0	R	Internal pending status of ***[I2SxIMUTE]*** register update. 0: Not busy 1: Pending
16	AUDIOSET Pend	0	R	Internal pending status of ***[I2SxIAUDIOSET]*** register update. 0: Not busy 1: Pending
15:4	-	0	R	Read as "0".
3	MODESET Busy	0	R	Processing status of ***[I2SxIMODESET]*** register update. 0: Not busy 1: Processing
2	-	0	R	Read as "0".
1	MuteBusy	0	R	Processing status of ***[I2SxIMUTE]*** register update. 0: Not busy 1: Processing
0	AUDIOSET Busy	0	R	Processing status of ***[I2SxIAUDIOSET]*** register update. 0: Not busy 1: Processing

4.3.11. *[I2SxITHRESHOLD]* (Reception Threshold Setting Register)

Bit	Bit Symbol	After Reset	Type	Function
31:5	-	0	R	Read as "0".
4:0	threshold [4:0]	00000	R/W	Threshold value of data transfer request for the CPU or DMA. Set a value of 0 to 31. The threshold value is <threshold[4:0]>+1.

Note1: In case of the INTI2SxSI interrupt and the Reception DMA request, the FIFO needs to read ***[I2SxITHRESHOLD]***<threshold[4:0]>+1 times to generate the next interrupt.

Note2: When the I2S connects with the FIR, the result of comparing FIFO free space and <threshold[4:0]>+1 value is output.

4.3.12. *[I2SxIFIFO_STS]* (Reception FIFO Status Register)

Bit	Bit Symbol	After Reset	Type	Function
31:7	-	0	R	Read as "0".
6:0	FIFOStatus [6:0]	0x00	R	The <FIFOStatus[6:0]> indicate the FIFO data storage status when the I2S is operating.

4.3.13. *[I2SxIMODESET]* (Reception Audio Data Format Setting Register)

Bit	Bit Symbol	After Reset	Type	Function
31:3	-	0	R	Read as "0".
2:0	WS[2:0]	000	R/W	Audio data format selection 000: I2S stereo 001: Reserved 010: LR stereo (Low period of LRCK is L channel.) 011: LR stereo (High period of LRCK is L channel.) 100: PCM monaural (Synchronized with Low of LRCK.) 101: PCM monaural (Synchronized with High of LRCK.) 110: Reserved 111: Reserved

Note: This register should not be written continuously, when ***[I2SxIREGBUSY]*** is not "0x00000000".

4.3.14. *[I2SxILMEM00] to [I2SxILMEM63]* (Reception Data Register 00 to 63)

Bit	Bit Symbol	After Reset	Type	Function
31:0	SDAT[31:0]	0x00000000	R	Audio Data Refer to "3.6.1. Receive FIFO".

4.4. Details of Transmission Control Registers

4.4.1. *[I2SxOSTART]* (Transmission Control Start Register)

Bit	Bit Symbol	After Reset	Type	Function
31:9	-	0	R	Read as "0".
8	Start	0	R/W	Transmission control operation start setting 0: Ignored 1: Start transmission control operation When set to "1", transmission control operation starts. When the ***[I2SxOBUSY]***<Busy> is "0", writing "1" in this bit is valid.
7:1	-	0	R	Read as "0".
0	SpkStart	0	R/W	Serial transfer start setting 0: Ignored 1: Start the serial transmission(output) operation When set the <SpkStart> to "1", the serial transfer starts. When the ***[I2SxOBUSY]***<SpkBusy> is "0", writing "1" in this bit is valid.

Note1: When restart the transfer after transmission stops, set <Start> to "1", after reading ***[I2SxOSTOP]*** and confirming that the stop processing is completed (***[I2SxOSTOP]***<I2S_STOP> = 0).

Note2: Confirm the ***[I2SxOREGBUSY]*** register is "0x00000000", before setting "1" to the <Start> bit.

Note3: Continuous access to the ***[I2SxOSTART]*** is prohibit. It is ignored even if it sets the ***[I2SxOSTART]***.

4.4.2. *[I2SxOBUSY]* (Transmission Operation Status Register)

Bit	Bit Symbol	After Reset	Type	Function
31:18	-	0	R	Read as "0".
17	LRErrBusy	0	R	Internal process status of LRCK error 0: Internal process is finished. 1: Internal process is operating.
16	ErrBusy	0	R	Internal process status of Underrun/Overrun error 0: Internal process is finished. 1: Internal process is operating.
15:9	-	0	R	Read as "0".
8	-	0	R	Read as "0".
7:2	-	0	R	Read as "0".
1	SeriBusy	0	R	Mute status 0: Mute 1: Not Mute
0	SpkBusy	0	R	Output operation status of SDATA(DO) 0: Stop 1: Operating

4.4.3. *[I2SxOSTOP]* (Stopping Transmission Data Register)

Bit	Bit Symbol	After Reset	Type	Function
31:1	-	0	R	Read as "0".
0	I2S_STOP	0	R	Internal process status of stop operation. 0: Stop operation finished 1: Stop operation processing After writing "1", this register returns "1" as a read data during processing the stop operation. This register returns "0" as a read data after completion of the stop operation.
			W	Data transmission stop control 0: Ignored 1: Stop the data transmission The Data transmission can be stopped by writing "1" to this register and cleared the internal status execpt setting registers and error interrupt status.

Note1: This register should be written "1" during the Data transmission - when ***[I2SxOBUSY]***<SpkBusy> is "1".

Note2: After setting <I2S_STOP> to "1", don't set <I2S_STOP> to "1" again during the stop processing operation. When set to "1", setting is ignored.

4.4.4. *[I2SxOAUDIOSET]* (Transmission AUDIOSET Register)

Bit	Bit Symbol	After Reset	Type	Function
31:17	-	0	R	Read as "0".
16	DTFmt	0	R/W	Data storage format In case of 8 or 16-bit length data: 0: Lower-first 1: Upper-first In case of 24-bit length data: 0: LSB justification 1: MSB justification Select the data alignment when reading or writing to the FIFO of 32-bits width.
15:13	-	0	R	Read as "0".
12	SDEdge	0	R/W	Sampling edge of SDATA(DO) 0: The BCK falling edge. 1: The BCK rising edge. For settings, refer to Table 3.4.
11	Edge	0	R/W	LRCK sampling edge 0: The BCK falling edge 1: The BCK rising edge For settings, refer to Table 3.4.
10:9	-	0	R	Read as "0".
8	SCLKtoWS	0	R/W	Specify the frame size of SDATA(DO). 0: 16 cycles 1: 32 cycles A frame size means a BCK cycle count per audio channel. For the PCM monaural format, a 1-frame-period is a 1-sampling-cycle. For the I2S stereo format and the LR stereo format, a 1-frame-period is a half of a 1-sampling-cycle because one sampling-data consists of two channels (Left and Right). The word length specified by <WordLen[5:0]> cannot exceed this frame size.
7:6	-	0	R	Read as "0".
5:0	WordLen [5:0]	000000	R/W	Word length Set the bit count for audio data. 100000: 32 bits 011000: 24 bits 010000: 16 bits 001000: 8 bits others: Reserved

Note: This register should not be written continuously, when ***[I2SxOREGBUSY]*** is not "0x00000000".

4.4.5. *[I2SxOINTSTAT]* (Transmission Control Interrupt Source Status Register)

Bit	Bit Symbol	After Reset	Type	Function
31:4	-	0	R	Read as "0".
3	LRCKErr	0	R	LRCK Error status 0: No LRCK Error 1: LRCK Error occurred When an abnormality is detected in the LRCK cycle, this bit is set to "1". This bit shows the status before masking. Writing "1" to ***[I2SxOINTCLR]***<LRErrClr>, this bit is cleared to "0".
2	URErr	0	R	Underrun Error status 0: No Underrun Error 1: Underrun Error occurred When an Underrun error occurs, this bit is set to "1". This bit shows the status before masking. Writing "1" to ***[I2SxOINTCLR]***<URClr>, this bit is cleared to "0".
1	ORErr	0	R	Overrun Error status 0: No Overrun Error 1: Overrun Error occurred When an Overrun error occurs, this bit is set to "1". This bit shows the status before masking. Writing "1" to ***[I2SxOINTCLR]***<ORClr>, this bit is cleared to "0".
0	Int	0	R	Transmission data transfer request status 0: No transmission data transfer request 1: Transmission data transfer request occurred This bit indicates that the FIFO free space is one word (4 bytes) data or more. This bit shows a status of before masking. The timing that this bit is cleared to "0" is below; - Writing "1" to the ***[I2SxOINTCLR]***<IntClr> - Receiving DMA acknowledgement when the DMAC request is enabled (***[I2SxOINTMASK]***<DMACMSK> is "0") - Overrun or Underrun occurred - Operating the stop process by the ***[I2SxOSTOP]***.

4.4.6. *[I2SxOINTMASK]* (Transmission Control Interrupt Mask Register)

Bit	Bit Symbol	After Reset	Type	Function
31:17	-	0	R	Read as "0".
16	DMACMSK	0	R/W	Mask selection of DMA request (Note) 0: Don't mask 1: Mask This bit masks the data request signal to the DMAC. When use the DMAC, set "0" in this bit.
15:4	-	0	R	Read as "0".
3	LRErrMask	1	R/W	Mask selection of LRCK Error 0: Don't mask 1: Mask This bit masks the LRCK Error (LRCKErr) interrupt.
2	URMask	1	R/W	Mask selection of Underrun Error 0: Don't mask 1: Mask This bit masks the Underrun Error (URErr) interrupt.
1	ORMask	1	R/W	Mask selection of Overrun Error 0: Don't mask 1: Mask This bit masks the Overrun Error (ORErr) interrupt.
0	Mask	1	R/W	Mask selection of Data transfer request interrupt(Note) 0: Don't mask 1: Mask Mask the data transfer request interrupt. This bit does not mask the data transfer request for DMAC.

Note: Data transfer request interrupt can be masked by <Mask>, and DMA request can be masked by <DMACMSK>. Mask either <Mask> or <DMACMSK>.

4.4.7. *[I2SxOINTCLR]* (Transmission Control Interrupt Source Clear Register)

Bit	Bit Symbol	After Reset	Type	Function
31:4	-	0	R	Read as "0".
3	LRErrClr	0	W	Clear the LRCK Error status 0: Ignored 1: Clear The ***[I2SxOINTSTAT]***<LRCKErr> is cleared to "0" by writing "1" to this bit. Writing "0" is ignored. When read this bit, always returned "0".
2	URClr	0	W	Clear the Underrun Error status 0: Ignored 1: Clear The ***[I2SxOINTSTAT]***<URErr> is cleared to "0" by writing "1" to this bit. Writing "0" is ignored. When read this bit, always returned "0".
1	ORClr	0	W	Clear the Overrun Error status 0: Ignored 1: Clear The ***[I2SxOINTSTAT]***<ORErr> is cleared to "0" by writing "1" to this bit. Writing "0" is ignored. When read this bit, always returned "0".
0	IntClr	0	W	Clear the Data transfer request status 0: Ignored 1: Clear The ***[I2SxOINTSTAT]***<Int> is cleared to "0" by writing "1" to this bit. Writing "0" is ignored. When read this bit, always returned "0". Don't set "1" to the ***[I2SxOINTCLR]***<IntClr>, when the Data transfer request is used as the source of the DMAC request.

4.4.8. *[I2SxOMUTE]* (Transmission Mute Setting Register)

Bit	Bit Symbol	After Reset	Type	Function
31:1	-	0	R	Read as "0".
0	MuteN	0	R/W	Mute setting 0: Mute ON 1: Mute OFF

Note: This register should not be written continuously, when ***[I2SxOREGBUSY]*** is not "0x00000000".

4.4.9. *[I2SxOEPTR]* (Transmission Control Error Occurrence Pointer Stored Register)

Bit	Bit Symbol	After Reset	Type	Function
31:6	-	0	R	Read as "0".
5:0	ErrPointer [5:0]	000000	R	Error Pointer <ErrPointer[5:0]> is indicated the address that overrun error or underrun error occurs.

4.4.10. *[I2SxOTX_SSIZE]* (TX_SSIZE Register)

Bit	Bit Symbol	After Reset	Type	Function
31:6	-	0	R	Read as "0".
5:0	TxStartSize [5:0]	0x20	R/W	Specifying the transmission starting threshold of the SDATA. Specify the data amount as the word count. (one word is 4 bytes) Initial value is 0x20 (32 words). The value of 4 to 63 is available, the value of 0 to 3 is not available.

Note1: A serial data transmission starts when the data over the specified value is stored in the buffer. This threshold has an effect on only the first data after writing "1" to ***[I2SxOSTART]***<SpkStart>

Note2: This register should not be written continuously, when ***[I2SxOREGBUSY]*** is not "0x00000000".

4.4.11. *[I2SxOREGBUSY]* (Transmission REGBUSY Register)

Bit	Bit Symbol	After Reset	Type	Function
31:20	-	0	R	Read as "0".
19	MODESET Pend	0	R	Internal pending status of ***[I2SxOMODESET]*** register update. 0: Not busy 1: Pending
18	TXSSize Pend	0	R	Internal pending status of ***[I2SxOTX_SSIZE]*** register update. 0: Not busy 1: Pending
17	Mute Pend	0	R	Internal pending status of ***[I2SxOMUTE]*** register update. 0: Not busy 1: Pending
16	AUDIOSET Pend	0	R	Internal pending status of ***[I2SxOAUDIOSET]*** register update. 0: Not busy 1: Pending
15:4	-	0	R	Read as "0".
3	MODESET Busy	0	R	Processing status of ***[I2SxOMODESET]*** register update. 0: Not busy 1: Processing
2	TXSSize Busy	0	R	Processing status of ***[I2SxOTX_SSIZE]*** register update. 0: Not busy 1: Processing
1	MuteBusy	0	R	Processing status of ***[I2SxOMUTE]*** register update. 0: Not busy 1: Processing
0	AUDIOSET Busy	0	R	Processing status of ***[I2SxOAUDIOSET]*** register update. 0: Not busy 1: Processing

Note: Check that the ***[I2SxOREGBUSY]*** register is "0x00000000", before the ***[I2SxOSTART]***<Start> is set to "1".

4.4.12. *[I2SxOTHRESHOLD]* (Transmission Threshold Setting Register)

Bit	Bit Symbol	After Reset	Type	Function
31:5	-	0	R	Read as "0".
4:0	threshold [4:0]	00000	R/W	Threshold value of data transfer request for the CPU or DMA. Set a value of 0 to 31. The threshold value is <threshold[4:0]>+1.

Note1: In case of the INTI2SxSO interrupt and the Transmission DMA request, the FIFO needs to write ***[I2SxOTHRESHOLD]***<threshold[4:0]>+1 times to generate the next interrupt.

Note2: When the I2S connects with the FIR, the result of comparing FIFO free space and <threshold[4:0]>+1 value is output.

4.4.13. *[I2SxOFIFO_STS]* (Transmission FIFO Status Register)

Bit	Bit Symbol	After Reset	Type	Function
31:7	-	0	R	Read as "0".
6:0	FIFOStatus [6:0]	0x40	R	The <FIFOStatus[6:0]> indicate the FIFO data storage status when the I2S is operating.

4.4.14. *[I2SxOMODESET]* (Transmission Audio Data Format Setting Register)

Bit	Bit Symbol	After Reset	Type	Function
31:3	-	0	R	Read as "0".
2:0	WS[2:0]	000	R/W	Audio data format selection 000: I2S stereo 001: Reserved 010: LR stereo (Low period of LRCK is L channel.) 011: LR stereo (High period of LRCK is L channel.) 100: PCM monaural (Synchronized with Low of LRCK.) 101: PCM monaural (Synchronized with High of LRCK.) 110: Reserved 111: Reserved

Note: This register should not be written continuously, when ***[I2SxOREGBUSY]*** is not "0x00000000".

4.4.15. *[I2SxOLMEM00] to [I2SxOLMEM63]* (Transmission Data Register 00 to 63)

Bit	Bit Symbol	After Reset	Type	Function
31:0	SDAT[31:0]	0x00000000	W	Audio data Refer to "3.6.2. Transmit FIFO".

5. Example of Use

5.1. Operation Process

Once an error occurs, the transmission or the reception cannot continue. When an error occurs, the process in "5.1.4.1. Overrun Error or Underrun Error Interrupt Occurrence" should be done. Then the transmission or the reception should be restarted.
When the underrun is generated intentionally, the process in "5.1.4.1. Overrun Error or Underrun Error Interrupt Occurrence" and "5.1.5. Operation Process of Reception Restart or Transmission Restart" should be done to restart the transmission or the reception.
After ***[I2SxOSTART]*** <Start> is set to "1", the interrupt of the notification of the FIFO's empty state and the DMA request are issued.

5.1.1. Operation Process of LRCK Generation Start

1. Master/Slave setting
   The operation of the I2Sx device (Master or Slave) should be set to ***[I2SxCMS_SEL]***<SEL>.
2. Port setting
   The port function should be set according to necessary function.
   For the details of the port setting, refer to "Input/Output Ports" in the Reference manual.
3. Frequency setting
   The setting of the MCLK input or output should be done in ***[I2SxCMCLK_IO_SEL]***<SEL>. If necessary, the frequency of the MCKO (External master clock output) and the source clock of the BCK should be set in ***[I2SxCPHT_DIV]***<PSCAL[7:0]> and ***[I2SxCPHT_DIVOUT_EN]***<EN>, respectively.
   For a master device, the BCK frequency should be set in ***[I2SxCBCK_SRC_SEL]***<SEL>, ***[I2SxCBCK_DIV]***<PSCAL[7:0]>, and ***[I2SxCBCK_DIVOUT_EN]***<EN>.
4. DMAC start-up (for DMA transfer)
   When the DMAC is used, the DMAC should be started up. For the detail settings of the DMAC, refer to "Multi-function DMA Controller" in the Reference manual.
5. Frame size of the clock control, Word length, and Clock edge setting (only for Master)
   The frame size should be set in ***[I2SxCAUDIOSET]***<SCLKtoWS> and ***[I2SxCAUDIOSET]***<WordLen[5:0]>. The clock edge should be set in ***[I2SxCAUDIOSET]***<Edge>.
6. Setting of the audio format of the clock control (only for Master)
   The audio format should be set in ***[I2SxCMODESET]***<WS[2:0]>.
7. Setting of LRCK generation start (only for Master)
   [I2SxCREGBUSY] = 0x00000000 should be checked. Then, ***[I2SxCSTART]***<Start> should be set to "1" to start generating the LRCK.

[I2SxCAUDIOSET] and ***[I2SxCMODESET]*** should not be written continuously. If a continuous access is done, ***[I2SxCSTART]***<Start> should not be written to "1" until ***[I2SxCREGBUSY]*** becomes "0x00000000".

Table 5.1 Registers set of LRCK generation start

Step	Setting item	Setting registers	Description
1	Master/Slave setting	***[I2SxCMS_SEL]***<SEL>	-
2	Port setting	Refer to "Input/Output Ports" in the Reference Manual.	
3	Frequency setting	***[I2SxCMCLK_IO_SEL]***<SEL>	MCLK input or output setting
		[I2SxCPHT_DIV]<PSCAL[7:0]> ***[I2SxCPHT_DIVOUT_EN]***<EN>	Setting of the frequency of MCKO (External master clock output) and setting of the source clock of BCK
		[I2SxCBCK_SRC_SEL]<SEL> ***[I2SxCBCK_DIV]***<PSCAL[7:0]> ***[I2SxCBCK_DIVOUT_EN]***<EN>	BCK frequency setting (BCK setting is necessary only for Master.)
4	DMAC start-up	Refer to "Multi-function DMA Controller" in the Reference manual.	
5	Frame size and Word length setting Clock edge setting	***[I2SxCAUDIOSET]***<SCLKtoWS> ***[I2SxCAUDIOSET]***<WordLen[5:0]> ***[I2SxCAUDIOSET]***<Edge>	Only for Master
6	Audio format selection	***[I2SxCMODESET]***<WS[2:0]>	Only for Master
7	LRCK generation start	***[I2SxCREGBUSY]*** ***[I2SxCSTART]***<Start>	Only for Master

5.1.2. Operation Process of Reception Start

1. Audio format setting of Reception control (Note)
   The audio format should be set in ***[I2SxIMODESET]***<WS[2:0]>.

2. Frame size, Word length, Clock edge, and Data storage format settings in Reception control (only for Master) (Note)
   The settings should be done for the frame size in ***[I2SxIAUDIOSET]***<SCLKtoWS> and ***[I2SxIAUDIOSET]***<WordLen[5:0]>, and for the clock edge in ***[I2SxIAUDIOSET]***<Edge> and ***[I2SxIAUDIOSET]***<SDEdge>. The data storage format should be set in ***[I2SxIAUDIOSET]***<DTFmt>.

3. Interrupt setting (Settings of Data transfer threshold value and Interrupt mask disable)
   The data transfer request threshold value should be set to ***[I2SxITHRESHOLD]***<threshold[4:0]>.
   When an interrupt source is unmasked, the corresponding bit of the ***[I2SxIINTMASK]*** register should be set to "0".

4. Operation start of Reception control block
   [I2SxIREGBUSY] = 0x00000000 should be checked. Then, ***[I2SxISTART]***<Start> should be set to "1" to start operating the reception control block.

5. Serial transfer start
   [I2SxIMUTE]<MuteN> = 1 should be set to switch the mute OFF.
   [I2SxISTART]<MicStart> = 1 should be set to start the serial transfer operation.

Note: When each bit in ***[I2SxIREGBUSY]*** is "1", ***[I2SxIAUDIOSET]***, ***[I2SxIMODESET]***, and ***[I2SxIMUTE]*** should not be written continuously.

Table 5.2 Registers set of Reception start

Step	Setting item	Setting registers	Description
1	Audio format selection	***[I2SxIMODESET]***<WS[2:0]>	-
2	Settings of Data storage format, Clock edge, Frame size, and Word length	***[I2SxIAUDIOSET]***<DTFmt> ***[I2SxIAUDIOSET]***<SDEdge> ***[I2SxIAUDIOSET]***<Edge> ***[I2SxIAUDIOSET]***<SCLKtoWS> ***[I2SxIAUDIOSET]***<WordLen[5:0]>	-
3	Interrupt setting (Setting of Data transfer request threshold value)	***[I2SxITHRESHOLD]***<threshold[4:0]>	-
	Interrupt setting (Interrupt mask disable)	***[I2SxIINTMASK]***<DMACMSK> ***[I2SxIINTMASK]***<LRErrMask> ***[I2SxIINTMASK]***<URMask> ***[I2SxIINTMASK]***<ORMask> ***[I2SxIINTMASK]***<Mask>	"0" should be set for unmasked interrupts. ("1" for a masked factor and "0" for an unmasked factor)
4	Operation start of Reception control block	***[I2SxISTART]***<Start>	-
5	Serial transfer start	***[I2SxIMUTE]***<MuteN>	Mute OFF setting
		[I2SxISTART]<MicStart>	-

5.1.3. Operation Process of Transmission Start

1. Audio format setting of Transmission control
   The audio format should be set in ***[I2SxOMODESET]***<WS[2:0]>.

2. Frame size, Word length, Clock edge, and data storage format settings in Transmission control (only for Master)
   The frame size should be set in ***[I2SxOAUDIOSET]***<SCLKtoWS> and ***[I2SxOAUDIOSET]***<WordLen[5:0]>. The clock edge should be set in ***[I2SxOAUDIOSET]***<Edge> and ***[I2SxOAUDIOSET]***<SDEdge>. The data storage format should be set in ***[I2SxOAUDIOSET]***<DTFmt>.

3. Setting of Transmission start threshold value
   The size of data stored in the FIFO should be set in ***[I2SxOTX_SSIZE]***<TxStartSize[5:0]>.

4. Interrupt setting (Settings of Data transfer request threshold value and Interrupt mask disable)
   The data transfer request threshold value should be set to ***[I2SxOTHRESHOLD]***<threshold[4:0]>.
   When an interrupt source is unmasked, the corresponding bit of the ***[I2SxOINTMASK]*** register should be set to "0".

5. Operation start of Transmission control block
   [I2SxOREGBUSY] = 0x00000000 should be checked. Then, ***[I2SxOSTART]***<Start> = 1 should be set to start operating the Transmission control block.

6. Serial transfer start
   [I2SxOMUTE]<MuteN> = 1 should be set to switch the mute OFF.
   [I2SxOSTART]<SpkStart> = 1 should be set to start the serial transfer operation.

   Note: When each bit in ***[I2SxOREGBUSY]*** is "1", ***[I2SxOAUDIOSET]***, ***[I2SxOMODESET]***, ***[I2SxOMUTE]***, and ***[I2SxOTX_SSIZE]*** should not be written continuously.

Table 5.3 Registers set of Transmission start

Step	Setting item	Setting registers	Description
1	Audio format selection	***[I2SxOMODESET]***<WS[2:0]>	-
2	Settings of Data storage format, Clock edge, Frame size, and Word length	***[I2SxOAUDIOSET]***<DTFmt> ***[I2SxOAUDIOSET]***<SDEdge> ***[I2SxOAUDIOSET]***<Edge> ***[I2SxOAUDIOSET]***<SCLKtoWS> ***[I2SxOAUDIOSET]***<WordLen[5:0]>	-
3	Setting of Transmission start threshold value	***[I2SxOTX_SSIZE]***<TxStartSize[5:0]>	-
4	Interrupt setting (Setting of Data transfer request threshold value)	***[I2SxOTHRESHOLD]***<threshold[4:0]>	-
	Interrupt setting (Interrupt mask disable)	***[I2SxOINTMASK]***<DMACMSK> ***[I2SxOINTMASK]***<LRErrMask> ***[I2SxOINTMASK]***<URMask> ***[I2SxOINTMASK]***<ORMask> ***[I2SxOINTMASK]***<Mask>	"0" should be set for unmasked interrupts. ("1" for a masked factor and "0" for an unmasked factor)
5	Operation start of Transmission control block	***[I2SxOSTART]***<Start> (Note)	-
6	Serial transfer start	***[I2SxOMUTE]***<MuteN>	Mute OFF setting
		[I2SxOSTART]<SpkStart>	-

Note: After "1" is set, the interrupt of the notification of the FIFO's empty state and the DMA request are issued.

5.1.4. Operation Process of Reception Stop and Transmission Stop

When the reception stop or the transmission stop is done, both a master device and a slave device are necessary to be supplied of the serial clock during the process of the data reception stop or data transmission stop (until ***[I2SxISTOP]*** <I2S_STOP> and ***[I2SxOSTOP]*** <I2S_STOP> are read as "0").

5.1.4.1. Overrun Error or Underrun Error Interrupt Occurrence

1. Interrupt mask
   All corresponding interrupts should be masked using the ***[I2SxIINTMASK]*** or ***[I2SxOINTMASK]*** register.

2. Check of completion of Overrun or Underrun process
   Check that ***[I2SxIBUSY]***<ErrBusy> or ***[I2SxOBUSY]***<ErrBusy> is "0".

3. Setting of Mute ON
   The mute should be ON by setting "0" to ***[I2SxIMUTE]***<MuteN> or ***[I2SxOMUTE]***<MuteN>.
   Check that ***[I2SxISTART]***<SeriBusy> or ***[I2SxOSTART]***<SeriBusy> becomes "0" to confirm the setting of the <MuteN> is valid internally.

4. Data transfer stop
   When ***[I2SxISTOP]***<I2S_STOP> or ***[I2SxOSTOP]***<I2S_STOP> is set to "1", the stop process starts.
   Check that ***[I2SxISTOP]***<I2S_STOP> or ***[I2SxOSTOP]***<I2S_STOP> becomes "0" to confirm the stop process of the data transfer has completed.

5. Check of LRCK generation operation (Unnecessary when the LRCK does not stop.)
   Check that ***[I2SxCBUSY]***<Busy> is "1" (Under operation of the generation).

6. LRCK generation stop (Unnecessary when the LRCK does not stop.)
   [I2SxCSTOP]<I2S_STOP> should be set to "1". Wait until ***[I2SxCSTOP]***<I2S_STOP> becomes "0".

7. Release of Error interrupt
   The factor bit of the error interrupt should be set to "1" in the ***[I2SxIINTCLR]*** or ***[I2SxOINTCLR]*** register.

Table 5.4 Setting registers for Reception stop or Transmission stop at occurrence of Overrun error or Underrun error interrupts

Step	Setting item	Reception	Transmission
1	Interrupt mask	***[I2SxIINTMASK]*** <DMACMSK>, <LRErrMask>, <URMask>, <ORMask>, <Mask>	***[I2SxOINTMASK]*** <DMACMSK>, <LRErrMask>, <URMask>, <ORMask>, <Mask>
2	Check of completion of internal process at occurrence of Overrun error or Underrun error	***[I2SxIBUSY]***<ErrBusy>	***[I2SxOBUSY]***<ErrBusy>
3	Setting of Mute ON	***[I2SxIMUTE]***<MuteN>	***[I2SxOMUTE]***<MuteN>
	Wait until the state of <MuteN> becomes valid internally	***[I2SxIBUSY]***<SeriBusy>	***[I2SxOBUSY]***<SeriBusy>
4	Setting of Data reception stop or Data transmission stop	Write ***[I2SxISTOP]***<I2S_STOP>	Write ***[I2SxOSTOP]***<I2S_STOP>
	Wait for process of Data reception stop or Data transmission stop	Read ***[I2SxISTOP]***<I2S_STOP>	Read ***[I2SxOSTOP]***<I2S_STOP>
5	Check of LRCK generation operation	***[I2SxCBUSY]***<Busy>	***[I2SxCBUSY]***<Busy>
6	LRCK stop	Write ***[I2SxCSTOP]***<I2S_STOP>	Write ***[I2SxCSTOP]***<I2S_STOP>
	Wait for completion of LRCK stop process	Read ***[I2SxCSTOP]***<I2S_STOP>	Read ***[I2SxCSTOP]***<I2S_STOP>
7	Clear of Interrupt factor	***[I2SxIINTCLR]***<URClr> ***[I2SxIINTCLR]***<ORClr>>	***[I2SxOINTCLR]***<URClr> ***[I2SxOINTCLR]***<ORClr>

5.1.4.2. LRCK Error Interrupt Occurrence

1. Interrupt mask
   All corresponding interrupts should be masked using the ***[I2SxIINTMASK]*** or ***[I2SxOINTMASK]*** register.

2. Check of completion of LRCK error process
   Check that ***[I2SxIBUSY]***<LRErrBusy> or ***[I2SxOBUSY]***<LRErrBusy> is "0".

3. Data transfer stop
   When ***[I2SxISTOP]***<I2S_STOP> or ***[I2SxOSTOP]***<I2S_STOP> is set to "1", the stop process starts.
   Check that ***[I2SxISTOP]***<I2S_STOP> or ***[I2SxOSTOP]***<I2S_STOP> becomes "0" to confirm the stop process of the data transfer has completed.

4. Check of LRCK generation operation (Unnecessary when the LRCK does not stop.)
   Check that ***[I2SxCBUSY]***<Busy> is "1" (Under operation of the generation).

5. LRCK generation stop (Unnecessary when the LRCK does not stop.)
   [I2SxCSTOP]<I2S_STOP> should be set to "1". Wait until ***[I2SxCSTOP]***<I2S_STOP> becomes "0".

6. Release of Error interrupt
   The factor bit of the error interrupt should be set to "1" in the ***[I2SxIINTCLR]*** or ***[I2SxOINTCLR]*** register.

Table 5.5 Setting registers for Reception stop or Transmission stop at occurrence of LRCK error interrupt

Step	Setting item	Reception	Transmission
1	Interrupt mask	***[I2SxIINTMASK]*** <DMACMSK>, <LRErrMask>, <URMask>, <ORMask>, <Mask>	***[I2SxOINTMASK]*** <DMACMSK>, <LRErrMask>, <URMask>, <ORMask>, <Mask>
2	Check of completion of internal process at occurrence of LRCK error	***[I2SxIBUSY]***<LRErrBusy>	***[I2SxOBUSY]***<LRErrBusy>
3	Setting of Data reception stop or Data transmission stop	Write ***[I2SxISTOP]***<I2S_STOP>	Write ***[I2SxOSTOP]***<I2S_STOP>
	Wait for process of Data reception stop or Data transmission stop	Read ***[I2SxISTOP]***<I2S_STOP>	Read ***[I2SxOSTOP]***<I2S_STOP>
4	Check of LRCK generation operation	***[I2SxCBUSY]***<Busy>	***[I2SxCBUSY]***<Busy>
5	LRCK stop	Write ***[I2SxCSTOP]***<I2S_STOP>	Write ***[I2SxCSTOP]***<I2S_STOP>
	Wait for completion of LRCK stop process	Read ***[I2SxCSTOP]***<I2S_STOP>	Read ***[I2SxCSTOP]***<I2S_STOP>
6	Clear of Interrupt factor	***[I2SxIINTCLR]***<LRErrClr>	***[I2SxOINTCLR]***<LRErrClr>

5.1.4.3. Except Error Interrupt Occurrence

1. Check of the data transfer state
   Check that ***[I2SxIBUSY]***<MicBusy> and ***[I2SxOBUSY]***<SpkBusy> are "1".
   This check is unnecessary when the operation state is obvious because enough time elapses after the start-up.

2. Setting of Mute ON
   The mute should be ON by setting "0" to ***[I2SxIMUTE]***<MuteN> or ***[I2SxOMUTE]***<MuteN>.
   Check that ***[I2SxISTART]***<SeriBusy> or ***[I2SxOSTART]***<SeriBusy> becomes "0" to confirm the setting of the <MuteN> is valid internally.

3. Data transfer stop
   When ***[I2SxISTOP]***<I2S_STOP> or ***[I2SxOSTOP]***<I2S_STOP> is set to "1", the stop process starts.
   Check that ***[I2SxISTOP]***<I2S_STOP> or ***[I2SxOSTOP]***<I2S_STOP> becomes "0" to confirm the stop process of the data transfer has completed.

4. LRCK generation stop (Unnecessary when the LRCK does not stop.)
   [I2SxCSTOP]<I2S_STOP> should be set to "1". Wait until ***[I2SxCSTOP]***<I2S_STOP> becomes "0".

Table 5.6 Setting registers for Reception stop or Transmission stop except error interrupt occurrence

Step	Setting item	Reception	Transmission
1	Check of the data transfer state	***[I2SxIBUSY]***<MicBusy>	***[I2SxOBUSY]***<SpkBusy>
2	Setting of Mute ON	***[I2SxIMUTE]***<MuteN>	***[I2SxOMUTE]***<MuteN>
	Wait until the state set in <MuteN> becomes valid internally	***[I2SxIBUSY]***<SeriBusy>	***[I2SxOBUSY]***<SeriBusy>
3	Setting of Data reception stop or Data transmission stop	Write ***[I2SxISTOP]***<I2S_STOP>	Write ***[I2SxOSTOP]***<I2S_STOP>
	Wait for process of Data reception stop or Data transmission stop	Read ***[I2SxISTOP]***<I2S_STOP>	Read ***[I2SxOSTOP]***<I2S_STOP>
4	LRCK stop	Write ***[I2SxCSTOP]***<I2S_STOP>	Write ***[I2SxCSTOP]***<I2S_STOP>
	Wait for completion of LRCK stop process	Read ***[I2SxCSTOP]***<I2S_STOP>	Read ***[I2SxCSTOP]***<I2S_STOP>

5.1.5. Operation Process of Reception Restart or Transmission Restart

When reception or transmission should be restarted after it stops, Step 4 and after in "5.1.1. Operation Process of LRCK Generation Start", and the process in "5.1.2. Operation Process of Reception Start" or "5.1.3. Operation Process of Transmission Start" should be done. Before <Start> is set to "1" at the reception restart or the transmission restart, <I2S_STOP> should be read to confirm that the stop process has completed.

- After ***[I2SxCSTOP]***<I2S_STOP> = 1 is set, ***[I2SxCSTOP]***<I2S_STOP> is read as "1" during the stop process. ***[I2SxCSTART]***<Start> = 1 should be set after checking ***[I2SxCSTOP]***<I2S_STOP> = 0.
- After ***[I2SxISTOP]***<I2S_STOP> = 1 is set, ***[I2SxISTOP]***<I2S_STOP> is read as "1" during the stop process. ***[I2SxISTART]***<Start>=1 should be set after checking ***[I2SxISTOP]***<I2S_STOP> = 0.
- After ***[I2SxOSTOP]***<I2S_STOP> = 1 is set, ***[I2SxOSTOP]***<I2S_STOP> is read as "1" during the stop process. ***[I2SxOSTART]***<Start> = 1 should be set after checking ***[I2SxOSTOP]***<I2S_STOP> = 0.

5.1.6. Stop Process

"5.1.4. Operation Process of Reception Stop and Transmission Stop" should be done.

5.2. Example of CPU Transfer Flow

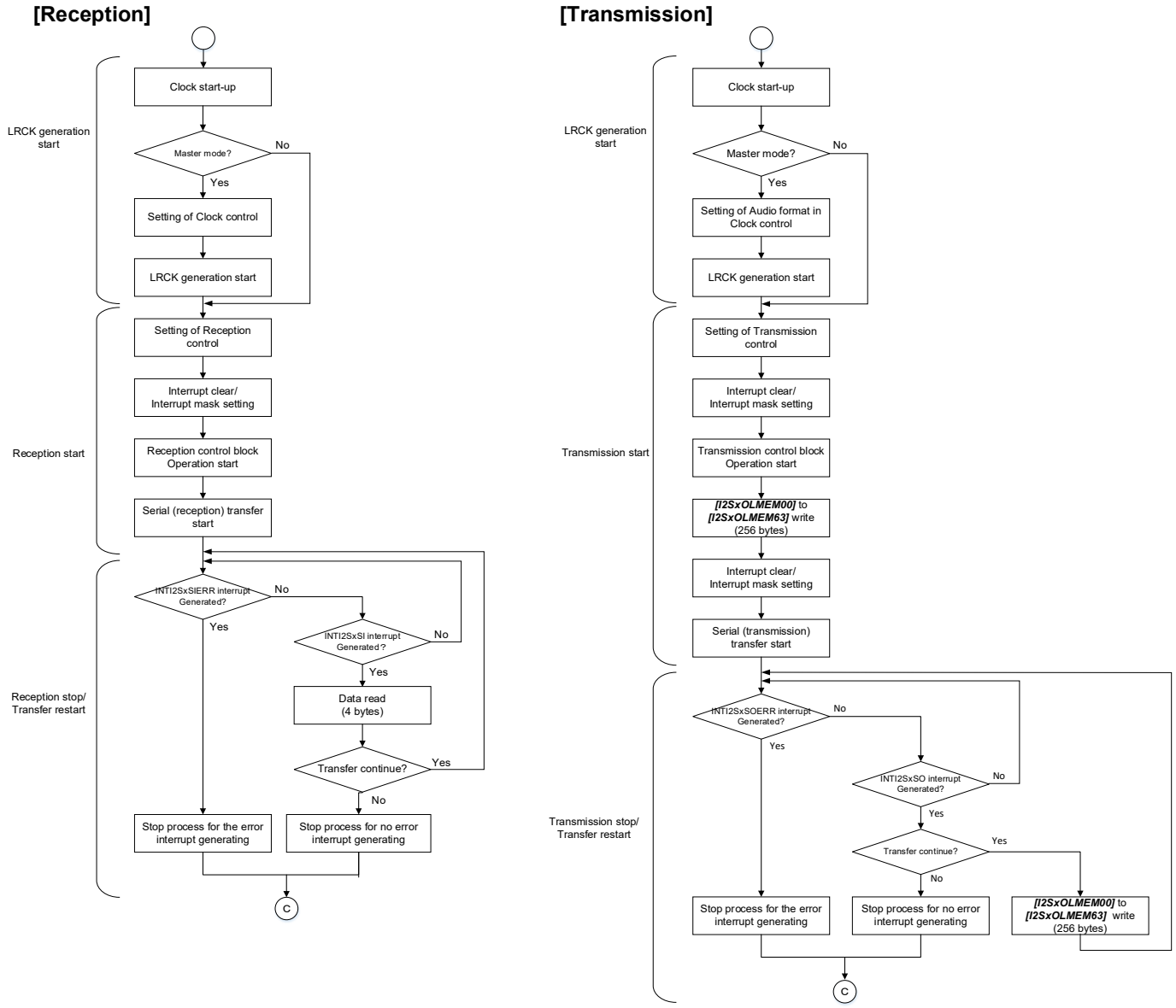


Figure 5.1 Example of CPU transfer flow

5.3. Example of DMA Transfer Flow

Figure 5.2 Example of DMA transfer flow

6. Precaution for Use

- The addresses to which no registers are assigned should not be accessed.

- When reception stop or transmission stop is done, both a master device and a slave device are necessary to be supplied of the serial clock during the process of the data reception stop or data transmission stop (until ***[I2SxISTOP]*** <I2S_STOP> or ***[I2SxOSTOP]*** <I2S_STOP> is read as "0").

- The successive accesses to the following registers are inhibited.

  [I2SxIAUDIOSET] / ***[I2SxOAUDIOSET]***, ***[I2SxIMODESET]*** / ***[I2SxOMODESET]***, ***[I2SxIMUTE]*** / ***[I2SxOMUTE]***, and ***[I2SxOTX_SSIZE]*** registers should not be written successively when the corresponding bit in each register access state is "1" in the ***[I2SxIREGBUSY]*** / ***[I2SxOREGBUSY]*** registers.

  Before ***[I2SxISTART]***<Start> or ***[I2SxOSTART]***<Start> is set to "1", check that the ***[I2SxIREGBUSY]*** or the ***[I2SxOREGBUSY]*** register is "0x00000000".

- The receive FIFO or the transmit FIFO should be accessed after ***[I2SxISTART]***<Start> or ***[I2SxOSTART]***<Start> is set to "1".

7. Revision History

Table 7.1 Revision History

Revision	Date	Description
1.0	2020-11-16	First release

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