32-Bit RISC Microcontroller

TXZ+ Family
TMPM4G Group (1)

Reference Manual
Product Information
(PINFO-M4G(1))

Revision 1.2

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Conventions

- Numeric formats follow the rules as shown below:
  Hexadecimal: 0xABC
  Decimal: 123 or 0d123 - Only when it needs to be explicitly shown that they are decimal numbers.
  Binary: 0b111 - It is possible to omit the "0b" when the number of bits can be distinctly understood from a sentence.
- "_N" is added to the end of signal names to indicate low active signals.
- It is called "assert" that a signal moves to its active level, "deassert" to its inactive level.
- When two or more signal names are referred, they are described like as [m:n].
  Example: S[3:0] shows four signal names S3, S2, S1 and S0 together.
- The characters surrounded by ***[ ]*** defines the register.
  Example: ***[ABCD]***
- "N" substitutes suffix number of two or more same kind of registers, fields, and bit names.
  Example: ***[XYZ1]***, ***[XYZ2]***, ***[XYZ3]*** → ***[XYZn]***
- "x" substitutes suffix number or character of units and channels in the register list.
- In case of unit, "x" means A, B, and C, ...
  Example: ***[ADACR0]***, ***[ADBCR0]***, ***[ADCCR0]*** → ***[ADxCR0]***
- In case of channel, "x" means 0, 1, and 2, ...
  Example: ***[T32A0RUNA]***, ***[T32A1RUNA]***, ***[T32A2RUNA]*** → ***[T32AxRUNA]***
- The bit range of a register is written like as [m: n].
  Example: Bit[3: 0] expresses the range of bit 3 to 0.
- The configuration value of a register is expressed by either the hexadecimal number or the binary number.
  Example: ***[ABCD]***<EFG> = 0x01 (hexadecimal), ***[XYZn]***<VW> = 1 (binary)
- Word and byte represent the following bit length.
  Byte: 8 bits
  Half word: 16 bits
  Word: 32 bits
  Double word: 64 bits
- Properties of each bit in a register are expressed as follows:
  R: Read only
  W: Write only
  R/W: Read and write are possible.
- Unless otherwise specified, register access supports only word access.
- The register defined as "Reserved" must not be rewritten. Moreover, do not use the read value.
- The value read from the bit having default value of "-" is unknown.
- When a register containing both of writable bits and read-only bits is written, read-only bits should be written with their default value, In the cases that default is "-", follow the definition of each register.
- Reserved bits of the write-only register should be written with their default value. In the cases that default is "-", follow the definition of each register.
- Do not use read-modified-write processing to the register of a definition which is different by writing and read out.

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Terms and Abbreviations

Some of abbreviations used in this document are as follows:

ADC	Analog to Digital Converter
A-PMD	Advanced Programmable Motor Control Circuit
BSC	Boundary Scan
CEC	Consumer Electronics Control
CG	Clock control and Generations
DAC	Digital to Analog Converter
DMA	Direct Memory Access
DMAC	Direct Memory Access Controller
DNF	Digital Noise Filter
EBIF	External Bus Interface
EHOSC	External High-speed Oscillator
EI2C	I^2C Interface Version A
ELOSC	External Low-speed Oscillator
FIR	Finite Impulse Response
fsys	frequency of SYSTEM Clock
FUART	Full Universal Asynchronous Receiver Transmitter
HDMAC	High-speed DMA Controller
IHOSC	Internal High-speed Oscillator
I2C	Inter-integrated Circuit
I2S	Inter-IC Sound
INT	Interrupt
ISD	Interval Sensor Detection
LTTMR	Long Term Timer
LVD	Voltage Detection Circuit
MDMAC	Multi-function DMA Controller
NBDIF	Non-break Debug Interface
NMI	Non-Maskable Interrupt
OFD	Oscillation Frequency Detector
POR	Power-on Reset Circuit
RLM	Reset LOSC<Low Power> Manager
RMC	Remote Control Signal Preprocessor
RTC	Real Time Clock
SIWDT	Clock Selective Watchdog Timer
SMIF	Serial Memory Interface
T32A	32-bit Timer Event Counter
TRGSEL	Trigger Selection Circuit
TSPI	Serial Peripheral Interface
TSSI	Synchronous Serial Interface
UART	Universal Asynchronous Receiver Transmitter

1. Outlines

This chapter describes the information which relates to peripheral functions about the channel or unit count, the pin information, and the product specific function. Use this document together with Reference manuals for peripheral functions.

2. Information of Peripheral Function

2.1. Register Base Address

The register base address type of TMPM4G Group (1) is shown below.
Each peripheral function should be developed using the type of the base address.

Table 2.1 Type of Register Base Address (1/3)

Peripheral function			Base address type (✓: Available, -: N/A)			Base address
			TYPE1	TYPE2	TYPE3	
High-speed DMA controller	HDMAC	unit A	✓	-	-	0x40000000
		unit B				0x40001000
Serial Memory Interface	SMIF	ch 0	✓	-	-	0x4000C000
Voltage Detection Circuit	LVD	-	✓	-	-	0x4003EC00
Long Term Timer	LTTMR	ch 0	✓	-	-	0x4003FF00
Serial Peripheral Interface	TSPI	ch 0	-	-	✓	0x4006A000
		ch 1				0x4006A400
		ch 2				0x4006A800
		ch 3				0x4006AC00
		ch 4				0x4006B000
		ch 5				0x4006B400
External Bus Interface	EBIF	-	-	-	✓	0x40076000
Digital Noise Filter Circuit	DNF	unit A	-	✓	-	0x400A0200
		unit B				0x400A0300
Trigger Selector	TRGSEL	ch 0	-	✓	-	0x400A0400
Clock Selective Watchdog Timer	SIWDT	ch 0	-	✓	-	0x400A0600
Non-break Debug Interface	NBD	-	-	✓	-	0x400A2000
Multi-function DMA controller	MDMAC	unit A	-	✓	-	0x400A4000
Full Universal Asynchronous Receiver Transmitter Circuit	FUART	ch 0	-	✓	-	0x400A8000
		ch 1				0x400A9000
12-bit Analog to Digital Converter	ADC	unit A	-	✓	-	0x400BA000
8-bit Digital to Analog Converter	DAC	ch 0	-	✓	-	0x400BC800
		ch 1				0x400BC900

Table 2.2 Type of Register Base Address (2/3)

Peripheral function			Base address type (✓: Available, -: N/A)			Base address
			TYPE1	TYPE2	TYPE3	
32-bit Timer Event Counter	T32A	ch 0	-	✓	-	0x400C1000
		ch 1				0x400C1400
		ch 2				0x400C1800
		ch 3				0x400C1C00
		ch 4				0x400C2000
		ch 5				0x400C2400
		ch 6				0x400C2800
		ch 7				0x400C2C00
		ch 8				0x400C3000
		ch 9				0x400C3400
		ch 10				0x400C3800
		ch 11				0x400C3C00
		ch 12				0x400C4000
		ch 13				0x400C4400
		ch 14				0x400C4800
		ch 15				0x400C4C00
Serial Peripheral Interface	TSPI	ch 6	-	✓	-	0x400CB800
		ch 7				0x400CBC00
		ch 8				0x400CC000
Synchronous Serial Interface	TSSI	ch 0	-	✓	-	0x400CD000
		ch 1				0x400CD400
Asynchronous Serial Communication Circuit	UART	ch 0	-	✓	-	0x400CE000
		ch 1				0x400CE400
		ch 2				0x400CE800
		ch 3				0x400CEC00
		ch 4				0x400CF000
		ch 5				0x400CF400
I^2S Interface	I2S	ch 0	-	✓	-	0x400D0000
		ch 1				0x400D0800
I^2C Interface	I2C	ch 0	-	✓	-	0x400D1000
		ch 1				0x400D2000
		ch 2				0x400D3000
		ch 3				0x400D4000
		ch 4				0x400D5000
I^2C Interface Version A	EI2C	ch 0	-	✓	-	0x400D8000
		ch 1				0x400D9000
		ch 2				0x400DA000
		ch 3				0x400DB000
		ch 4				0x400DC000
FIR calculation Circuit	FIR	-	-	✓	-	0x400DD000

Table 2.3 Type of Register Base Address (3/3)

Peripheral function			Base address type (✓: Available, -: N/A)			Base address
			TYPE1	TYPE2	TYPE3	
Trimming Circuit	TRM	-	-	✓	-	0x400E3100
Oscillation Frequency Detector	OFD	-	-	✓	-	0x400E4000
Real Time Clock	RTC	-	-	✓	-	0x400E4800
Consumer Electronics Control Circuit	CEC	ch 0	-	✓	-	0x400E8000
Remote Control Signal Preprocessor	RMC	ch 0	-	✓	-	0x400E8100
		ch 1				0x400E8200
Advanced Programmable Motor Control Circuit	A-PMD	ch 0	-	✓	-	0x400E9000
Interval Sensor Detection Circuit	ISD	unit A	-	✓	-	0x400F0000
		unit B				0x400F0100
		unit C				0x400F0200
Flash Memory	FLASH	-	✓	-	-	0x5DFF0000

2.2. Trigger Selector (TRGSEL)

The trigger selector (TRGSEL) is the circuit which selects the one trigger and outputs the trigger signal to the peripheral function from two or more triggers inputted from the peripheral function, the port, etc.

The trigger selected from eight triggers by ***[TSEL0CRn]***<INSELm> is outputted to the peripheral function of a connection destination.

Figure 2.1 shows an example of the trigger selector connection. One of TSPI, UART, I2C, and T32A triggers is selected and connected to DMA controller via the TRGSEL. ***[TSEL0CR0]***<INSEL0> controls the input trigger selection, enable or disable of the edge detection, the setting of the conditions of the edge detection, and enable or disable of the trigger output.

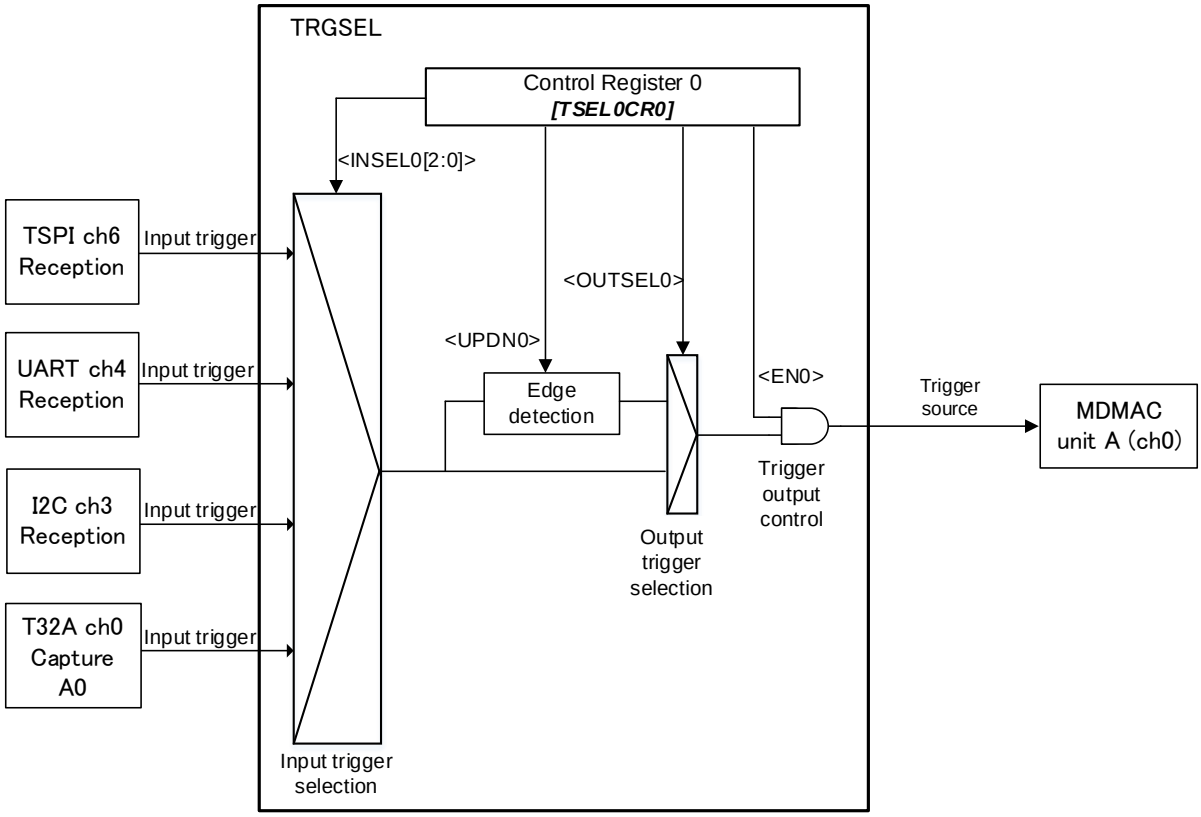

Figure 2.1 Example of TRGSEL connection

2.2.1. TRGSEL for Each Product

TRGSEL of TMPM4G Group (1) consists of 15 control registers (***[TSEL0CR0]*** ~ ***[TSEL0CR14]***) and can control 57 triggers.

The control register, the connection destination, and corresponding products are shown in the following tables.

Table 2.4 List of TRGSEL for Each Product (1/7)

Register		Trigger source	Input trigger	Product table (✓: Available, -: N/A)		
	Bit symbol			M4GR	M4GQ	M4GN
[TSEL0CR0]	INSEL0[2:0]	MDMAC unit A ch0	TSPI ch6 receive DMA request	✓	✓	-
			UART ch4 reception DMA request	✓	✓	-
			I2C ch3 receiving DMA request	✓	✓	-
			T32A ch0 DMA request at capture A0 register	✓	✓	✓
			EI2C ch3 receiving DMA request	✓	✓	-
			I2S ch0 receiving DMA request	✓	✓	✓
	INSEL1[2:0]	MDMAC unit A ch1	TSPI ch6 transmit DMA request	✓	✓	-
			UART ch4 transmission DMA request	✓	✓	-
			I2C ch3 transmitting DMA request	✓	✓	-
			T32A ch0 DMA request at capture C0 register	✓	✓	✓
			EI2C ch3 transmitting DMA request	✓	✓	-
			I2S ch0 transmitting DMA request	✓	✓	✓
	INSEL2[2:0]	MDMAC unit A ch2	TSPI ch7 receive DMA request	✓	✓	-
			FUART ch1 reception DMA request	✓	✓	-
			I2C ch4 receiving DMA request	✓	✓	-
			EI2C ch4 receiving DMA request	✓	✓	-
			I2S ch1 receiving DMA request	✓	✓	✓
	INSEL3[2:0]	MDMAC unit A ch3	TSPI ch7 transmit DMA request	✓	✓	-
			FUART ch1 transmission DMA request	✓	✓	-
			I2C ch4 transmitting DMA request	✓	✓	-
			EI2C ch4 transmitting DMA request	✓	✓	-
			I2S ch1 transmitting DMA request	✓	✓	✓
[TSEL0CR1]	INSEL4[2:0]	MDMAC unit A ch4	TSPI ch8 receive DMA request	✓	-	-
			T32A ch0 DMA request at match A1 register	✓	✓	✓
			T32A ch0 DMA request at match C1 register	✓	✓	✓
			FIR input data write request	✓	✓	✓
	INSEL5[2:0]	MDMAC unit A ch5	TSPI ch8 transmit DMA request	✓	-	-
			T32A ch0 DMA request at match B1 register	✓	✓	✓
			T32A ch0 DMA request at capture B0 register	✓	✓	✓
			FIR arithmetic result data read request	✓	✓	✓
	INSEL6[2:0]	MDMAC unit A ch6	T32A ch1 DMA request at match A1 register	✓	✓	✓
			T32A ch1 DMA request at match C1 register	✓	✓	✓
			T32A ch1 DMA request at capture A0 register	✓	✓	✓
			T32A ch1 DMA request at capture C0 register	✓	✓	✓
	INSEL7[2:0]	MDMAC unit A ch7	T32A ch1 DMA request at match B1 register	✓	✓	✓
			T32A ch1 DMA request at capture B0 register	✓	✓	✓
			UART ch0 reception DMA request	✓	✓	✓
			I2C ch0 receiving DMA request	✓	✓	✓
			EI2C ch0 receiving DMA request	✓	✓	✓

Table 2.5 List of TRGSEL for Each Product (2/7)

Register		Trigger source	Input trigger	Product table (✓: Available, -: N/A)		
	Bit symbol			M4GR	M4GQ	M4GN
[TSEL0CR2]	INSEL8[2:0]	MDMAC unit A ch8	T32A ch2 DMA request at match A1 register	✓	✓	✓
			T32A ch2 DMA request at match C1 register	✓	✓	✓
			T32A ch2 DMA request at capture A0 register	✓	✓	✓
			T32A ch2 DMA request at capture C0 register	✓	✓	✓
	INSEL9[2:0]	MDMAC unit A ch9	T32A ch2 DMA request at match B1 register	✓	✓	✓
			T32A ch2 DMA request at capture B0 register	✓	✓	✓
			UART ch0 transmission DMA request	✓	✓	✓
			I2C ch0 transmitting DMA request	✓	✓	✓
			EI2C ch0 transmitting DMA request	✓	✓	✓
	INSEL10[2:0]	MDMAC unit A ch10	T32A ch3 DMA request at match A1 register	✓	✓	✓
			T32A ch3 DMA request at match C1 register	✓	✓	✓
			T32A ch3 DMA request at capture A0 register	✓	✓	✓
			T32A ch3 DMA request at capture C0 register	✓	✓	✓
	INSEL11[2:0]	MDMAC unit A ch11	T32A ch3 DMA request at match B1 register	✓	✓	✓
			T32A ch3 DMA request at capture B0 register	✓	✓	✓
			UART ch1 reception DMA request	✓	✓	✓
			I2C ch1 receiving DMA request	✓	✓	✓
			EI2C ch1 receiving DMA request	✓	✓	✓
[TSEL0CR3]	INSEL12[2:0]	MDMAC unit A ch12	T32A ch4 DMA request at match A1 register	✓	✓	✓
			T32A ch4 DMA request at match C1 register	✓	✓	✓
			T32A ch4 DMA request at capture A0 register	✓	✓	✓
			T32A ch4 DMA request at capture C0 register	✓	✓	✓
	INSEL13[2:0]	MDMAC unit A ch13	T32A ch4 DMA request at match B1 register	✓	✓	✓
			T32A ch4 DMA request at capture B0 register	✓	✓	✓
			UART ch1 transmission DMA request	✓	✓	✓
			I2C ch1 transmitting DMA request	✓	✓	✓
			EI2C ch1 transmitting DMA request	✓	✓	✓
	INSEL14[2:0]	MDMAC unit A ch14	T32A ch5 DMA request at match A1 register	✓	✓	✓
			T32A ch5 DMA request at match C1 register	✓	✓	✓
			T32A ch5 DMA request at capture A0 register	✓	✓	✓
			T32A ch5 DMA request at capture C0 register	✓	✓	✓
	INSEL15[2:0]	MDMAC unit A ch15	T32A ch5 DMA request at match B1 register	✓	✓	✓
			T32A ch5 DMA request at capture B0 register	✓	✓	✓
			FUART ch0 transmission DMA request	✓	✓	✓
			I2C ch2 transmitting DMA request	✓	✓	✓
			EI2C ch2 transmitting DMA request	✓	✓	✓

Table 2.6 List of TRGSEL for Each Product (3/7)

Register		Trigger source	Input trigger	Product table (✓: Available, -: N/A)		
	Bit symbol			M4GR	M4GQ	M4GN
[TSEL0CR4]	INSEL16[2:0]	MDMAC unit A ch16	T32A ch6 DMA request at match A1 register	✓	✓	✓
			T32A ch6 DMA request at match C1 register	✓	✓	✓
			T32A ch6 DMA request at capture A0 register	✓	✓	✓
			T32A ch6 DMA request at capture C0 register	✓	✓	✓
	INSEL17[2:0]	MDMAC unit A ch17	T32A ch6 DMA request at match B1 register	✓	✓	✓
			T32A ch6 DMA request at capture B0 register	✓	✓	✓
			FUART ch0 reception DMA request	✓	✓	✓
			I2C ch2 receiving DMA request	✓	✓	✓
			EI2C ch2 receiving DMA request	✓	✓	✓
	INSEL18[2:0]	MDMAC unit A ch18	T32A ch7 DMA request at match A1 register	✓	✓	✓
			T32A ch7 DMA request at match C1 register	✓	✓	✓
			T32A ch7 DMA request at capture A0 register	✓	✓	✓
			T32A ch7 DMA request at capture C0 register	✓	✓	✓
			UART ch0 reception DMA request	✓	✓	✓
	INSEL19[2:0]	MDMAC unit A ch19	T32A ch7 DMA request at match B1 register	✓	✓	✓
			T32A ch7 DMA request at capture B0 register	✓	✓	✓
			UART ch2 reception DMA request	✓	✓	✓
			ADC unit A general purpose trigger DMA request	✓	✓	✓
			TSSI ch0 receive DMA request	✓	✓	✓
[TSEL0CR5]	INSEL20[2:0]	MDMAC unit A ch20	T32A ch8 DMA request at match A1 register	✓	✓	✓
			T32A ch8 DMA request at match C1 register	✓	✓	✓
			T32A ch8 DMA request at capture A0 register	✓	✓	✓
			T32A ch8 DMA request at capture C0 register	✓	✓	✓
			UART ch0 transmission DMA request	✓	✓	✓
	INSEL21[2:0]	MDMAC unit A ch21	T32A ch8 DMA request at match B1 register	✓	✓	✓
			T32A ch8 DMA request at capture B0 register	✓	✓	✓
			UART ch2 transmission DMA request	✓	✓	✓
			ADC unit A Highest priority DMA request	✓	✓	✓
			TSSI ch0 transmit DMA request	✓	✓	✓
	INSEL22[2:0]	MDMAC unit A ch22	T32A ch9 DMA request at match A1 register	✓	✓	✓
			T32A ch9 DMA request at match C1 register	✓	✓	✓
			T32A ch9 DMA request at capture A0 register	✓	✓	✓
			T32A ch9 DMA request at capture C0 register	✓	✓	✓
			UART ch1 reception DMA request	✓	✓	✓
	INSEL23[2:0]	MDMAC unit A ch23	T32A ch9 DMA request at match B1 register	✓	✓	✓
			T32A ch9 DMA request at capture B0 register	✓	✓	✓
			T32A ch9 DMA request at capture A1 register	✓	✓	✓
			T32A ch9 DMA request at capture B1 register	✓	✓	✓
			UART ch1 transmission DMA request	✓	✓	✓

Table 2.7 List of TRGSEL for Each Product (4/7)

Register		Trigger source	Input trigger	Product table (✓: Available, -: N/A)		
	Bit symbol			M4GR	M4GQ	M4GN
[TSEL0CR6]	INSEL24[2:0]	MDMAC unit A ch24	T32A ch10 DMA request at match A1 register	✓	✓	✓
			T32A ch10 DMA request at match C1 register	✓	✓	✓
			T32A ch10 DMA request at capture A0 register	✓	✓	✓
			T32A ch10 DMA request at capture C0 register	✓	✓	✓
			UART ch2 reception DMA request	✓	✓	✓
	INSEL25[2:0]	MDMAC unit A ch25	T32A ch10 DMA request at match B1 register	✓	✓	✓
			T32A ch10 DMA request at capture B0 register	✓	✓	✓
			T32A ch10 DMA request at capture A1 register	✓	✓	✓
			T32A ch10 DMA request at capture B1 register	✓	✓	✓
			UART ch2 transmission DMA request	✓	✓	✓
	INSEL26[2:0]	MDMAC unit A ch26	T32A ch11 DMA request at match A1 register	✓	✓	✓
			T32A ch11 DMA request at match C1 register	✓	✓	✓
			T32A ch11 DMA request at capture A0 register	✓	✓	✓
			T32A ch11 DMA request at capture C0 register	✓	✓	✓
			TSSI ch1 receive DMA request	✓	-	-
	INSEL27[2:0]	MDMAC unit A ch27	T32A ch11 DMA request at match B1 register	✓	✓	✓
			T32A ch11 DMA request at capture B0 register	✓	✓	✓
			T32A ch11 DMA request at capture A1 register	✓	✓	✓
			T32A ch11 DMA request at capture B1 register	✓	✓	✓
			TSSI ch1 transmit DMA request	✓	-	-
[TSEL0CR7]	INSEL28[2:0]	MDMAC unit A ch28	T32A ch12 DMA request at match A1 register	✓	✓	✓
			T32A ch12 DMA request at match C1 register	✓	✓	✓
			UART ch3 reception DMA request	✓	✓	-
			T32A ch12 DMA request at capture A0 register	✓	✓	✓
			T32A ch12 DMA request at capture C0 register	✓	✓	✓
	INSEL29[2:0]	MDMAC unit A ch29	T32A ch12 DMA request at match B1 register	✓	✓	✓
			UART ch3 transmission DMA request	✓	✓	-
			A-PMD ch0 PWM interrupt	✓	✓	✓
			T32A ch12 DMA request at capture B0 register	✓	✓	✓
	INSEL30[2:0]	MDMAC unit A ch30	T32A ch13 DMA request at match A1 register	✓	✓	✓
			T32A ch13 DMA request at match C1 register	✓	✓	✓
			UART ch5 reception DMA request	✓	-	-
			T32A ch13 DMA request at capture A0 register	✓	✓	✓
			T32A ch13 DMA request at capture C0 register	✓	✓	✓
	INSEL31[2:0]	MDMAC unit A ch31	T32A ch13 DMA request at match B1 register	✓	✓	✓
			UART ch5 transmission DMA request	✓	-	-
			PT3 pin (TRGIN2)	✓	✓	✓
			T32A ch13 DMA request at capture B0 register	✓	✓	✓

Table 2.8 List of TRGSEL for Each Product (5/7)

Register		Trigger source	Input trigger	Product table (✓: Available, -: N/A)		
	Bit symbol			M4GR	M4GQ	M4GN
[TSEL0CR8]	INSEL32[2:0]	ADC unit A	A-PMD ch0 ADC synchronous trigger output 0	✓	✓	✓
			A-PMD ch0 ADC synchronous trigger output 1	✓	✓	✓
			A-PMD ch0 ADC synchronous trigger output 2	✓	✓	✓
			A-PMD ch0 ADC synchronous trigger output 3	✓	✓	✓
			TRGSEL37 output (INSEL37)	✓	✓	✓
			TRGSEL38 output (INSEL38)	✓	✓	✓
	INSEL33[2:0]	ADC unit A	A-PMD ch0 ADC synchronous trigger output 0	✓	✓	✓
			A-PMD ch0 ADC synchronous trigger output 1	✓	✓	✓
			A-PMD ch0 ADC synchronous trigger output 2	✓	✓	✓
			A-PMD ch0 ADC synchronous trigger output 3	✓	✓	✓
			TRGSEL37 output (INSEL37)	✓	✓	✓
			TRGSEL38 output (INSEL38)	✓	✓	✓
	INSEL34[2:0]	T32A ch8 timer A	ELOSC low speed clock	✓	✓	✓
			TSPI ch8 transmit complete trigger	✓	-	-
			TSPI ch8 receive complete trigger	✓	-	-
	INSEL35[2:0]	T32A ch13 timer A	RMC ch0 trigger output	✓	✓	✓
			T32A ch2 timer register A0 match trigger	✓	✓	✓
[TSEL0CR9]	INSEL36[2:0]	T32A ch13 timer B	RMC ch1 trigger output	✓	✓	-
			T32A ch2 timer register A0 match trigger	✓	✓	✓
	INSEL37[2:0]	TRGSEL32, TRGSEL33	T32A ch9 timer register A1 match trigger	✓	✓	✓
			T32A ch9 timer register B1 match trigger	✓	✓	✓
			T32A ch10 timer register A1 match trigger	✓	✓	✓
			T32A ch10 timer register B1 match trigger	✓	✓	✓
			T32A ch11 timer register A1 match trigger	✓	✓	✓
			T32A ch11 timer register B1 match trigger	✓	✓	✓
			PG3 pin (TRGIN0)	✓	✓	✓
			PL7 pin (TRGIN1)	✓	-	-
	INSEL38[2:0]	TRGSEL32, TRGSEL33	T32A ch9 timer register A1 match trigger	✓	✓	✓
			T32A ch9 timer register B1 match trigger	✓	✓	✓
			T32A ch10 timer register A1 match trigger	✓	✓	✓
			T32A ch10 timer register B1 match trigger	✓	✓	✓
			T32A ch11 timer register A1 match trigger	✓	✓	✓
			T32A ch11 timer register B1 match trigger	✓	✓	✓
			PG3 pin (TRGIN0)	✓	✓	✓
			PL7 pin (TRGIN1)	✓	-	-
	INSEL39[2:0]	T32A ch5 timer A	T32A ch9 timer register A0 match trigger	✓	✓	✓
			T32A ch13 timer register A0 match trigger	✓	✓	✓
			TSPI ch5 transmit complete trigger	✓	✓	-
			UART ch5 transmission completion trigger	✓	-	-

Table 2.9 List of TRGSEL for Each Product (6/7)

Register		Trigger source	Input trigger	Product table (✓: Available, -: N/A)		
	Bit symbol			M4GR	M4GQ	M4GN
[TSEL0CR10]	INSEL40[2:0]	T32A ch5 timer B	T32A ch9 timer register A0 match trigger	✓	✓	✓
			T32A ch13 timer register A0 match trigger	✓	✓	✓
			TSPI ch5 receive complete trigger	✓	✓	-
			UART ch5 reception completion trigger	✓	-	-
			T32A ch5 timer register A0 match trigger	✓	✓	✓
	INSEL41[2:0]	T32A ch6 timer A	T32A ch10 timer register A0 match trigger	✓	✓	✓
			T32A ch13 timer register B0 match trigger	✓	✓	✓
			TSPI ch6 transmit complete trigger	✓	✓	-
	INSEL42[2:0]	T32A ch6 timer B	T32A ch10 timer register A0 match trigger	✓	✓	✓
			T32A ch13 timer register B0 match trigger	✓	✓	✓
			TSPI ch6 receive complete trigger	✓	✓	-
			T32A ch6 timer register A0 match trigger	✓	✓	✓
	INSEL43[2:0]	T32A ch7 timer A	T32A ch11 timer register A0 match trigger	✓	✓	✓
			T32A ch13 timer register B0 match trigger	✓	✓	✓
			TSPI ch7 transmit complete trigger	✓	✓	-
[TSEL0CR11]	INSEL44[2:0]	T32A ch7 timer B	T32A ch11 timer register A0 match trigger	✓	✓	✓
			T32A ch13 timer register B0 match trigger	✓	✓	✓
			TSPI ch7 receive complete trigger	✓	✓	-
			T32A ch7 timer register A0 match trigger	✓	✓	✓
	INSEL45[2:0]	T32A ch8 timer B	T32A ch4 timer B output	✓	✓	✓
			T32A ch8 timer A output	✓	✓	✓
	INSEL46[2:0]	T32A ch0 timer A	TSPI ch0 transmit complete trigger	✓	✓	✓
			UART ch0 transmission completion trigger	✓	✓	✓
			T32A ch12 timer register A0 match trigger	✓	✓	✓
	INSEL47[2:0]	T32A ch0 timer B	TSPI ch0 receive complete trigger	✓	✓	✓
			UART ch0 reception completion trigger	✓	✓	✓
			T32A ch12 timer register A0 match trigger	✓	✓	✓
			T32A ch0 timer register A0 match trigger	✓	✓	✓

Table 2.10 List of TRGSEL for Each Product (7/7)

Register		Trigger source	Input trigger	Product table (✓: Available, -: N/A)		
	Bit symbol			M4GR	M4GQ	M4GN
[TSEL0CR12]	INSEL48[2:0]	T32A ch1 timer A	TSPI ch1 transmit complete trigger	✓	✓	✓
			UART ch1 transmission completion trigger	✓	✓	✓
			T32A ch12 timer register A0 match trigger	✓	✓	✓
	INSEL49[2:0]	T32A ch1 timer B	TSPI ch1 receive complete trigger	✓	✓	✓
			UART ch1 reception completion trigger	✓	✓	✓
			T32A ch12 timer register A0 match trigger	✓	✓	✓
			T32A ch1 timer register A0 match trigger	✓	✓	✓
	INSEL50[2:0]	T32A ch2 timer A	TSPI ch2 transmit complete trigger	✓	✓	✓
			UART ch2 transmission completion trigger	✓	✓	✓
			T32A ch12 timer register B0 match trigger	✓	✓	✓
	INSEL51[2:0]	T32A ch2 timer B	TSPI ch2 receive complete trigger	✓	✓	✓
			UART ch2 reception completion trigger	✓	✓	✓
			T32A ch12 timer register B0 match trigger	✓	✓	✓
			T32A ch2 timer register A0 match trigger	✓	✓	✓
[TSEL0CR13]	INSEL52[2:0]	T32A ch3 timer A	TSPI ch3 transmit complete trigger	✓	✓	✓
			T32A ch12 timer register B0 match trigger	✓	✓	✓
			UART ch3 transmission completion trigger	✓	✓	-
	INSEL53[2:0]	T32A ch3 timer B	TSPI ch3 receive complete trigger	✓	✓	✓
			T32A ch12 timer register B0 match trigger	✓	✓	✓
			UART ch3 reception completion trigger	✓	✓	-
			T32A ch3 timer register A0 match trigger	✓	✓	✓
	INSEL54[2:0]	T32A ch4 timer A	TSPI ch4 transmit complete trigger	✓	✓	✓
			T32A ch13 timer register A0 match trigger	✓	✓	✓
			UART ch4 transmission completion trigger	✓	✓	-
	INSEL55[2:0]	T32A ch4 timer B	TSPI ch4 receive complete trigger	✓	✓	✓
			T32A ch13 timer register A0 match trigger	✓	✓	✓
			UART ch4 reception completion trigger	✓	✓	-
			T32A ch4 timer register A0 match trigger	✓	✓	✓
[TSEL0CR14]	INSEL56[2:0]	FIR	I2S ch0 receive FIFO threshold signal	✓	✓	✓
			I2S ch0 transmit FIFO threshold signal	✓	✓	✓
			I2S ch1 receive FIFO threshold signal	✓	✓	✓
			I2S ch1 transmit FIFO threshold signal	✓	✓	✓

2.2.2. Operation and Setting

When using TRGSEL, please set an applicable clock enable bit to "1" (clock supply) in fsys supply stop register A (***[CGFSYSENA]***, ***[CGFSYSMENA]***), fsys supply stop register B (***[CGFSYSENB]***, ***[CGFSYSMENB]***), fsys supply stop register C (***[CGFSYSMENC]***), and fc supply stop registers (***[CGFCEN]***).

An applicable register and the bit position vary according to a product. Therefore, the register may not exist with the product. Please refer to reference manual "Clock Control and Operation Mode" for the details.

Setting procedure of trigger selector is as following.

(1) Selection of an input trigger (***[TSEL0CRn]*** <INSELm>)

Selection of the input trigger used for the trigger source is performed.
Please set up selection of the input trigger by the input trigger subdevice bit (***[TSEL0CRn]*** <INSELm>) of the control register. (n: register number, m: trigger number)

(2) Selection of edge detection conditions (***[TSEL0CRn]*** <UPDNm>)

For the selected input trigger signal, select detection of rising edge or falling edge.
To select the edge detection condition, set with the edge detection condition bit (***[TSEL0CRn]*** <UPDNm>) of the control register.
The following shows the trigger signal which needs edge detection.

- External trigger input (TRGIN0, TRGIN1, and TRGIN2)
- ELOSC low speed clock (fs)
- RMC channel x trigger output (RMC0TRG, RMC1TRG)

(3) Selection of a trigger output (***[TSEL0CRn]***<OUTSELm>)

Selection of an output without or with edge detection is performed.
Please set up selection of a trigger output in the selection bit (***[TSEL0CRn]***<OUTSELm>) of a control register.

(4) Output enable (***[TSEL0CRn]***<ENm>)

The output (enable/disable) of the selected trigger signal is chosen.
Please set up selection of output (enable/disable) in the setting bit (***[TSEL0CRn]***<ENm>) of a control register.
A trigger output will be enabled if ***[TSEL0CRn]***<ENm> is set to "1".

2.2.3. List of Registers

The control registers and their addresses are shown in the following tables.

Peripheral function		Channel/unit	Base address
			TYPE 2
Trigger Selector	TRGSEL	ch0	0x400A0400

Register name		Address (Base+)
Control Register 0	***[TSEL0CR0]***	0x0000
Control Register 1	***[TSEL0CR1]***	0x0004
Control Register 2	***[TSEL0CR2]***	0x0008
Control Register 3	***[TSEL0CR3]***	0x000C
Control Register 4	***[TSEL0CR4]***	0x0010
Control Register 5	***[TSEL0CR5]***	0x0014
Control Register 6	***[TSEL0CR6]***	0x0018
Control Register 7	***[TSEL0CR7]***	0x001C
Control Register 8	***[TSEL0CR8]***	0x0020
Control Register 9	***[TSEL0CR9]***	0x0024
Control Register 10	***[TSEL0CR10]***	0x0028
Control Register 11	***[TSEL0CR11]***	0x002C
Control Register 12	***[TSEL0CR12]***	0x0030
Control Register 13	***[TSEL0CR13]***	0x0034
Control Register 14	***[TSEL0CR14]***	0x0038

2.2.4. Details of Registers

2.2.4.1. *[TSEL0CR0]* (Control Register 0)

Bit	Bit symbol	After reset	Type	Description
31	-	0	R	Read as "0".
30:28	INSEL3[2:0]	000	R/W	Input trigger selection (MDMAC unit A ch3) 000: TSPI ch7 transmit DMA request (TSPI7TX_DMA) 001: FUART ch1 transmission DMA request (FUART1TX_DMAREQ) 010: I2C ch4 transmitting DMA request (I2C4TXDMAREQ) 011: EI2C ch4 transmitting DMA request (I2C4ATXDMAREQ) 100: I2S ch1 transmitting DMA request (I2S1TXDMAREQ) Others: Reserved
27	-	0	R	Read as "0".
26	UPDN3	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.
25	OUTSEL3	0	R/W	Output trigger selection 0: No edge is detected. 1: An edge is detected.
24	EN3	0	R/W	Trigger output control 0: Disabled 1: Enabled
23	-	0	R	Read as "0".
22:20	INSEL2[2:0]	000	R/W	Input trigger selection (MDMAC unit A ch2) 000: TSPI ch7 receive DMA request (TSPI7RX_DMA) 001: FUART ch1 reception DMA request (FUART1RX_DMAREQ) 010: I2C ch4 receiving DMA request (I2C4RXDMAREQ) 011: EI2C ch4 receiving DMA request (I2C4ARXDMAREQ) 100: I2S ch1 receiving DMA request (I2S1RXDMAREQ) Others: Reserved
19	-	0	R	Read as "0".
18	UPDN2	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.
17	OUTSEL2	0	R/W	Output trigger selection 0: No edge is detected. 1: An edge is detected.
16	EN2	0	R/W	Trigger output control 0: Disabled 1: Enabled
15	-	0	R	Read as "0".

Bit	Bit symbol	After reset	Type	Description
14:12	INSEL1[2:0]	000	R/W	Input trigger selection (MDMAC unit A ch1) 000: TSPI ch6 transmit DMA request (TSPI6TX_DMA) 001: UART ch4 transmission DMA request (UART4TX_DMAREQ) 010: I2C ch3 transmitting DMA request (I2C3TXDMAREQ) 011: T32A ch0 DMA request at capture C0 register (T32A00DMAREQCAPC0) 100: EI2C ch3 transmitting DMA request (I2C3ATXDMAREQ) 101: I2S ch0 transmitting DMA request (I2S0TXDMAREQ) Others: Reserved
11	-	0	R	Read as "0".
10	UPDN1	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.
9	OUTSEL1	0	R/W	Output trigger selection 0: No edge is detected. 1: An edge is detected.
8	EN1	0	R/W	Trigger output control 0: Disabled 1: Enabled
7	-	0	R	Read as "0".
6:4	INSEL0[2:0]	000	R/W	Input trigger selection (MDMAC unit A ch0) 000: TSPI ch6 receive DMA request (TSPI6RX_DMA) 001: UART ch4 reception DMA request (UART4RX_DMAREQ) 010: I2C ch3 receiving DMA request (I2C3RXDMAREQ) 011: T32A ch0 DMA request at capture A0 register (T32A00DMAREQCAPA0) 100: EI2C ch3 receiving DMA request (I2C3ARXDMAREQ) 101: I2S ch0 receiving DMA request (I2S0RXDMAREQ) Others: Reserved
3	-	0	R	Read as "0".
2	UPDN0	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.
1	OUTSEL0	0	R/W	Output trigger selection 0: No edge is detected. 1: An edge is detected.
0	EN0	0	R/W	Trigger output control 0: Disabled 1: Enabled

2.2.4.2. *[TSEL0CR1]* (Control Register 1)

Bit	Bit symbol	After reset	Type	Description
31	-	0	R	Read as "0".
30:28	INSEL7[2:0]	000	R/W	Input trigger selection (MDMAC unit A ch7) 000: T32A ch1 DMA request at match B1 register (T32A01DMAREQCMPB1) 001: T32A ch1 DMA request at capture B0 register (T32A01DMAREQCAPB0) 010: UART ch0 reception DMA request (UART0RX_DMAREQ) 011: I2C ch0 receiving DMA request (I2C0RXDMAREQ) 100: EI2C ch0 receiving DMA request (I2C0ARXDMAREQ) Others: Reserved.
27	-	0	R	Read as "0".
26	UPDN7	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.
25	OUTSEL7	0	R/W	Output trigger selection 0: No edge is detected. 1: An edge is detected.
24	EN7	0	R/W	Trigger output control 0: Disabled 1: Enabled
23	-	0	R	Read as "0".
22:20	INSEL6[2:0]	000	R/W	Input trigger selection (MDMAC unit A ch6) 000: T32A ch1 DMA request at match A1 register (T32A01DMAREQCMPA1) 001: T32A ch1 DMA request at match C1 register (T32A01DMAREQCMPC1) 010: T32A ch1 DMA request at capture A0 register (T32A01DMAREQCAPA0) 011: T32A ch1 DMA request at capture C0 register (T32A01DMAREQCAPC0) Others: Reserved
19	-	0	R	Read as "0".
18	UPDN6	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.
17	OUTSEL6	0	R/W	Output trigger selection 0: No edge is detected. 1: An edge is detected.
16	EN6	0	R/W	Trigger output control 0: Disabled 1: Enabled
15	-	0	R	Read as "0".

Bit	Bit symbol	After reset	Type	Description
14:12	INSEL5[2:0]	000	R/W	Input trigger selection (MDMAC unit A ch5) 000: TSPI ch8 transmit DMA request (TSPI8TX_DMA) 001: T32A ch0 DMA request at match B1 register (T32A00DMAREQCMPB1) 010: T32A ch0 DMA request at capture B0 register (T32A00DMAREQCAPB0) 011: FIR arithmetic result data read request (FIRDATARDDMAREQ) Others: Reserved
11	-	0	R	Read as "0".
10	UPDN5	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.
9	OUTSEL5	0	R/W	Output trigger selection 0: No edge is detected. 1: An edge is detected.
8	EN5	0	R/W	Trigger output control 0: Disabled 1: Enabled
7	-	0	R	Read as "0".
6:4	INSEL4[2:0]	000	R/W	Input trigger selection (MDMAC unit A ch4) 000: TSPI ch8 receive DMA request (TSPI8RX_DMA) 001: T32A ch0 DMA request at match A1 register (T32A00DMAREQCMPA1) 010: T32A ch0 DMA request at match C1 register (T32A00DMAREQCMPC1) 011: FIR input data write request (FIRDATAWRDMAREQ) Others: Reserved
3	-	0	R	Read as "0".
2	UPDN4	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.
1	OUTSEL4	0	R/W	Output trigger selection 0: No edge is detected. 1: An edge is detected.
0	EN4	0	R/W	Trigger output control 0: Disabled 1: Enabled

2.2.4.3. *[TSEL0CR2]* (Control Register 2)

Bit	Bit symbol	After reset	Type	Description
31	-	0	R	Read as "0".
30:28	INSEL11[2:0]	000	R/W	Input trigger selection (MDMAC unit A ch11) 000: T32A ch3 DMA request at match B1 register (T32A03DMAREQCMPB1) 001: T32A ch3 DMA request at capture B0 register (T32A03DMAREQCAPB0) 010: UART ch1 reception DMA request (UART1RX_DMAREQ) 011: I2C ch1 receiving DMA request (I2C1RXDMAREQ) 100: EI2C ch1 receiving DMA request (I2C1ARXDMAREQ) Others: Reserved
27	-	0	R	Read as "0".
26	UPDN11	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.
25	OUTSEL11	0	R/W	Output trigger selection 0: No edge is detected. 1: An edge is detected.
24	EN11	0	R/W	Trigger output control 0: Disabled 1: Enabled
23	-	0	R	Read as "0".
22:20	INSEL10[2:0]	000	R/W	Input trigger selection (MDMAC unit A ch10) 000: T32A ch3 DMA request at match A1 register (T32A03DMAREQCMPA1) 001: T32A ch3 DMA request at match C1 register (T32A03DMAREQCMPC1) 010: T32A ch3 DMA request at capture A0 register (T32A03DMAREQCAPA0) 011: T32A ch3 DMA request at match C0 register (T32A03DMAREQCAPC0) Others: Reserved
19	-	0	R	Read as "0".
18	UPDN10	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.
17	OUTSEL10	0	R/W	Output trigger selection 0: No edge is detected. 1: An edge is detected.
16	EN10	0	R/W	Trigger output control 0: Disabled 1: Enabled
15	-	0	R	Read as "0".

Bit	Bit symbol	After reset	Type	Description
14:12	INSEL9[2:0]	000	R/W	Input trigger selection (MDMAC unit A ch9) 000: T32A ch2 DMA request at match B1 register (T32A02DMAREQCMPB1) 001: T32A ch2 DMA request at capture B0 register (T32A02DMAREQCAPB0) 010: UART ch0 transmission DMA request (UART0TX_DMAREQ) 011: I2C ch0 transmitting DMA request (I2C0TXDMAREQ) 100: EI2C ch0 transmitting DMA request (I2C0ATXDMAREQ) Others: Reserved
11	-	0	R	Read as "0".
10	UPDN9	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.
9	OUTSEL9	0	R/W	Output trigger selection 0: No edge is detected. 1: An edge is detected.
8	EN9	0	R/W	Trigger output control 0: Disabled 1: Enabled
7	-	0	R	Read as "0".
6:4	INSEL8[2:0]	000	R/W	Input trigger selection (MDMAC unit A ch8) 000: T32A ch2 DMA request at match A1 register (T32A02DMAREQCMPA1) 001: T32A ch2 DMA request at match C1 register (T32A02DMAREQCMPC1) 010: T32A ch2 DMA request at capture A0 register (T32A02DMAREQCAPA0) 011: T32A ch2 DMA request at capture C0 register (T32A02DMAREQCAPC0) Others: Reserved
3	-	0	R	Read as "0".
2	UPDN8	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.
1	OUTSEL8	0	R/W	Output trigger selection 0: No edge is detected. 1: An edge is detected.
0	EN8	0	R/W	Trigger output control 0: Disabled 1: Enabled

2.2.4.4. *[TSEL0CR3]* (Control Register 3)

Bit	Bit symbol	After reset	Type	Description
31	-	0	R	Read as "0".
30:28	INSEL15[2:0]	000	R/W	Input trigger selection (MDMAC unit A ch15) 000: T32A ch5 DMA request at match B1 register (T32A05DMAREQCMPB1) 001: T32A ch5 DMA request at capture B0 register (T32A05DMAREQCAPB0) 010: FUART ch0 transmission DMA request (FUART0TX_DMAREQ) 011: I2C ch2 transmitting DMA request (I2C2TXDMAREQ) 100: EI2C ch2 transmitting DMA request (I2C2ATXDMAREQ) Others: Reserved
27	-	0	R	Read as "0".
26	UPDN15	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.
25	OUTSEL15	0	R/W	Output trigger selection 0: No edge is detected. 1: An edge is detected.
24	EN15	0	R/W	Trigger output control 0: Disabled 1: Enabled
23	-	0	R	Read as "0".
22:20	INSEL14[2:0]	000	R/W	Input trigger selection (MDMAC unit A ch14) 000: T32A ch5 DMA request at match A1 register (T32A05DMAREQCMPA1) 001: T32A ch5 DMA request at match C1 register (T32A05DMAREQCMPC1) 010: T32A ch5 DMA request at capture A0 register (T32A05DMAREQCAPA0) 011: T32A ch5 DMA request at capture C0 register (T32A05DMAREQCAPC0) Others: Reserved
19	-	0	R	Read as "0".
18	UPDN14	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.
17	OUTSEL14	0	R/W	Output trigger selection 0: No edge is detected. 1: An edge is detected.
16	EN14	0	R/W	Trigger output control 0: Disabled 1: Enabled
15	-	0	R	Read as "0".

Bit	Bit symbol	After reset	Type	Description
14:12	INSEL13[2:0]	000	R/W	Input trigger selection (MDMAC unit A ch13) 000: T32A ch4 DMA request at match B1 register (T32A04DMAREQCMPB1) 001: T32A ch4 DMA request at capture B0 register (T32A04DMAREQCAPB0) 010: UART ch1 transmission DMA request (UART1TX_DMAREQ) 011: I2C ch1 transmitting DMA request (I2C1TXDMAREQ) 100: EI2C ch1 transmitting DMA request (I2C1ATXDMAREQ) Others: Reserved
11	-	0	R	Read as "0".
10	UPDN13	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.
9	OUTSEL13	0	R/W	Output trigger selection 0: No edge is detected. 1: An edge is detected.
8	EN13	0	R/W	Trigger output control 0: Disabled 1: Enabled
7	-	0	R	Read as "0".
6:4	INSEL12[2:0]	000	R/W	Input trigger selection (MDMAC unit A ch12) 000: T32A ch4 DMA request at match A1 register (T32A04DMAREQCMPA1) 001: T32A ch4 DMA request at match C1 register (T32A04DMAREQCMPC1) 010: T32A ch4 DMA request at capture A0 register (T32A04DMAREQCAPA0) 011: T32A ch4 DMA request at capture C0 register (T32A04DMAREQCAPC0) Others: Reserved
3	-	0	R	Read as "0".
2	UPDN12	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.
1	OUTSEL12	0	R/W	Output trigger selection 0: No edge is detected. 1: An edge is detected.
0	EN12	0	R/W	Trigger output control 0: Disabled 1: Enabled

2.2.4.5. *[TSEL0CR4]* (Control Register 4)

Bit	Bit symbol	After reset	Type	Description
31	-	0	R	Read as "0".
30:28	INSEL19[2:0]	000	R/W	Input trigger selection (MDMAC unit A ch19) 000: T32A ch7 DMA request at match B1 register (T32A07DMAREQCMPB1) 001: T32A ch7 DMA request at capture B0 register (T32A07DMAREQCAPB0) 010: UART ch2 reception DMA request (UART2RX_DMAREQ) 011: ADC unit A general purpose trigger DMA request (ADATRG_DMAREQ) 100: TSSI ch0 receive DMA request (TSSI0RXDMAREQ) Others: Reserved
27	-	0	R	Read as "0".
26	UPDN19	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.
25	OUTSEL19	0	R/W	Output trigger selection 0: No edge is detected. 1: An edge is detected.
24	EN19	0	R/W	Trigger output control 0: Disabled 1: Enabled
23	-	0	R	Read as "0".
22:20	INSEL18[2:0]	000	R/W	Input trigger selection (MDMAC unit A ch18) 000: T32A ch7 DMA request at match A1 register (T32A07DMAREQCMPA1) 001: T32A ch7 DMA request at match C1 register (T32A07DMAREQCMPC1) 010: T32A ch7 DMA request at capture A0 register (T32A07DMAREQCAPA0) 011: T32A ch7 DMA request at capture C0 register (T32A07DMAREQCAPC0) 100: UART ch0 reception DMA request (UART0RX_DMAREQ) Others: Reserved
19	-	0	R	Read as "0".
18	UPDN18	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.
17	OUTSEL18	0	R/W	Output trigger selection 0: No edge is detected. 1: An edge is detected.
16	EN18	0	R/W	Trigger output control 0: Disabled 1: Enabled
15	-	0	R	Read as "0".

Bit	Bit symbol	After reset	Type	Description
14:12	INSEL17[2:0]	000	R/W	Input trigger selection (MDMAC unit A ch17) 000: T32A ch6 DMA request at match B1 register (T32A06DMAREQCMPB1) 001: T32A ch6 DMA request at capture B0 register (T32A06DMAREQCAPB0) 010: FUART ch0 reception DMA request (FUART0RX_DMAREQ) 011: I2C ch2 receiving DMA request (I2C2RXDMAREQ) 100: EI2C ch2 receiving DMA request (I2C2ARXDMAREQ) Others: Reserved
11	-	0	R	Read as "0".
10	UPDN17	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.
9	OUTSEL17	0	R/W	Output trigger selection 0: No edge is detected. 1: An edge is detected.
8	EN17	0	R/W	Trigger output control 0: Disabled 1: Enabled
7	-	0	R	Read as "0".
6:4	INSEL16[2:0]	000	R/W	Input trigger selection (MDMAC unit A ch16) 000: T32A ch6 DMA request at match A1 register (T32A06DMAREQCMPA1) 001: T32A ch6 DMA request at match C1 register (T32A06DMAREQCMPC1) 010: T32A ch6 DMA request at capture A0 register (T32A06DMAREQCAPA0) 011: T32A ch6 DMA request at capture C0 register (T32A06DMAREQCAPC0) Others: Reserved
3	-	0	R	Read as "0".
2	UPDN16	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.
1	OUTSEL16	0	R/W	Output trigger selection 0: No edge is detected. 1: An edge is detected.
0	EN16	0	R/W	Trigger output control 0: Disabled 1: Enabled

2.2.4.6. *[TSEL0CR5]* (Control Register 5)

Bit	Bit symbol	After reset	Type	Description
31	-	0	R	Read as "0".
30:28	INSEL23[2:0]	000	R/W	Input trigger selection (MDMAC unit A ch23) 000: T32A ch9 DMA request at match B1 register (T32A09DMAREQCMPB1) 001: T32A ch9 DMA request at capture B0 register (T32A09DMAREQCAPB0) 010: T32A ch9 DMA request at capture A1 register (T32A09DMAREQCAPA1) 011: T32A ch9 DMA request at capture B1 register (T32A09DMAREQCAPB1) 100: UART ch1 transmission DMA request (UART1TX_DMAREQ) Others: Reserved
27	-	0	R	Read as "0".
26	UPDN23	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.
25	OUTSEL23	0	R/W	Output trigger selection 0: No edge is detected. 1: An edge is detected.
24	EN23	0	R/W	Trigger output control 0: Disabled 1: Enabled
23	-	0	R	Read as "0".
22:20	INSEL22[2:0]	000	R/W	Input trigger selection (MDMAC unit A ch22) 000: T32A ch9 DMA request at match A1 register (T32A09DMAREQCMPA1) 001: T32A ch9 DMA request at match C1 register (T32A09DMAREQCMPC1) 010: T32A ch9 DMA request at capture A0 register (T32A09DMAREQCAPA0) 011: T32A ch9 DMA request at capture C0 register (T32A09DMAREQCAPC0) 100: UART ch1 reception DMA request (UART1RX_DMAREQ) Others: Reserved
19	-	0	R	Read as "0".
18	UPDN22	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.
17	OUTSEL22	0	R/W	Output trigger selection 0: No edge is detected. 1: An edge is detected.
16	EN22	0	R/W	Trigger output control 0: Disabled 1: Enabled
15	-	0	R	Read as "0".

Bit	Bit symbol	After reset	Type	Description
14:12	INSEL21[2:0]	000	R/W	Input trigger selection (MDMAC unit A ch21) 000: T32A ch8 DMA request at match B1 register (T32A08DMAREQCMPB1) 001: T32A ch8 DMA request at capture B0 register (T32A08DMAREQCAPB0) 010: UART ch2 transmission DMA request (UART2TX_DMAREQ) 011: ADC unit A Highest priority DMA request (ADAHP_DMAREQ) 100: TSSI ch0 transmit DMA request (TSSI0TXDMAREQ) Others: Reserved
11	-	0	R	Read as "0".
10	UPDN21	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.
9	OUTSEL21	0	R/W	Output trigger selection 0: No edge is detected. 1: An edge is detected.
8	EN21	0	R/W	Trigger output control 0: Disabled 1: Enabled
7	-	0	R	Read as "0".
6:4	INSEL20[2:0]	000	R/W	Input trigger selection (MDMAC unit A ch20) 000: T32A ch8 DMA request at match A1 register (T32A08DMAREQCMPA1) 001: T32A ch8 DMA request at match C1 register (T32A08DMAREQCMPC1) 010: T32A ch8 DMA request at capture A0 register (T32A08DMAREQCAPA0) 011: T32A ch8 DMA request at capture C0 register (T32A08DMAREQCAPC0) 100: UART ch0 transmission DMA request (UART0TX_DMAREQ) Others: Reserved
3	-	0	R	Read as "0".
2	UPDN20	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.
1	OUTSEL20	0	R/W	Output trigger selection 0: No edge is detected. 1: An edge is detected.
0	EN20	0	R/W	Trigger output control 0: Disabled 1: Enabled

2.2.4.7. *[TSEL0CR6]* (Control Register 6)

Bit	Bit symbol	After reset	Type	Description
31	-	0	R	Read as "0".
30:28	INSEL27[2:0]	000	R/W	Input trigger selection (MDMAC unit A ch27) 000: T32A ch11 DMA request at match B1 register (T32A11DMAREQCMPB1) 001: T32A ch11 DMA request at capture B0 register (T32A11DMAREQCAPB0) 010: T32A ch11 DMA request at capture A1 register (T32A11DMAREQCAPA1) 011: T32A ch11 DMA request at capture B1 register (T32A11DMAREQCAPB1) 100: TSSI ch1 transmit DMA request (TSSI1TXDMAREQ) Others: Reserved
27	-	0	R	Read as "0".
26	UPDN27	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.
25	OUTSEL27	0	R/W	Output trigger selection 0: No edge is detected. 1: An edge is detected.
24	EN27	0	R/W	Trigger output control 0: Disabled 1: Enabled
23	-	0	R	Read as "0".
22:20	INSEL26[2:0]	000	R/W	Input trigger selection (MDMAC unit A ch26) 000: T32A ch11 DMA request at match A1 register (T32A11DMAREQCMPA1) 001: T32A ch11 DMA request at match C1 register (T32A11DMAREQCMPC1) 010: T32A ch11 DMA request at capture A0 register (T32A11DMAREQCAPA0) 011: T32A ch11 DMA request at capture C0 register (T32A11DMAREQCAPC0) 100: TSSI ch1 receive DMA request (TSSI1RXDMAREQ) Others: Reserved
19	-	0	R	Read as "0".
18	UPDN26	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.
17	OUTSEL26	0	R/W	Output trigger selection 0: No edge is detected. 1: An edge is detected.
16	EN26	0	R/W	Trigger output control 0: Disabled 1: Enabled
15	-	0	R	Read as "0".

Bit	Bit symbol	After reset	Type	Description
14:12	INSEL25[2:0]	000	R/W	Input trigger selection (MDMAC unit A ch25) 000: T32A ch10 DMA request at match B1 register (T32A10DMAREQCMPB1) 001: T32A ch10 DMA request at capture B0 register (T32A10DMAREQCAPB0) 010: T32A ch10 DMA request at capture A1 register (T32A10DMAREQCAPA1) 011: T32A ch10 DMA request at capture B1 register (T32A10DMAREQCAPB1) 100: UART ch2 transmission DMA request (UART2TX_DMAREQ) Others: Reserved
11	-	0	R	Read as "0".
10	UPDN25	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.
9	OUTSEL25	0	R/W	Output trigger selection 0: No edge is detected. 1: An edge is detected.
8	EN25	0	R/W	Trigger output control 0: Disabled 1: Enabled
7	-	0	R	Read as "0".
6:4	INSEL24[2:0]	000	R/W	Input trigger selection (MDMAC unit A ch24) 000: T32A ch10 DMA request at match A1 register (T32A10DMAREQCMPA1) 001: T32A ch10 DMA request at match C1 register (T32A10DMAREQCMPC1) 010: T32A ch10 DMA request at capture A0 register (T32A10DMAREQCAPA0) 011: T32A ch10 DMA request at capture C0 register (T32A10DMAREQCAPC0) 100: UART ch2 reception DMA request (UART2RX_DMAREQ) Others: Reserved
3	-	0	R	Read as "0".
2	UPDN24	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.
1	OUTSEL24	0	R/W	Output trigger selection 0: No edge is detected. 1: An edge is detected.
0	EN24	0	R/W	Trigger output control 0: Disabled 1: Enabled

2.2.4.8. *[TSEL0CR7]* (Control Register 7)

Bit	Bit symbol	After reset	Type	Description
31	-	0	R	Read as "0".
30:28	INSEL31[2:0]	000	R/W	Input trigger selection (MDMAC unit A ch31) 000: T32A ch13 DMA request at match B1 register (T32A13DMAREQCMPB1) 001: UART ch5 transmission DMA request (UART5TX_DMAREQ) 010: PT3 pin (TRGIN2) 011: T32A ch13 DMA request at capture B0 register (T32A13DMAREQCAPB0) Others: Reserved When "010" (TRGIN2) is selected, <OUTSEL31> should be set to "1" (An edge is detected.).
27	-	0	R	Read as "0".
26	UPDN31	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.
25	OUTSEL31	0	R/W	Output trigger selection 0: No edge is detected. 1: An edge is detected.
24	EN31	0	R/W	Trigger output control 0: Disabled 1: Enabled
23	-	0	R	Read as "0".
22:20	INSEL30[2:0]	000	R/W	Input trigger selection (MDMAC unit A ch30) 000: T32A ch13 DMA request at match A1 register (T32A13DMAREQCMPA1) 001: T32A ch13 DMA request at match C1 register (T32A13DMAREQCMPC1) 010: UART ch5 reception DMA request (UART5RX_DMAREQ) 011: T32A ch13 DMA request at capture A0 register (T32A13DMAREQCAPA0) 100: T32A ch13 DMA request at capture C0 register (T32A13DMAREQCAPC0) Others: Reserved
19	-	0	R	Read as "0".
18	UPDN30	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.
17	OUTSEL30	0	R/W	Output trigger selection 0: No edge is detected. 1: An edge is detected.
16	EN30	0	R/W	Trigger output control 0: Disabled 1: Enabled
15	-	0	R	Read as "0".

Bit	Bit symbol	After reset	Type	Description
14:12	INSEL29[2:0]	000	R/W	Input trigger selection (MDMAC unit A ch29) 000: T32A ch12 DMA request at match B1 register (T32A12DMAREQCMPB1) 001: UART ch3 transmission DMA request (UART3TX_DMAREQ) 010: A-PMD ch0 PWM interrupt (INTPWM0) 011: T32A ch12 DMA request at capture B0 register (T32A12DMAREQCAPB0) Others: Reserved
11	-	0	R	Read as "0".
10	UPDN29	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.
9	OUTSEL29	0	R/W	Output trigger selection 0: No edge is detected. 1: An edge is detected.
8	EN29	0	R/W	Trigger output control 0: Disabled 1: Enabled
7	-	0	R	Read as "0".
6:4	INSEL28[2:0]	000	R/W	Input trigger selection (MDMAC unit A ch28) 000: T32A ch12 DMA request at match A1 register (T32A12DMAREQCMPA1) 001: T32A ch12 DMA request at match C1 register (T32A12DMAREQCMPC1) 010: UART ch3 reception DMA request (UART3RX_DMAREQ) 011: T32A ch12 DMA request at capture A0 register (T32A12DMAREQCAPA0) 100: T32A ch12 DMA request at capture C0 register (T32A12DMAREQCAPC0) Others: Reserved
3	-	0	R	Read as "0".
2	UPDN28	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.
1	OUTSEL28	0	R/W	Output trigger selection 0: No edge is detected. 1: An edge is detected.
0	EN28	0	R/W	Trigger output control 0: Disabled 1: Enabled

2.2.4.9. *[TSEL0CR8]* (Control Register 8)

Bit	Bit symbol	After reset	Type	Description
31	-	0	R	Read as "0".
30:28	INSEL35[2:0]	000	R/W	Input trigger selection (T32A ch13 timer A) 000: RMC ch0 trigger output (RMC0TRG) 001: T32A ch2 timer register A0 match trigger (T32A02TRGOUTCMPA0) Others: Reserved. When "000" (RMC ch0 trigger output) is selected, <OUTSEL35> should be set to "1" (An edge is detected.).
27	-	0	R	Read as "0".
26	UPDN35	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.
25	OUTSEL35	0	R/W	Output trigger selection 0: No edge is detected. 1: An edge is detected.
24	EN35	0	R/W	Trigger output control 0: Disabled 1: Enabled
23	-	0	R	Read as "0".
22:20	INSEL34[2:0]	000	R/W	Input trigger selection (T32A ch8 timer A) 000: ELOSC low speed clock (fs) 001: Reserved 010: TSPI ch8 transmit complete trigger (TSPI8TXDEND) 011: TSPI ch8 receive complete trigger (TSPI8RXDEND) 100: Reserved 101: Reserved 110: Reserved 111: Reserved When "000" (ELOSC low speed clock) is selected, <OUTSEL34> should be set to "1" (An edge is detected.).
19	-	0	R	Read as "0".
18	UPDN34	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.
17	OUTSEL34	0	R/W	Output trigger selection 0: No edge is detected. 1: An edge is detected.
16	EN34	0	R/W	Trigger output control 0: Disabled 1: Enabled
15	-	0	R	Read as "0".

Bit	Bit symbol	After reset	Type	Description
14:12	INSEL33[2:0]	000	R/W	Input trigger selection (ADC unit A) 000: A-PMD ch0 ADC synchronous trigger output 0 (PMD0TRG0) 001: A-PMD ch0 ADC synchronous trigger output 1 (PMD0TRG1) 010: A-PMD ch0 ADC synchronous trigger output 2 (PMD0TRG2) 011: A-PMD ch0 ADC synchronous trigger output 3 (PMD0TRG3) 100: Reserved 101: Reserved 110: TRGSEL37 output (TRGSEL0OUT37) 111: TRGSEL38 output (TRGSEL0OUT38)
11	-	0	R	Read as "0".
10	UPDN33	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.
9	OUTSEL33	0	R/W	Output trigger selection 0: No edge is detected. 1: An edge is detected.
8	EN33	0	R/W	Trigger output control 0: Disabled 1: Enabled
7	-	0	R	Read as "0".
6:4	INSEL32[2:0]	000	R/W	Input trigger selection (ADC unit A) 000: A-PMD ch0 ADC synchronous trigger output 0 (PMD0TRG0) 001: A-PMD ch0 ADC synchronous trigger output 1 (PMD0TRG1) 010: A-PMD ch0 ADC synchronous trigger output 2 (PMD0TRG2) 011: A-PMD ch0 ADC synchronous trigger output 3 (PMD0TRG3) 100: Reserved 101: Reserved 110: TRGSEL37 output (TRGSEL0OUT37) 111: TRGSEL38 output (TRGSEL0OUT38)
3	-	0	R	Read as "0".
2	UPDN32	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.
1	OUTSEL32	0	R/W	Output trigger selection 0: No edge is detected. 1: An edge is detected.
0	EN32	0	R/W	Trigger output control 0: Disabled 1: Enabled

2.2.4.10. *[TSEL0CR9]* (Control Register 9)

Bit	Bit symbol	After reset	Type	Description
31	-	0	R	Read as "0".
30:28	INSEL39[2:0]	000	R/W	Input trigger selection (T32A ch5 timer A) 000: T32A ch9 timer register A0 match trigger (T32A09TRGOUTCMPA0) 001: T32A ch13 timer register A0 match trigger (T32A13TRGOUTCMPA0) 010: TSPI ch5 transmit complete trigger (TSPI5TXDEND) 011: UART ch5 transmission completion trigger (UART5TXTRG) Others: Reserved
27	-	0	R	Read as "0".
26	UPDN39	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.
25	OUTSEL39	0	R/W	Output trigger selection 0: No edge is detected. 1: An edge is detected.
24	EN39	0	R/W	Trigger output control 0: Disabled 1: Enabled
23	-	0	R	Read as "0".
22:20	INSEL38[2:0]	000	R/W	Input trigger selection (TRGSEL32, TRGSEL33) 000: T32A ch9 timer register A1 match trigger (T32A09TRGOUTCMPA1) 001: T32A ch9 timer register B1 match trigger (T32A09TRGOUTCMPB1) 010: T32A ch10 timer register A1 match trigger (T32A10TRGOUTCMPA1) 011: T32A ch10 timer register B1 match trigger (T32A10TRGOUTCMPB1) 100: T32A ch11 timer register A1 match trigger (T32A11TRGOUTCMPA1) 101: T32A ch11 timer register B1 match trigger (T32A11TRGOUTCMPB1) 110: PG3 pin (TRGIN0) 111: PL7 pin (TRGIN1) When "110" (TRGIN0) or "111" (TRGIN1) is selected, <OUTSEL38> should be set to "1" (An edge is detected.).
19	-	0	R	Read as "0".
18	UPDN38	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.
17	OUTSEL38	0	R/W	Output trigger selection 0: No edge is detected. 1: An edge is detected.
16	EN38	0	R/W	Trigger output control 0: Disabled 1: Enabled

Bit	Bit symbol	After reset	Type	Description
15	-	0	R	Read as "0".
14:12	INSEL37[2:0]	000	R/W	Input trigger selection (TRGSEL32, TRGSEL33) 000: T32A ch9 timer register A1 match trigger (T32A09TRGOUTCMPA1) 001: T32A ch9 timer register B1 match trigger (T32A09TRGOUTCMPB1) 010: T32A ch10 timer register A1 match trigger (T32A10TRGOUTCMPA1) 011: T32A ch10 timer register B1 match trigger (T32A10TRGOUTCMPB1) 100: T32A ch11 timer register A1 match trigger (T32A11TRGOUTCMPA1) 101: T32A ch11 timer register B1 match trigger (T32A11TRGOUTCMPB1) 110: PG3 pin (TRGIN0) 111: PL7 pin (TRGIN1) When "110" (TRGIN0) or "111" (TRGIN1) is selected, <OUTSEL37> should be set to "1" (An edge is detected.).
11	-	0	R	Read as "0".
10	UPDN37	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.
9	OUTSEL37	0	R/W	Output trigger selection 0: No edge is detected. 1: An edge is detected.
8	EN37	0	R/W	Trigger output control 0: Disabled 1: Enabled
7	-	0	R	Read as "0".
6:4	INSEL36[2:0]	000	R/W	Input trigger selection (T32A ch13 timer B) 000: RMC ch1 trigger output (RMC1TRG) 001: T32A ch2 timer register A0 match trigger (T32A02TRGOUTCMPA0) Others: Reserved When "000" (RMC ch1 trigger output) is selected, <OUTSEL36> should be set to "1" (An edge is detected.).
3	-	0	R	Read as "0".
2	UPDN36	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.
1	OUTSEL36	0	R/W	Output trigger selection 0: No edge is detected. 1: An edge is detected.
0	EN36	0	R/W	Trigger output control 0: Disabled 1: Enabled

2.2.4.11. *[TSEL0CR10]* (Control Register 10)

Bit	Bit symbol	After reset	Type	Description
31	-	0	R	Read as "0".
30:28	INSEL43[2:0]	000	R/W	Input trigger selection (T32A ch7 timer A) 000: T32A ch11 timer register A0 match trigger (T32A11TRGOUTCMPA0) 001: T32A ch13 timer register B0 match trigger (T32A13TRGOUTCMPB0) 010: TSPI ch7 transmit complete trigger (TSPI7TXDEND) Others: Reserved
27	-	0	R	Read as "0".
26	UPDN43	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.
25	OUTSEL43	0	R/W	Output trigger selection 0: No edge is detected. 1: An edge is detected.
24	EN43	0	R/W	Trigger output control 0: Disabled 1: Enabled
23	-	0	R	Read as "0".
22:20	INSEL42[2:0]	000	R/W	Input trigger selection (T32A ch6 timer B) 000: T32A ch10 timer register A0 match trigger (T32A10TRGOUTCMPA0) 001: T32A ch13 timer register B0 match trigger (T32A13TRGOUTCMPB0) 010: TSPI ch6 receive complete trigger (TSPI6RXDEND) 011: T32A ch6 timer register A0 match trigger (T32A06TRGOUTCMPA0) Others: Reserved
19	-	0	R	Read as "0".
18	UPDN42	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.
17	OUTSEL42	0	R/W	Output trigger selection 0: No edge is detected. 1: An edge is detected.
16	EN42	0	R/W	Trigger output control 0: Disabled 1: Enabled
15	-	0	R	Read as "0".
14:12	INSEL41[2:0]	000	R/W	Input trigger selection (T32A ch6 timer A) 000: T32A ch10 timer register A0 match trigger (T32A10TRGOUTCMPA0) 001: T32A ch13 timer register B0 match trigger (T32A13TRGOUTCMPB0) 010: TSPI ch6 transmit complete trigger (TSPI6TXDEND) Others: Reserved
11	-	0	R	Read as "0".

Bit	Bit symbol	After reset	Type	Description
10	UPDN41	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.
9	OUTSEL41	0	R/W	Output trigger selection 0: No edge is detected. 1: An edge is detected.
8	EN41	0	R/W	Trigger output control 0: Disabled 1: Enabled
7	-	0	R	Read as "0".
6:4	INSEL40[2:0]	000	R/W	Input trigger selection (T32A ch5 timer B) 000: T32A ch9 timer register A0 match trigger (T32A09TRGOUTCMPA0) 001: T32A ch13 timer register A0 match trigger (T32A13TRGOUTCMPA0) 010: TSPI ch5 receive complete trigger (TSPI5RXDEND) 011: UART ch5 reception completion trigger (UART5RXTRG) 100: T32A ch5 timer register A0 match trigger (T32A05TRGOUTCMPA0) Others: Reserved
3	-	0	R	Read as "0".
2	UPDN40	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.
1	OUTSEL40	0	R/W	Output trigger selection 0: No edge is detected. 1: An edge is detected.
0	EN40	0	R/W	Trigger output control 0: Disabled 1: Enabled

2.2.4.12. *[TSEL0CR11]* (Control Register 11)

Bit	Bit symbol	After reset	Type	Description
31	-	0	R	Read as "0".
30:28	INSEL47[2:0]	000	R/W	Input trigger selection (T32A ch0 timer B) 000: TSPI ch0 receive complete trigger (TSPI0RXDEND) 001: UART ch0 reception completion trigger (UART0RXTRG) 010: T32A ch12 timer register A0 match trigger (T32A12TRGOUTCMPA0) 011: T32A ch0 timer register A0 match trigger (T32A00TRGOUTCMPA0) Others: Reserved
27	-	0	R	Read as "0".
26	UPDN47	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.
25	OUTSEL47	0	R/W	Output trigger selection 0: No edge is detected. 1: An edge is detected.
24	EN47	0	R/W	Trigger output control 0: Disabled 1: Enabled
23	-	0	R	Read as "0".
22:20	INSEL46[2:0]	000	R/W	Input trigger selection (T32A ch0 timer A) 000: TSPI ch0 transmit complete trigger (TSPI0TXDEND) 001: UART ch0 transmission completion trigger (UART0TXTRG) 010: T32A ch12 timer register A0 match trigger (T32A12TRGOUTCMPA0) Others: Reserved
19	-	0	R	Read as "0".
18	UPDN46	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.
17	OUTSEL46	0	R/W	Output trigger selection 0: No edge is detected. 1: An edge is detected.
16	EN46	0	R/W	Trigger output control 0: Disabled 1: Enabled
15	-	0	R	Read as "0".
14:12	INSEL45[2:0]	000	R/W	Input trigger selection (T32A ch8 timer B) 000: T32A ch4 timer B output (T32A04OUTB) 001: T32A ch8 timer A output (T32A08OUTA) Others: Reserved
11	-	0	R	Read as "0".
10	UPDN45	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.

Bit	Bit symbol	After reset	Type	Description
9	OUTSEL45	0	R/W	Output trigger selection 0: No edge is detected. 1: An edge is detected.
8	EN45	0	R/W	Trigger output control 0: Disabled 1: Enabled
7	-	0	R	Read as "0".
6:4	INSEL44[2:0]	000	R/W	Input trigger selection (T32A ch7 timer B) 000: T32A ch11 timer register A0 match trigger (T32A11TRGOUTCMPA0) 001: T32A ch13 timer register B0 match trigger (T32A13TRGOUTCMPB0) 010: TSPI ch7 receive complete trigger (TSPI7RXDEND) 011: T32A ch7 timer register A0 match trigger (T32A07TRGOUTCMPA0) Others: Reserved
3	-	0	R	Read as "0".
2	UPDN44	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.
1	OUTSEL44	0	R/W	Output trigger selection 0: No edge is detected. 1: An edge is detected.
0	EN44	0	R/W	Trigger output control 0: Disabled 1: Enabled

2.2.4.13. *[TSEL0CR12]* (Control Register 12)

Bit	Bit symbol	After reset	Type	Description
31	-	0	R	Read as "0".
30:28	INSEL51[2:0]	000	R/W	Input trigger selection (T32A ch2 timer B) 000: TSPI ch2 receive complete trigger (TSPI2RXDEND) 001: UART ch2 reception completion trigger (UART2RXTRG) 010: T32A ch12 timer register B0 match trigger (T32A12TRGOUTCMPB0) 011: T32A ch2 timer register A0 match trigger (T32A02TRGOUTCMPA0) Others: Reserved
27	-	0	R	Read as "0".
26	UPDN51	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.
25	OUTSEL51	0	R/W	Output trigger selection 0: No edge is detected. 1: An edge is detected.
24	EN51	0	R/W	Trigger output control 0: Disabled 1: Enabled
23	-	0	R	Read as "0".
22:20	INSEL50[2:0]	000	R/W	Input trigger selection (T32A ch2 timer A) 000: TSPI ch2 transmit complete trigger (TSPI2TXDEND) 001: UART ch2 transmission completion trigger (UART2TXTRG) 010: T32A ch12 timer register B0 match trigger (T32A12TRGOUTCMPB0) Others: Reserved
19	-	0	R	Read as "0".
18	UPDN50	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.
17	OUTSEL50	0	R/W	Output trigger selection 0: No edge is detected. 1: An edge is detected.
16	EN50	0	R/W	Trigger output control 0: Disabled 1: Enabled
15	-	0	R	Read as "0".
14:12	INSEL49[2:0]	000	R/W	Input trigger selection (T32A ch1 timer B) 000: TSPI ch1 receive complete trigger (TSPI1RXDEND) 001: UART ch1 reception completion trigger (UART1RXTRG) 010: T32A ch12 timer register A0 match trigger (T32A12TRGOUTCMPA0) 011: T32A ch1 timer register A0 match trigger (T32A01TRGOUTCMPA0) Others: Reserved

Bit	Bit symbol	After reset	Type	Description
11	-	0	R	Read as "0".
10	UPDN49	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.
9	OUTSEL49	0	R/W	Output trigger selection 0: No edge is detected. 1: An edge is detected.
8	EN49	0	R/W	Trigger output control 0: Disabled 1: Enabled
7	-	0	R	Read as "0".
6:4	INSEL48[2:0]	000	R/W	Input trigger selection (T32A ch1 timer A) 000: TSPI ch1 transmit complete trigger (TSPI1TXDEND) 001: UART ch1 transmission completion trigger (UART1TXTRG) 010: T32A ch12 timer register A0 match trigger (T32A12TRGOUTCMPA0) Others: Reserved
3	-	0	R	Read as "0".
2	UPDN48	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.
1	OUTSEL48	0	R/W	Output trigger selection 0: No edge is detected. 1: An edge is detected.
0	EN48	0	R/W	Trigger output control 0: Disabled 1: Enabled

2.2.4.14. *[TSEL0CR13]* (Control Register 13)

Bit	Bit symbol	After reset	Type	Description
31	-	0	R	Read as "0".
30:28	INSEL55[2:0]	000	R/W	Input trigger selection (T32A ch4 timer B) 000: TSPI ch4 receive complete trigger (TSPI4RXDEND) 001: T32A ch13 timer register A0 match trigger (T32A13TRGOUTCMPA0) 010: UART ch4 reception completion trigger (UART4RXTRG) 011: T32A ch4 timer register A0 match trigger (T32A04TRGOUTCMPA0) Others: Reserved
27	-	0	R	Read as "0".
26	UPDN55	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.
25	OUTSEL55	0	R/W	Output trigger selection 0: No edge is detected. 1: An edge is detected.
24	EN55	0	R/W	Trigger output control 0: Disabled 1: Enabled
23	-	0	R	Read as "0".
22:20	INSEL54[2:0]	000	R/W	Input trigger selection (T32A ch4 timer A) 000: TSPI ch4 transmit complete trigger (TSPI4TXDEND) 001: T32A ch13 timer register A0 match trigger (T32A13TRGOUTCMPA0) 010: UART ch4 transmission completion trigger (UART4TXTRG) Others: Reserved
19	-	0	R	Read as "0".
18	UPDN54	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.
17	OUTSEL54	0	R/W	Output trigger selection 0: No edge is detected. 1: An edge is detected.
16	EN54	0	R/W	Trigger output control 0: Disabled 1: Enabled
15	-	0	R	Read as "0".
14:12	INSEL53[2:0]	000	R/W	Input trigger selection (T32A ch3 timer B) 000: TSPI ch3 receive complete trigger (TSPI3RXDEND) 001: T32A ch12 timer register B0 match trigger (T32A12TRGOUTCMPB0) 010: UART ch3 reception completion trigger (UART3RXTRG) 011: T32A ch3 timer register A0 match trigger (T32A03TRGOUTCMPA0) Others: Reserved

Bit	Bit symbol	After reset	Type	Description
11	-	0	R	Read as "0".
10	UPDN53	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.
9	OUTSEL53	0	R/W	Output trigger selection 0: No edge is detected. 1: An edge is detected.
8	EN53	0	R/W	Trigger output control 0: Disabled 1: Enabled
7	-	0	R	Read as "0".
6:4	INSEL52[2:0]	000	R/W	Input trigger selection (T32A ch3 timer A) 000: TSPI ch3 transmit complete trigger (TSPI3TXDEND) 001: T32A ch12 timer register B0 match trigger (T32A12TRGOUTCMPB0) 010: UART ch3 transmission completion trigger (UART3TXTRG) Others: Reserved
3	-	0	R	Read as "0".
2	UPDN52	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.
1	OUTSEL52	0	R/W	Output trigger selection 0: No edge is detected. 1: An edge is detected.
0	EN52	0	R/W	Trigger output control 0: Disabled 1: Enabled

2.2.4.15. *[TSEL0CR14]* (Control Register 14)

Bit	Bit symbol	After reset	Type	Description
31:7	-	0	R	Read as "0".
6:4	INSEL56[2:0]	000	R/W	Input trigger selection (FIR) 000: I2S ch0 receive FIFO threshold signal (I2S0RXFIFOTH) 001: I2S ch0 transmit FIFO threshold signal (I2S0TXFIFOTH) 010: I2S ch1 receive FIFO threshold signal (I2S1RXFIFOTH) 011: I2S ch1 transmit FIFO threshold signal (I2S1TXFIFOTH) Others: Reserved
3	-	0	R	Read as "0".
2	UPDN56	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.
1	OUTSEL56	0	R/W	Output trigger selection 0: No edge is detected. 1: An edge is detected.
0	EN56	0	R/W	Trigger output control 0: Disabled 1: Enabled

2.3. Clock Selective Watchdog Timer (SIWDT)

2.3.1. Built-in Channel

The built-in channel for each product is shown in the following table.

Table 2.11 SIWDT Built-in Channel

Product	SIWDT built-in channel (✓: Available, -: N/A)
	Channel 0
M4GR	✓
M4GQ	✓
M4GN	✓

2.3.2. Count Clock

The SIWDT can select the clock to count. The clocks which can be selected are shown in the following table.

Table 2.12 SIWDT Count Clock

Clock	Signal name	Selection
System clock	fsysm	Selected by the ***[SIWD0MOD]***<WDCLS> register.
Internal high-speed oscillator 1 clock (Note1)	f_{IHOSC1}	
Internal high-speed oscillator 2 clock (Note2)	f_{IHOSC2}	

Note1: The oscillation control register is ***[CGOSCCR]***<IHOSC1EN>.

Note2: The oscillation control register is ***[RLMLOSCCR]***<POSCEN>.

2.3.3. Oscillation Clock Protection Function

When the internal high-speed oscillator 2 (f_{IHOSC2}) is selected, it is possible to forbid rewriting of the internal high-speed oscillator 2.

Table 2.13 SIWDT Control Output

Control Output	Signal name	Remarks
The protection signal of an internal high-speed oscillator 2 oscillation control bit (***[RLMLOSCCR]***<POSCEN>)	OSCPRO	The protection function is set by the ***[SIWD0OSCCR]***<OSCPRO> register.

2.4. Oscillation Frequency Detection Circuit (OFD)

2.4.1. Built-in List

The following table shows the built-in list for each product.

Table 2.14 OFD Built-in List

Product	Built-in OFD (✓:Available, -: N/A)
M4GR	✓
M4GQ	✓
M4GN	✓

2.4.2. Reference Clock

The OFD operates with the clock in the following table as the reference clock.

Table 2.15 OFD Reference Clock

Reference clock	Signal name	Divide value
Internal high-speed oscillator 2	f_{IHOSC2}	128

Note: The oscillation control register is ***[RLMLOSCCR]***<POSCEN>.

2.4.3. Clock for Detection

The OFD selects clock to detect from the following table.

Table 2.16 OFD Clock for Detection

Detection target clock		Signal name
Input signal	External high-speed oscillator clock	f_{EHOSC}
	Clock selected by the ***[CGOSCCR]***<OSCSEL> and ***[CGPLL0SEL]***<PLL0SEL>	fc

2.5. Debug Interface

2.5.1. Debug Interface Pin List for Each Product

Table 2.17 Debug Interface Pin List

Debug interface pin		Port	Product table (✓: Available, -: N/A)		
			M4GR	M4GQ	M4GN
SWDIO	I/O	PH4	✓	✓	✓
TMS	Input				
SWCLK	Input	PH5	✓	✓	✓
TCK	Input				
SWV	Output	PH6	✓	✓	✓
TDO	Output				
TDI	Input	PH3	✓	✓	✓
TRST_N	Input	PH7	✓	✓	✓
TRACECLK	Output	PG6	✓	✓	✓
TRACEDATA0	Output	PG7	✓	✓	✓
TRACEDATA1	Output	PH0	✓	✓	✓
TRACEDATA2	Output	PH1	✓	✓	✓
TRACEDATA3	Output	PH2	✓	✓	✓

2.5.2. Divided Ratio for Trace Clock

Table 2.18 Divided Ratio for Trace Clock (TRACECLK)

Source clock	Divided ratio	Output
fsysh	1/4	TRACECLK

2.6. Non-break Debug Interface (NBDIF)

2.6.1. Built-in List

The following table shows the built-in list for each product.

Table 2.19 NBDIF Built-in List

Product	Built-in NBDIF (✓:Available, -: N/A)
M4GR	✓
M4GQ	✓
M4GN	✓

2.6.2. Non-break Debug Interface Pin List for Each Product

Table 2.20 Non-break Debug Interface Pin List

Non-break debug interface pin		Port	Product table (✓: Available, -: N/A)		
			M4GR	M4GQ	M4GN
NBDCLK	Input	PG6	✓	✓	✓
NBDDATA0	I/O	PG7	✓	✓	✓
NBDDATA1	I/O	PH0	✓	✓	✓
NBDDATA2	I/O	PH1	✓	✓	✓
NBDDATA3	I/O	PH2	✓	✓	✓
NBDSYNC	Input	PH3	✓	✓	✓

2.7. Flash Memory

2.7.1. Clock for Programming and Erasing

As for flash memory, the clock of the following table is used for programming/erasing of the code flash or the data flash.

Table 2.21 Clock for Programming and Erasing

Clock for programming and erasing
f_{IHOSC1}

Note: The oscillation control register is ***[CGOSCCR]***<IHOSC1EN>.

2.7.2. Block Configuration of Code Flash Memory for Each Product

The code flash memory differs in the block configuration with the product, as shown in the following table.

Table 2.22 Block Configuration of Code Flash Memory for Each Product

Area	Block name		TMPM4GRF20FG TMPM4GRF20XBG TMPM4GQF20FG TMPM4GQF20XBG TMPM4GNF20FG	TMPM4GRF15FG TMPM4GRF15XBG TMPM4GQF15FG TMPM4GQF15XBG TMPM4GNF15FG	TMPM4GRF10FG TMPM4GRF10XBG TMPM4GQF10FG TMPM4GQF10XBG TMPM4GNF10FG	TMPM4GRFDFG TMPM4GRFDXBG TMPM4GQFDFG TMPM4GQFDXBG TMPM4GNFDFG	Block size (KB)
0	Block0	PG0	✓	✓	✓	✓	4
		PG1	✓	✓	✓	✓	4
		PG2	✓	✓	✓	✓	4
		PG3	✓	✓	✓	✓	4
		PG4	✓	✓	✓	✓	4
		PG5	✓	✓	✓	✓	4
		PG6	✓	✓	✓	✓	4
		PG7	✓	✓	✓	✓	4
	Block1		✓	✓	✓	✓	32
	Block2		✓	✓	✓	✓	32
	Block3		✓	✓	✓	✓	32
	Block4		✓	✓	✓	✓	32
	Block5		✓	✓	✓	✓	32
	Block6		✓	✓	✓	✓	32
	Block7		✓	✓	✓	✓	32
	Block8		✓	✓	✓	✓	32
	Block9		✓	✓	✓	✓	32
	Block10		✓	✓	✓	✓	32
	Block11		✓	✓	✓	✓	32
	Block12		✓	✓	✓	✓	32
	Block13		✓	✓	✓	✓	32
	Block14		✓	✓	✓	✓	32
	Block15		✓	✓	✓	✓	32

	Block16	✓	✓	✓	-	32
	Block17	✓	✓	✓	-	32
	Block18	✓	✓	✓	-	32
	Block19	✓	✓	✓	-	32
	Block20	✓	✓	✓	-	32
	Block21	✓	✓	✓	-	32
	Block22	✓	✓	✓	-	32
	Block23	✓	✓	✓	-	32
	Block24	✓	✓	✓	-	32
	Block25	✓	✓	✓	-	32
	Block26	✓	✓	✓	-	32
	Block27	✓	✓	✓	-	32
	Block28	✓	✓	✓	-	32
	Block29	✓	✓	✓	-	32
	Block30	✓	✓	✓	-	32
	Block31	✓	✓	✓	-	32
1	Block32	✓	✓	-	-	32
	Block33	✓	✓	-	-	32
	Block34	✓	✓	-	-	32
	Block35	✓	✓	-	-	32
	Block36	✓	✓	-	-	32
	Block37	✓	✓	-	-	32
	Block38	✓	✓	-	-	32
	Block39	✓	✓	-	-	32
	Block40	✓	✓	-	-	32
	Block41	✓	✓	-	-	32
	Block42	✓	✓	-	-	32
	Block43	✓	✓	-	-	32
	Block44	✓	✓	-	-	32
	Block45	✓	✓	-	-	32
	Block46	✓	✓	-	-	32
	Block47	✓	✓	-	-	32
	Block48	✓	-	-	-	32
	Block49	✓	-	-	-	32
	Block50	✓	-	-	-	32
	Block51	✓	-	-	-	32
	Block52	✓	-	-	-	32
	Block53	✓	-	-	-	32
	Block54	✓	-	-	-	32
	Block55	✓	-	-	-	32
	Block56	✓	-	-	-	32
	Block57	✓	-	-	-	32
	Block58	✓	-	-	-	32
	Block59	✓	-	-	-	32
	Block60	✓	-	-	-	32
	Block61	✓	-	-	-	32
	Block62	✓	-	-	-	32
	Block63	✓	-	-	-	32

Note: ✓: Available, -: N/A

2.7.3. Block Configuration of Data Flash Memory for Each Product

The data flash memory differs in the block configuration with the product, as shown in the following table.

Table 2.23 Block Configuration of Data Flash Memory for Each Product

Area	Block name	TMPM4GRF20FG TMPM4GRF20XBG TMPM4GQF20FG TMPM4GQF20XBG TMPM4GNF20FG	TMPM4GRF15FG TMPM4GRF15XBG TMPM4GQF15FG TMPM4GQF15XBG TMPM4GNF15FG	TMPM4GRF10FG TMPM4GRF10XBG TMPM4GQF10FG TMPM4GQF10XBG TMPM4GNF10FG	TMPM4GRFDFG TMPM4GRFDXBG TMPM4GQFDFG TMPM4GQFDXBG TMPM4GNFDFG	Block size (KB)
4	Block0	✓	✓	✓	✓	4
	Block1	✓	✓	✓	✓	4
	Block2	✓	✓	✓	✓	4
	Block3	✓	✓	✓	✓	4
	Block4	✓	✓	✓	✓	4
	Block5	✓	✓	✓	✓	4
	Block6	✓	✓	✓	✓	4
	Block7	✓	✓	✓	✓	4

Note: ✓: Available, -: N/A

2.7.4. Macro Code at ID-Read

Macro codes are as following.

Table 2.24 Macro code at ID-Read

Code	ID[15:0]
Macro code (Code Flash memory)	0x0403
Macro code (Data Flash memory)	0x0404

2.7.5. Resource in Single Boot Mode

The peripheral function of the following table is used in single boot mode.

Table 2.25 Resource in Single Boot Mode

Peripheral function	Channel	Pin name
BOOT	-	PY4 (BOOT_N)
UART	ch0	PH4/PH5 (UT0TXDA/UT0RXD),
T32A	ch0	-

The single boot mode can be set by reset release from the RESET_N pin or from the power on reset (POR).

The end address in which RAM transmission is possible by the RAM loader command should use the following table.

Table 2.26 End Address in which RAM Transmission is Possible

Product name	End address in which RAM transmission is possible
TMPM4GRF20FG, TMPM4GRF20XBG, TMPM4GQF20FG, TMPM4GQF20XBG, TMPM4GNF20FG TMPM4GRF15FG, TMPM4GRF15XBG, TMPM4GQF15FG, TMPM4GQF15XBG, TMPM4GNF15FG TMPM4GRF10FG, TMPM4GRF10XBG, TMPM4GQF10FG, TMPM4GQF10XBG, TMPM4GNF10FG	0x20027FFF
TMPM4GRFDFG, TMPM4GRFDXBG, TMPM4GQFDFG, TMPM4GQFDXBG, TMPM4GNFDFG	0x2001FFFF

2.8. High-speed DMA Controller (HDMAC)

2.8.1. Built-in Unit

The built-in unit for each product is shown in the following table.

Table 2.27 HDMAC Built-in Unit

Product	HDMAC built-in unit (✓: Available, -: N/A)	
	unit A	unit B
M4GR	✓	✓
M4GQ	✓	✓
M4GN	✓	✓

2.8.2. DMA Transfer Request List

The DMA transfer request list is shown in the following tables.
"-" in the tables does not have an applicable function.

Table 2.28 HDMAC DMA Transfer Request List: Unit A

Channel	Single transfer request		Burst transfer request	
		Signal name		Signal name
ch0	TSPI ch0 receive DMA request	TSPI0RX_DMA	TSPI ch0 receive DMA request	TSPI0RX_DMA
ch1	TSPI ch0 transmit DMA request	TSPI0TX_DMA	TSPI ch0 transmit DMA request	TSPI0TX_DMA
ch2	TSPI ch2 receive DMA request	TSPI2RX_DMA	TSPI ch2 receive DMA request	TSPI2RX_DMA
ch3	TSPI ch2 transmit DMA request	TSPI2TX_DMA	TSPI ch2 transmit DMA request	TSPI2TX_DMA
ch4	TSPI ch4 receive DMA request	TSPI4RX_DMA	TSPI ch4 receive DMA request	TSPI4RX_DMA
ch5	TSPI ch4 transmit DMA request	TSPI4TX_DMA	TSPI ch4 transmit DMA request	TSPI4TX_DMA
ch6	-	-	SMIF ch0 interrupt	INTSMI0
ch7	-	-	-	-
ch8	-	-	-	-
ch9	-	-	-	-
ch10	-	-	-	-
ch11	-	-	-	-
ch12	-	-	-	-
ch13	-	-	-	-
ch14	-	-	-	-
ch15	-	-	PB1 (HDMAREQA) Trigger input (Note)	PB1 (HDMAREQA)

Note: When requesting DMA transfer, input "High" level for 2 or more cycles with the high speed system clock (fsysh) to the PB1 port.

Table 2.29 HDMAC DMA Transfer Request List: Unit B

Channel	Single transfer request		Burst transfer request	
		Signal name		Signal name
ch0	TSPI ch1 receive DMA request	TSPI1RX_DMA	TSPI ch1 receive DMA request	TSPI1RX_DMA
ch1	TSPI ch1 transmit DMA request	TSPI1TX_DMA	TSPI ch1 transmit DMA request	TSPI1TX_DMA
ch2	TSPI ch3 receive DMA request	TSPI3RX_DMA	TSPI ch3 receive DMA request	TSPI3RX_DMA
ch3	TSPI ch3 transmit DMA request	TSPI3TX_DMA	TSPI ch3 transmit DMA request	TSPI3TX_DMA
ch4	TSPI ch5 receive DMA request (Note1)	TSPI5RX_DMA	TSPI ch5 receive DMA request (Note1)	TSPI5RX_DMA
ch5	TSPI ch5 transmit DMA request (Note1)	TSPI5TX_DMA	TSPI ch5 transmit DMA request (Note1)	TSPI5TX_DMA
ch6	-	-	-	-
ch7	-	-	-	-
ch8	-	-	-	-
ch9	-	-	-	-
ch10	-	-	-	-
ch11	-	-	-	-
ch12	-	-	-	-
ch13	-	-	-	-
ch14	-	-	-	-
ch15	-	-	PK1 (HDMAREQB) Trigger input (Note2)	PK1 (HDMAREQB)

Note1: M4GN does not have this function.

Note2: When requesting DMA transfer, input "High" level for 2 or more cycles with the high-speed system clock (fsysh) to the PK1 port.

2.9. Multi-Function DMA Controller (MDMAC)

2.9.1. Built-in Unit

The built-in unit for each product is shown in the following table.

Table 2.30 MDMAC Built-in Unit

Product	MDMAC built-in unit (✓: Available, -: N/A)
	unit A
M4GR	✓
M4GQ	✓
M4GN	✓

2.9.2. DMA Transfer Request List

The DMAC transfer request list is shown in the following tables.

The channel which has a register name in the trigger selector column of the tables should select the request used by a trigger selector. "-" in the tables does not have an applicable function.

Table 2.31 MDMAC DMA Transfer Request List: Unit A (1/5)

Channel	Single transfer request			Burst transfer request	
	Trigger selector		Signal name		Signal name
ch0	***[TSEL0CR0]*** <INSEL0[2:0]> (Note1)	TSPI ch6 receive DMA request (Note2)	TSPI6RX_DMA	-	-
		UART ch4 reception DMA request (Note2)	UART4RX_DMAREQ		
		I2C ch3 receiving DMA request (Note2)	I2C3RXDMAREQ		
		T32A ch0 DMA request at capture A0 register	T32A00DMAREQCAPA0		
		EI2C ch3 receiving DMA request (Note2)	I2C3ARXDMAREQ		
		I2S ch0 receiving DMA request	I2S0RXDMAREQ		
ch1	***[TSEL0CR0]*** <INSEL1[2:0]> (Note1)	TSPI ch6 transmit DMA request (Note2)	TSPI6TX_DMA	-	-
		UART ch4 transmission DMA request (Note2)	UART4TX_DMAREQ		
		I2C ch3 transmitting DMA request (Note2)	I2C3TXDMAREQ		
		T32A ch0 DMA request at capture C0 register	T32A00DMAREQCAPC0		
		EI2C ch3 transmitting DMA request (Note2)	I2C3ATXDMAREQ		
		I2S ch0 transmitting DMA request	I2S0TXDMAREQ		
ch2	***[TSEL0CR0]*** <INSEL2[2:0]> (Note1)	TSPI ch7 receive DMA request (Note2)	TSPI7RX_DMA	-	-
		FUART ch1 reception DMA request (Note2)	FUART1RX_DMAREQ		
		I2C ch4 receiving DMA request (Note2)	I2C4RXDMAREQ		
		EI2C ch4 receiving DMA request (Note2)	I2C4ARXDMAREQ		
		I2S ch1 receiving DMA request	I2S1RXDMAREQ		
ch3	***[TSEL0CR0]*** <INSEL3[2:0]> (Note1)	TSPI ch7 transmit DMA request (Note2)	TSPI7TX_DMA	-	-
		FUART ch1 transmission DMA request (Note2)	FUART1TX_DMAREQ		
		I2C ch4 transmitting DMA request (Note2)	I2C4TXDMAREQ		
		EI2C ch4 transmitting DMA request (Note2)	I2C4ATXDMAREQ		
		I2S ch1 transmitting DMA request	I2S1TXDMAREQ		

Note1: Ch0 to ch31 select the trigger source of a DMA transfer request by a trigger selector. Please refer to "2.2. Trigger Selector (TRGSEL)" for the detailed connection.

Note2: M4GN does not have this function.

Table 2.32 MDMAC DMA Transfer Request List: Unit A (2/5)

Channel	Single transfer request			Burst transfer request	
	Trigger selector		Signal name		Signal name
ch4	***[TSEL0CR1]*** <INSEL4[2:0]> (Note1)	TSPI ch8 receive DMA request (Note2) (Note3)	TSPI8RX_DMA	-	-
		T32A ch0 DMA request at match A1 register	T32A00DMAREQCMPA1		
		T32A ch0 DMA request at match C1 register	T32A00DMAREQCMPC1		
		FIR input data write request	FIRDATAWRDMAREQ		
ch5	***[TSEL0CR1]*** <INSEL5[2:0]> (Note1)	TSPI ch8 transmit DMA request (Note2) (Note3)	TSPI8TX_DMA	-	-
		T32A ch0 DMA request at match B1 register	T32A00DMAREQCMPB1		
		T32A ch0 DMA request at capture B0 register	T32A00DMAREQCAPB0		
		FIR arithmetic result data read request	FIRDATARDDMAREQ		
ch6	***[TSEL0CR1]*** <INSEL6[2:0]> (Note1)	T32A ch1 DMA request at match A1 register	T32A01DMAREQCMPA1	-	-
		T32A ch1 DMA request at match C1 register	T32A01DMAREQCMPC1		
		T32A ch1 DMA request at capture A0 register	T32A01DMAREQCAPA0		
		T32A ch1 DMA request at capture C0 register	T32A01DMAREQCAPC0		
ch7	***[TSEL0CR1]*** <INSEL7[2:0]> (Note1)	T32A ch1 DMA request at match B1 register	T32A01DMAREQCMPB1	-	-
		T32A ch1 DMA request at capture B0 register	T32A01DMAREQCAPB0		
		UART ch0 reception DMA request	UART0RX_DMAREQ		
		I2C ch0 receiving DMA request	I2C0RXDMAREQ		
		EI2C ch0 receiving DMA request	I2C0ARXDMAREQ		
ch8	***[TSEL0CR2]*** <INSEL8[2:0]> (Note1)	T32A ch2 DMA request at match A1 register	T32A02DMAREQCMPA1	-	-
		T32A ch2 DMA request at match C1 register	T32A02DMAREQCMPC1		
		T32A ch2 DMA request at capture A0 register	T32A02DMAREQCAPA0		
		T32A ch2 DMA request at capture C0 register	T32A02DMAREQCAPC0		
ch9	***[TSEL0CR2]*** <INSEL9[2:0]> (Note1)	T32A ch2 DMA request at match B1 register	T32A02DMAREQCMPB1	-	-
		T32A ch2 DMA request at capture B0 register	T32A02DMAREQCAPB0		
		UART ch0 transmission DMA request	UART0TX_DMAREQ		
		I2C ch0 transmitting DMA request	I2C0TXDMAREQ		
		EI2C ch0 transmitting DMA request	I2C0ATXDMAREQ		
ch10	***[TSEL0CR2]*** <INSEL10[2:0]> (Note1)	T32A ch3 DMA request at match A1 register	T32A03DMAREQCMPA1	-	-
		T32A ch3 DMA request at match C1 register	T32A03DMAREQCMPC1		
		T32A ch3 DMA request at capture A0 register	T32A03DMAREQCAPA0		
		T32A ch3 DMA request at capture C0 register	T32A03DMAREQCAPC0		
ch11	***[TSEL0CR2]*** <INSEL11[2:0]> (Note1)	T32A ch3 DMA request at match B1 register	T32A03DMAREQCMPB1	-	-
		T32A ch3 DMA request at capture B0 register	T32A03DMAREQCAPB0		
		UART ch1 reception DMA request	UART1RX_DMAREQ		
		I2C ch1 receiving DMA request	I2C1RXDMAREQ		
		EI2C ch1 receiving DMA request	I2C1ARXDMAREQ		

Note1: Ch0 to ch31 select the trigger source of a DMA transfer request by a trigger selector. Please refer to "2.2. Trigger Selector (TRGSEL)" for the detailed connection.

Note2: M4GQ does not have this function.

Note3: M4GN does not have this function.

Table 2.33 MDMAC DMA Transfer Request List: Unit A: unit A (3/5)

Channel	Single transfer request			Burst transfer request	
	Trigger selector		Signal name		Signal name
ch12	***[TSEL0CR3]*** <INSEL12[2:0]> (Note)	T32A ch4 DMA request at match A1 register	T32A04DMAREQCMPA1	-	-
		T32A ch4 DMA request at match C1 register	T32A04DMAREQCMPC1		
		T32A ch4 DMA request at capture A0 register	T32A04DMAREQCAPA0		
		T32A ch4 DMA request at capture C0 register	T32A04DMAREQCAPC0		
ch13	***[TSEL0CR3]*** <INSEL13[2:0]> (Note)	T32A ch4 DMA request at match B1 register	T32A04DMAREQCMPB1	-	-
		T32A ch4 DMA request at capture B0 register	T32A04DMAREQCAPB0		
		UART ch1 transmission DMA request	UART1TX_DMAREQ		
		I2C ch1 transmitting DMA request	I2C1TXDMAREQ		
		EI2C ch1 transmitting DMA request	I2C1ATXDMAREQ		
ch14	***[TSEL0CR3]*** <INSEL14[2:0]> (Note)	T32A ch5 DMA request at match A1 register	T32A05DMAREQCMPA1	-	-
		T32A ch5 DMA request at match C1 register	T32A05DMAREQCMPC1		
		T32A ch5 DMA request at capture A0 register	T32A05DMAREQCAPA0		
		T32A ch5 DMA request at capture C0 register	T32A05DMAREQCAPC0		
ch15	***[TSEL0CR3]*** <INSEL15[2:0]> (Note)	T32A ch5 DMA request at match B1 register	T32A05DMAREQCMPB1	-	-
		T32A ch5 DMA request at capture B0 register	T32A05DMAREQCAPB0		
		FUART ch0 transmission DMA request	FUART0TX_DMAREQ		
		I2C ch2 transmitting DMA request	I2C2TXDMAREQ		
		EI2C ch2 transmitting DMA request	I2C2ATXDMAREQ		
ch16	***[TSEL0CR4]*** <INSEL16[2:0]> (Note)	T32A ch6 DMA request at match A1 register	T32A06DMAREQCMPA1	-	-
		T32A ch6 DMA request at match C1 register	T32A06DMAREQCMPC1		
		T32A ch6 DMA request at capture A0 register	T32A06DMAREQCAPA0		
		T32A ch6 DMA request at capture C0 register	T32A06DMAREQCAPC0		
ch17	***[TSEL0CR4]*** <INSEL17[2:0]> (Note)	T32A ch6 DMA request at match B1 register	T32A06DMAREQCMPB1	-	-
		T32A ch6 DMA request at capture B0 register	T32A06DMAREQCAPB0		
		FUART ch0 reception DMA request	FUART0RX_DMAREQ		
		I2C ch2 receiving DMA request	I2C2RXDMAREQ		
		EI2C ch2 receiving DMA request	I2C2ARXDMAREQ		
ch18	***[TSEL0CR4]*** <INSEL18[2:0]> (Note)	T32A ch7 DMA request at match A1 register	T32A07DMAREQCMPA1	-	-
		T32A ch7 DMA request at match C1 register	T32A07DMAREQCMPC1		
		T32A ch7 DMA request at capture A0 register	T32A07DMAREQCAPA0		
		T32A ch7 DMA request at capture C0 register	T32A07DMAREQCAPC0		
		UART ch0 reception DMA request	UART0RX_DMAREQ		
ch19	***[TSEL0CR4]*** <INSEL19[2:0]> (Note)	T32A ch7 DMA request at match B1 register	T32A07DMAREQCMPB1	-	-
		T32A ch7 DMA request at capture B0 register	T32A07DMAREQCAPB0		
		UART ch2 reception DMA request	UART2RX_DMAREQ		
		ADC unit A general purpose trigger DMA request	ADATRG_DMAREQ		
		TSSI ch0 receive DMA request	TSSI0RXDMAREQ		

Note: Ch0 to ch31 select the trigger source of a DMA transfer request by a trigger selector. Please refer to "2.2. Trigger Selector (TRGSEL)" for the detailed connection.

Table 2.34 MDMAC DMA Transfer Request List: Unit A (4/5)

Channel	Single transfer request			Burst transfer request	
	Trigger selector		Signal name		Signal name
ch20	***[TSEL0CR5]*** <INSEL20[2:0]> (Note1)	T32A ch8 DMA request at match A1 register	T32A08DMAREQCMPA1	-	-
		T32A ch8 DMA request at match C1 register	T32A08DMAREQCMPC1		
		T32A ch8 DMA request at capture A0 register	T32A08DMAREQCAPA0		
		T32A ch8 DMA request at capture C0 register	T32A08DMAREQCAPC0		
		UART ch0 transmission DMA request	UART0TX_DMAREQ		
ch21	***[TSEL0CR5]*** <INSEL21[2:0]> (Note1)	T32A ch8 DMA request at match B1 register	T32A08DMAREQCMPB1	-	-
		T32A ch8 DMA request at capture B0 register	T32A08DMAREQCAPB0		
		UART ch2 transmission DMA request	UART2TX_DMAREQ		
		ADC unit A Highest priority DMA request	ADAHP_DMAREQ		
		TSSI ch0 transmit DMA request	TSSI0TXDMAREQ		
ch22	***[TSEL0CR5]*** <INSEL22[2:0]> (Note1)	T32A ch9 DMA request at match A1 register	T32A09DMAREQCMPA1	-	-
		T32A ch9 DMA request at match C1 register	T32A09DMAREQCMPC1		
		T32A ch9 DMA request at capture A0 register	T32A09DMAREQCAPA0		
		T32A ch9 DMA request at capture C0 register	T32A09DMAREQCAPC0		
		UART ch1 reception DMA request	UART1RX_DMAREQ		
ch23	***[TSEL0CR5]*** <INSEL23[2:0]> (Note1)	T32A ch9 DMA request at match B1 register	T32A09DMAREQCMPB1	-	-
		T32A ch9 DMA request at capture B0 register	T32A09DMAREQCAPB0		
		T32A ch9 DMA request at capture A1 register	T32A09DMAREQCAPA1		
		T32A ch9 DMA request at capture B1 register	T32A09DMAREQCAPB1		
		UART ch1 transmission DMA request	UART1TX_DMAREQ		
ch24	***[TSEL0CR6]*** <INSEL24[2:0]> (Note1)	T32A ch10 DMA request at match A1 register	T32A10DMAREQCMPA1	-	-
		T32A ch10 DMA request at match C1 register	T32A10DMAREQCMPC1		
		T32A ch10 DMA request at capture A0 register	T32A10DMAREQCAPA0		
		T32A ch10 DMA request at capture C0 register	T32A10DMAREQCAPC0		
		UART ch2 reception DMA request	UART2RX_DMAREQ		
ch25	***[TSEL0CR6]*** <INSEL25[2:0]> (Note1)	T32A ch10 DMA request at match B1 register	T32A10DMAREQCMPB1	-	-
		T32A ch10 DMA request at capture B0 register	T32A10DMAREQCAPB0		
		T32A ch10 DMA request at capture A1 register	T32A10DMAREQCAPA1		
		T32A ch10 DMA request at capture B1 register	T32A10DMAREQCAPB1		
		UART ch2 transmission DMA request	UART2TX_DMAREQ		
ch26	***[TSEL0CR6]*** <INSEL26[2:0]> (Note1)	T32A ch11 DMA request at match A1 register	T32A11DMAREQCMPA1	-	-
		T32A ch11 DMA request at match C1 register	T32A11DMAREQCMPC1		
		T32A ch11 DMA request at capture A0 register	T32A11DMAREQCAPA0		
		T32A ch11 DMA request at capture C0 register	T32A11DMAREQCAPC0		
		TSSI ch1 receive DMA request (Note2) (Note3)	TSSI1RXDMAREQ		
ch27	***[TSEL0CR6]*** <INSEL27[2:0]> (Note1)	T32A ch11 DMA request at match B1 register	T32A11DMAREQCMPB1	-	-
		T32A ch11 DMA request at capture B0 register	T32A11DMAREQCAPB0		
		T32A ch11 DMA request at capture A1 register	T32A11DMAREQCAPA1		
		T32A ch11 DMA request at capture B1 register	T32A11DMAREQCAPB1		
		TSSI ch1 transmit DMA request (Note2) (Note3)	TSSI1TXDMAREQ		

Note1: Ch0 to ch31 select the trigger source of a DMA transfer request by a trigger selector. Please refer to "2.2. Trigger Selector (TRGSEL)" for the detailed connection.

Note2: M4GQ does not have this function.

Note3: M4GN does not have this function.

Table 2.35 MDMAC DMA Transfer Request List: Unit A (5/5)

Channel	Single transfer request			Burst transfer request	
	Trigger Selector		Signal name		Signal name
ch28	***[TSEL0CR7]*** <INSEL28[2:0]> (Note1)	T32A ch12 DMA request at match A1 register	T32A12DMAREQCMPA1	-	-
		T32A ch12 DMA request at match C1 register	T32A12DMAREQCMPC1		
		UART ch3 reception DMA request (Note3)	UART3RX_DMAREQ		
		T32A ch12 DMA request at capture A0 register	T32A12DMAREQCAPA0		
		T32A ch12 DMA request at capture C0 register	T32A12DMAREQCAPC0		
ch29	***[TSEL0CR7]*** <INSEL29[2:0]> (Note1)	T32A ch12 DMA request at match B1 register	T32A12DMAREQCMPB1	-	-
		UART ch3 transmission DMA request (Note3)	UART3TX_DMAREQ		
		A-PMD ch0 PWM interrupt	INTPWM0		
		T32A ch12 DMA request at capture B0 register	T32A12DMAREQCAPB0		
ch30	***[TSEL0CR7]*** <INSEL30[2:0]> (Note1)	T32A ch13 DMA request at match A1 register	T32A13DMAREQCMPA1	-	-
		T32A ch13 DMA request at match C1 register	T32A13DMAREQCMPC1		
		UART ch5 reception DMA request (Note2) (Note3)	UART5RX_DMAREQ		
		T32A ch13 DMA request at capture A0 register	T32A13DMAREQCAPA0		
		T32A ch13 DMA request at capture C0 register	T32A13DMAREQCAPC0		
ch31	***[TSEL0CR7]*** <INSEL31[2:0]> (Note1)	T32A ch13 DMA request at match B1 register	T32A13DMAREQCMPB1	-	-
		UART ch5 transmission DMA request (Note2) (Note3)	UART5TX_DMAREQ		
		PT3 pin (TRGIN2) (Note4)	TRGIN2		
		T32A ch13 DMA request at capture B0 register	T32A13DMAREQCAPB0		

Note1: Ch0 to ch31 select the trigger source of a DMA transfer request by a trigger selector. Please refer to "2.2. Trigger Selector (TRGSEL)" for the detailed connection.

Note2: M4GQ product does not have this function.

Note3: M4GN product does not have this function.

Note4: When requesting DMA transfer, input "High" level for 3 or more cycles with the middle speed system clock (fsysm) to the PT3 port.

2.10. Advanced Programmable Motor Control Circuit (A-PMD)

2.10.1. Built-in Channel

The built-in channel for each product is shown in the following table.

Table 2.36 A-PMD Built-in Channel

Product	A-PMD built-in channel (✓: Available, -: N/A)
	ch0
M4GR	✓
M4GQ	✓
M4GN	✓

2.10.2. System Clock

The A-PMD operates with the clock in the following table as the system clock.

Table 2.37 A-PMD System Clock

Clock	Signal name
System clock	fsysm

2.10.3. Function Pin and Port

The functional pin is assigned to the following ports.

Table 2.38 A-PMD Function Pin and Port

Channel	Function pin		Port	Product table (✓: Available, -: N/A)		
				M4GR	M4GQ	M4GN
ch0	XO0	Output	PD1	✓	✓	✓
			PV1	✓	✓	-
	YO0	Output	PD3	✓	✓	✓
			PV3	✓	✓	-
	ZO0	Output	PD5	✓	✓	✓
			PV5	✓	✓	-
	UO0	Output	PD0	✓	✓	✓
			PV0	✓	✓	-
	VO0	Output	PD2	✓	✓	✓
			PV2	✓	✓	-
	WO0	Output	PD4	✓	✓	✓
			PV4	✓	✓	-
	EMG0	Input	PD6	✓	✓	✓
			PV6	✓	✓	-
	OVV0	Input	PD7	✓	✓	✓
			PV7	✓	✓	-
	PMD0DBG	Output	-	-	-	-

2.10.4. DMA Request

The A-PMD has the DMA request shown in the following table.

Table 2.39 A-PMD DMA request

Channel	Request		Trigger Selector	DMA request channel (MDMAC unit A)		
		Signal name			Single transfer	Burst transfer
ch0	PWM interrupt	INTPWM0	[TSEL0CR7] <INSEL29[2:0]>	29	✓	-

Note: ✓: Available, -: Not available.

2.10.5. Internal Signal Connection Specification

Some internal signals are connected to a peripheral function in the A-PMD, as shown in the following table.

2.10.5.1. ADC Connection

Table 2.40 A-PMD Internal Signal Connection Specification: Output

Channel	Function output		Output destination		
		Signal name	Trigger Selector		Signal name
ch0	ADC synchronous trigger output 0	PMD0TRG0	***[TSEL0CR8]*** <INSEL32[2:0]>	ADC unit A highest priority trigger input	ADAHPTRGIN
	ADC synchronous trigger output 1	PMD0TRG1			
	ADC synchronous trigger output 2	PMD0TRG2			
	ADC synchronous trigger output 3	PMD0TRG3			
	ADC synchronous trigger output 0	PMD0TRG0	***[TSEL0CR8]*** <INSEL33[2:0]>	ADC unit A general purpose trigger input	ADATRGIN
	ADC synchronous trigger output 1	PMD0TRG1			
	ADC synchronous trigger output 2	PMD0TRG2			
	ADC synchronous trigger output 3	PMD0TRG3			

2.11. 12-bit Analog to Digital Converter (ADC)

2.11.1. Built-in Unit

The built-in unit for each product is shown in the following table.

Table 2.41 ADC Built-in Unit

Product	ADC built-in unit (✓: Available, -: N/A)
	unit A
M4GR	✓
M4GQ	✓
M4GN	✓

2.11.2. Function Pin and Port

The functional pin is assigned to the port of the following table.

Table 2.42 ADC Function Pin and Port

Unit	Input channel	Function pin	Port	Product table (✓: Available, -: N/A)		
				M4GR	M4GQ	M4GN
Unit A	ch0	AINA00	PN0	✓	✓	✓
	ch1	AINA01	PN1	✓	✓	✓
	ch2	AINA02	PN2	✓	✓	✓
	ch3	AINA03	PN3	✓	✓	✓
	ch4	AINA04	PN4	✓	✓	✓
	ch5	AINA05	PN5	✓	✓	✓
	ch6	AINA06	PN6	✓	✓	✓
	ch7	AINA07	PN7	✓	✓	✓
	ch8	AINA08	PP0	✓	✓	✓
	ch9	AINA09	PP1	✓	✓	✓
	ch10	AINA10	PP2	✓	✓	✓
	ch11	AINA11	PP3	✓	✓	✓
	ch12	AINA12	PP4	✓	✓	✓
	ch13	AINA13	PP5	✓	✓	✓
	ch14	AINA14	PP6	✓	✓	✓
	ch15	AINA15	PP7	✓	✓	✓
	ch16	AINA16	PR0	✓	✓	-
	ch17	AINA17	PR1	✓	✓	-
	ch18	AINA18	PR2	✓	✓	-
	ch19	AINA19	PR3	✓	✓	-
	ch20	AINA20	PR4	✓	✓	-
	ch21	AINA21	PR5	✓	✓	-
	ch22	AINA22	PR6	✓	✓	-
	ch23	AINA23	PR7	✓	✓	-

Note: For inputs of ADAHPTRGIN and ADATRGIN, refer to "2.11.8.1. Start Trigger Connection Specification".

2.11.3. Analog Reference Pins

The analog reference pins (VREFHA, VREFLA) are shared with the analog power supply pins (AVDD3, AVSS).

2.11.4. Conversion Clock for ADC

The ADC uses the conversion clock shown in the following table.

Table 2.43 Conversion Clock for ADC

Clock
ADCLK

2.11.5. Setting of Mode Setting Register 2

Set the mode setting register 2 (***[ADxMOD2]***) according to the following table.

Table 2.44 ADC Mode Setting Register 2 Setting

Register name	Value
[ADxMOD2]<MOD2[31:0]>	0x00000000

2.11.6. DMA Request

The ADC has the DMA request shown in the following table.

Table 2.45 ADC DMA Request

Unit	Request		Trigger Selector	DMA request channel (MDMAC unit A)		
		Signal name			Single transfer	Burst transfer
Unit A	General purpose trigger DMA request	ADATRG_DMAREQ	***[TSEL0CR4]*** <INSEL19[2:0]>	19	✓	-
	Highest priority DMA request	ADAHP_DMAREQ	***[TSEL0CR5]*** <INSEL21[2:0]>	21	✓	-

Note: ✓: Available, -: Not available

2.11.7. Monitoring Functions

The monitoring function supports the functions shown in the following table.

Table 2.46 ADC Monitoring Functions Support

Function	Function support (✓: Supported, -: Not supported)
Monitor Function 0	✓
Monitor Function 1	✓
Monitor Function 2	-
Monitor Function 3	-

2.11.8. Internal Signal Connection Specification

2.11.8.1. Start Trigger Connection Specification

The ADC has a conversion function by the trigger signal.

Table 2.47 ADC start-up Trigger Connection Specification

Unit	Trigger input		Start-up trigger		
		Signal name	Trigger Selector		Signal name
Unit A	Highest priority trigger input	ADAHPTRGIN	***[TSEL0CR8]*** <INSEL32[2:0]> (Note)	ADC synchronous trigger output 0	PMD0TRG0
				ADC synchronous trigger output 1	PMD0TRG1
				ADC synchronous trigger output 2	PMD0TRG2
				ADC synchronous trigger output 3	PMD0TRG3
				TRGSEL 37 output	TRGSEL0OUT37
				TRGSEL 38 output	TRGSEL0OUT38
	General purpose trigger input	ADATRGIN	***[TSEL0CR8]*** <INSEL33[2:0]> (Note)	ADC synchronous trigger output 0	PMD0TRG0
				ADC synchronous trigger output 1	PMD0TRG1
				ADC synchronous trigger output 2	PMD0TRG2
				ADC synchronous trigger output 3	PMD0TRG3
				TRGSEL 37 output	TRGSEL0OUT37
				TRGSEL 38 output	TRGSEL0OUT38

Note: Select the trigger source of the start trigger with the trigger selector. For details on the connection destination, refer to "2.2. Trigger Selector (TRGSEL)".

Table 2.48 ADC Start-up Trigger Connection Specification (TRGSEL37 and 38 Outputs)

Connection source (Signal name)	Start-up trigger		
	Trigger selector		Signal name
TRGSEL 37 output (TRGSEL0OUT37)	***[TSEL0CR9]*** <INSEL37[2:0]> (Note)	T32A ch9 timer register A1 match trigger	T32A09TRGOUTCMPA1
		T32A ch9 timer register B1 match trigger	T32A09TRGOUTCMPB1
		T32A ch10 timer register A1 match trigger	T32A10TRGOUTCMPA1
		T32A ch10 timer register B1 match trigger	T32A10TRGOUTCMPB1
		T32A ch11 timer register A1 match trigger	T32A11TRGOUTCMPA1
		T32A ch11 timer register B1 match trigger	T32A11TRGOUTCMPB1
		PG3 pin (TRGIN0)	TRGIN0
		PL7 pin (TRGIN1)	TRGIN1
TRGSEL 38 output (TRGSEL0OUT38)	***[TSEL0CR9]*** <INSEL38[2:0]> (Note)	T32A ch9 timer register A1 match trigger	T32A09TRGOUTCMPA1
		T32A ch9 timer register B1 match trigger	T32A09TRGOUTCMPB1
		T32A ch10 timer register A1 match trigger	T32A10TRGOUTCMPA1
		T32A ch10 timer register B1 match trigger	T32A10TRGOUTCMPB1
		T32A ch11 timer register A1 match trigger	T32A11TRGOUTCMPA1
		T32A ch11 timer register B1 match trigger	T32A11TRGOUTCMPB1
		PG3 pin (TRGIN0)	TRGIN0
		PL7 pin (TRGIN1)	TRGIN1

Note: Select the trigger source of the start trigger with the trigger selector. For details on the connection destination, refer to " 2.2. Trigger Selector (TRGSEL) ".

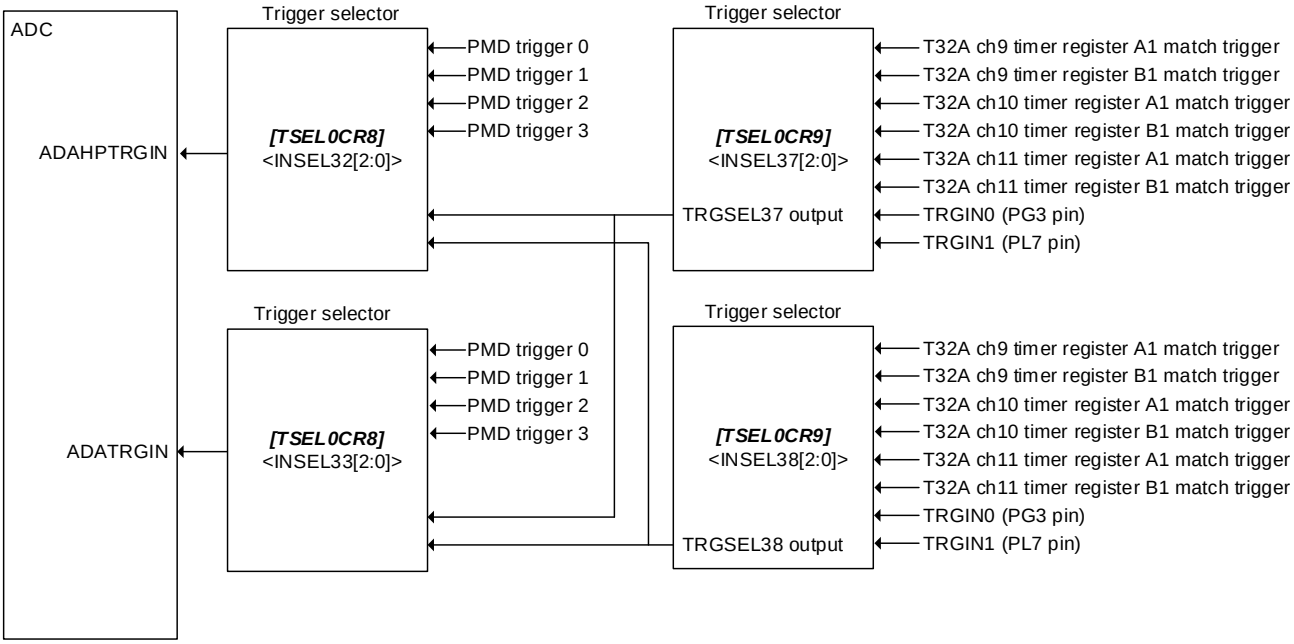

Figure 2.2 ADC Start-up Trigger Connection Diagram

2.12. 8-bit Digital to Analog Converter (DAC)

2.12.1. Built-in Channel

The built-in channel for each product is shown in the following table.

Table 2.49 DAC Built-in Channel

Product	DAC built-in channel (✓: Available, -: N/A)	
	ch0	ch1
M4GR	✓	✓
M4GQ	✓	✓
M4GN	✓	✓

2.12.2. Function Pin and Port

The functional pin is assigned to the following ports.

Table 2.50 DAC Function Pin and Port

Channel	Function pin	Port	Product table (✓: Available, -: N/A)		
			M4GR	M4GQ	M4GN
ch0	DAC0	PT0	✓	✓	✓
ch1	DAC1	PT1	✓	✓	✓

2.13. Voltage Detection Circuit (LVD)

2.13.1. Built-in List

The following table shows the built-in list for each product.

Table 2.51 LVD Built-in List

Product	Built-in LVD (✓: Available, -: N/A)
M4GR	✓
M4GQ	✓
M4GN	✓

2.13.2. LVD Detection Power Supply

The LVD monitors the power supply of the following table.

Table 2.52 LVD Detection Power Supply

LVD detection power supply	Power supply name
Power supply for digital circuit	DVDD3

2.14. 32-bit Timer Event Counter (T32A)

2.14.1. Built-in Channel

The built-in channel for each product is shown in the following table.

Table 2.53 T32A Built-in Channel

Product	T32A built-in channel (✓: Available, -: N/A)															
	ch0	ch1	ch2	ch3	ch4	ch5	ch6	ch7	ch8	ch9	ch10	ch11	ch12	ch13	ch14	ch15
M4GR	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
M4GQ	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
M4GN	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

2.14.2. Function Pin and Port

The functional pin is assigned to the port of the following tables.
Please use exclusively the same functional pin currently assigned to plurality.

Table 2.54 T32A Function Pin and Port (1/4)

Channel	Function pin		Port	Product table (✓: Available, -: N/A)		
				M4GR	M4GQ	M4GN
ch0	T32A00INA0	Input	PA0/PK0	✓/✓	✓/✓	✓/✓
	T32A00INA1	Input	PA3	✓	✓	✓
	T32A00OUTA	Output	PA1/PW1	✓/✓	✓/-	✓/-
	T32A00INB0	Input	PA3/PK1	✓/✓	✓/✓	✓/✓
	T32A00INB1	Input	PA0	✓	✓	✓
	T32A00OUTB	Output	PA2/PW0	✓/✓	✓/-	✓/-
	T32A00INC0	Input	PA0/PK0	✓/✓	✓/✓	✓/✓
	T32A00INC1	Input	PA3/PK1	✓/✓	✓/✓	✓/✓
	T32A00OUTC	Output	PA1/PW1	✓/✓	✓/-	✓/-
ch1	T32A01INA0	Input	PA4/PK6	✓/✓	✓/✓	✓/✓
	T32A01INA1	Input	PA7	✓	✓	✓
	T32A01OUTA	Output	PA5/PW2	✓/✓	✓/-	✓/-
	T32A01INB0	Input	PA7/PK7	✓/✓	✓/✓	✓/✓
	T32A01INB1	Input	PA4	✓	✓	✓
	T32A01OUTB	Output	PA6/PW3	✓/✓	✓/-	✓/-
	T32A01INC0	Input	PA4/PK6	✓/✓	✓/✓	✓/✓
	T32A01INC1	Input	PA7/PK7	✓/✓	✓/✓	✓/✓
	T32A01OUTC	Output	PA5/PW2	✓/✓	✓/-	✓/-

Table 2.55 T32A Function Pin and Port (2/4)

Channel	Function pin		Port	Product table (✓: Available, -: N/A)		
				M4GR	M4GQ	M4GN
ch2	T32A02INA0	Input	PB0 / PL0	✓/✓	✓/✓	✓/✓
	T32A02INA1	Input	PB1	✓	✓	✓
	T32A02OUTA	Output	PB2 / PG5	✓/✓	✓/✓	✓/✓
	T32A02INB0	Input	PB1 / PL3	✓/✓	✓/✓	✓/✓
	T32A02INB1	Input	PB0	✓	✓	✓
	T32A02OUTB	Output	PB3 / PG4	✓/✓	✓/✓	✓/✓
	T32A02INC0	Input	PB0 / PL0	✓/✓	✓/✓	✓/✓
	T32A02INC1	Input	PB1 / PL3	✓/✓	✓/✓	✓/✓
	T32A02OUTC	Output	PB2 / PG5	✓/✓	✓/✓	✓/✓
ch3	T32A03INA0	Input	PB6 / PJ4	✓/✓	✓/-	✓/-
	T32A03INA1	Input	PB7	✓	✓	✓
	T32A03OUTA	Output	PB4 / PT3	✓/✓	✓/✓	✓/✓
	T32A03INB0	Input	PB7 / PJ5	✓/✓	✓/-	✓/-
	T32A03INB1	Input	PB6	✓	✓	✓
	T32A03OUTB	Output	PB5 / PT5	✓/✓	✓/✓	✓/-
	T32A03INC0	Input	PB6 / PJ4	✓/✓	✓/-	✓/-
	T32A03INC1	Input	PB7 / PJ5	✓/✓	✓/-	✓/-
	T32A03OUTC	Output	PB4 / PT3	✓/✓	✓/✓	✓/✓
ch4	T32A04INA0	Input	PD0 / PP0	✓/✓	✓/✓	✓/✓
	T32A04INA1	Input	PD1 / PP1	✓/✓	✓/✓	✓/✓
	T32A04OUTA	Output	PD2 / PV5	✓/✓	✓/✓	✓/-
	T32A04INB0	Input	PD1 / PP1	✓/✓	✓/✓	✓/✓
	T32A04INB1	Input	PD0 / PP0	✓/✓	✓/✓	✓/✓
	T32A04OUTB	Output	PD3 / PV4	✓/✓	✓/✓	✓/-
	T32A04INC0	Input	PD0 / PP0	✓/✓	✓/✓	✓/✓
	T32A04INC1	Input	PD1 / PP1	✓/✓	✓/✓	✓/✓
	T32A04OUTC	Output	PD2 / PV5	✓/✓	✓/✓	✓/-
ch5	T32A05INA0	Input	PD6 / PP2	✓/✓	✓/✓	✓/✓
	T32A05INA1	Input	PD7 / PP3	✓/✓	✓/✓	✓/✓
	T32A05OUTA	Output	PD4 / PV6	✓/✓	✓/✓	✓/-
	T32A05INB0	Input	PD7 / PP3	✓/✓	✓/✓	✓/✓
	T32A05INB1	Input	PD6 / PP2	✓/✓	✓/✓	✓/✓
	T32A05OUTB	Output	PD5 / PV7	✓/✓	✓/✓	✓/-
	T32A05INC0	Input	PD6 / PP2	✓/✓	✓/✓	✓/✓
	T32A05INC1	Input	PD7 / PP3	✓/✓	✓/✓	✓/✓
	T32A05OUTC	Output	PD4 / PV6	✓/✓	✓/✓	✓/-
ch6	T32A06INA0	Input	PE2 / PP4	✓/✓	✓/✓	✓/✓
	T32A06INA1	Input	PE0 / PP5	✓/✓	✓/✓	✓/✓
	T32A06OUTA	Output	PE1 / PM5	✓/✓	✓/✓	✓/-
	T32A06INB0	Input	PE3 / PP5	✓/✓	✓/✓	✓/✓
	T32A06INB1	Input	PE0 / PP4	✓/✓	✓/✓	✓/✓
	T32A06OUTB	Output	PE0 / PM4	✓/✓	✓/✓	✓/-
	T32A06INC0	Input	PE2 / PP4	✓/✓	✓/✓	✓/✓
	T32A06INC1	Input	PE3 / PP5	✓/✓	✓/✓	✓/✓
	T32A06OUTC	Output	PE1 / PM5	✓/✓	✓/✓	✓/-

Table 2.56 T32A Function Pin and Port (3/4)

Channel	Function pin		Port	Product table (✓: Available, -: N/A)		
				M4GR	M4GQ	M4GN
ch7	T32A07INA0	Input	PE4 / PP6	✓/✓	✓/✓	✓/✓
	T32A07INA1	Input	PE7 / PP7	✓/✓	✓/✓	✓/✓
	T32A07OUTA	Output	PE6 / PM6	✓/✓	✓/✓	✓/-
	T32A07INB0	Input	PE5 / PP7	✓/✓	✓/✓	✓/✓
	T32A07INB1	Input	PE7 / PP6	✓/✓	✓/✓	✓/✓
	T32A07OUTB	Output	PE7 / PM7	✓/✓	✓/✓	✓/-
	T32A07INC0	Input	PE4 / PP6	✓/✓	✓/✓	✓/✓
	T32A07INC1	Input	PE5 / PP7	✓/✓	✓/✓	✓/✓
	T32A07OUTC	Output	PE6 / PM6	✓/✓	✓/✓	✓/-
ch8	T32A08INA0	Input	PC0 / PR0	✓/✓	✓/✓	-/-
	T32A08INA1	Input	-	-	-	-
	T32A08OUTA	Output	PC2 / PL4	✓/✓	✓/-	-/-
	T32A08INB0	Input	PC1 / PR1	✓/✓	✓/✓	-/-
	T32A08INB1	Input	-	-	-	-
	T32A08OUTB	Output	PC3 / PL5	✓/✓	✓/-	-/-
	T32A08INC0	Input	PC0 / PR0	✓/✓	✓/✓	-/-
	T32A08INC1	Input	PC1 / PR1	✓/✓	✓/✓	-/-
	T32A08OUTC	Output	PC2 / PL4	✓/✓	✓/-	-/-
ch9	T32A09INA0	Input	PR2 / PV0	✓/✓	✓/✓	-/-
	T32A09INA1	Input	-	-	-	-
	T32A09OUTA	Output	PL6 / PV2	✓/✓	-/✓	-/-
	T32A09INB0	Input	PR3 / PV1	✓/✓	✓/✓	-/-
	T32A09INB1	Input	-	-	-	-
	T32A09OUTB	Output	PL7 / PV3	✓/✓	-/✓	-/-
	T32A09INC0	Input	PR2 / PV0	✓/✓	✓/✓	-/-
	T32A09INC1	Input	PR3 / PV1	✓/✓	✓/✓	-/-
	T32A09OUTC	Output	PL6 / PV2	✓/✓	-/✓	-/-
ch10	T32A10INA0	Input	PR4 / PW4	✓/✓	✓/-	-/-
	T32A10INA1	Input	PW7	✓	-	-
	T32A10OUTA	Output	PC4 / PW5	✓/✓	✓/-	-/-
	T32A10INB0	Input	PR5	✓	✓	-
	T32A10INB1	Input	-	-	-	-
	T32A10OUTB	Output	PC5 / PW4	✓/✓	✓/-	-/-
	T32A10INC0	Input	PR4	✓	✓	-
	T32A10INC1	Input	PR5	✓	✓	-
	T32A10OUTC	Output	PC4 / PW5	✓/✓	✓/-	-/-
ch11	T32A11INA0	Input	PR6 / PW7	✓/✓	✓/-	-/-
	T32A11INA1	Input	PW4	✓	-	-
	T32A11OUTA	Output	PM2 / PW6	✓/✓	✓/-	-/-
	T32A11INB0	Input	PR7	✓	✓	-
	T32A11INB1	Input	-	-	-	-
	T32A11OUTB	Output	PM3 / PW7	✓/✓	✓/-	-/-
	T32A11INC0	Input	PR6	✓	✓	-
	T32A11INC1	Input	PR7	✓	✓	-
	T32A11OUTC	Output	PM2 / PW6	✓/✓	✓/-	-/-

Table 2.57 T32A Function Pin and Port (4/4)

Channel	Function pin		Port	Product table (✓: Available, -: N/A)		
				M4GR	M4GQ	M4GN
ch12	T32A12INA0	Input	PU2	✓	-	-
	T32A12INA1	Input	-	-	-	-
	T32A12OUTA	Output	PU0	✓	-	-
	T32A12INB0	Input	PU3	✓	-	-
	T32A12INB1	Input	-	-	-	-
	T32A12OUTB	Output	PU1	✓	-	-
	T32A12INC0	Input	PU2	✓	-	-
	T32A12INC1	Input	PU3	✓	-	-
	T32A12OUTC	Output	PU0	✓	-	-
ch13	T32A13INA0	Input	PU5	✓	-	-
	T32A13INA1	Input	-	-	-	-
	T32A13OUTA	Output	PU6	✓	-	-
	T32A13INB0	Input	PU4	✓	-	-
	T32A13INB1	Input	-	-	-	-
	T32A13OUTB	Output	PU7	✓	-	-
	T32A13INC0	Input	PU5	✓	-	-
	T32A13INC1	Input	PU4	✓	-	-
	T32A13OUTC	Output	PU6	✓	-	-

Note: The functional pins of ch14 and ch15 do not have port input / output.

2.14.3. Clock for Prescaler

The clock shown in the table below is used as the prescaler clock for T32A.

Table 2.58 T32A Clock for Prescaler

Clock for prescaler
ΦT0m

2.14.4. Internal Signal Connection Specification

The following tables show the internal signals connected to the T32A.

2.14.4.1. Capture/counter Channel Connection Specification

The following tables show the capture trigger signals connected to the T32A.

The input trigger signal which has a register name in the trigger selector column of the following tables should select the input trigger with a trigger selector.

Table 2.59 T32A Input Trigger Connection

T32A				Trigger selector	T32A			
Channel	Timer	Function input	Signal name		Channel	Timer	Function output	Signal name
ch0	A	Internal trigger (Register A0 match)	T32A00TRGOUTCMPA0	***[TSEL0CR11]*** <INSEL47[2:0]>	ch0	B	Internal trigger input	T32A00TRGINBPCK
ch1	A	Internal trigger (Register A0 match)	T32A01TRGOUTCMPA0	***[TSEL0CR12]*** <INSEL49[2:0]>	ch1	B	Internal trigger input	T32A01TRGINBPCK
ch2	A	Internal trigger (Register A0 match)	T32A02TRGOUTCMPA0	***[TSEL0CR11]*** <INSEL51[2:0]>	ch2	B	Internal trigger input	T32A02TRGINBPCK
				-	ch12	A	Internal trigger input	T32A12TRGINAPCK
				-	ch12	B		T32A12TRGINBPCK
				[TSEL0CR8] <INSEL35[2:0]>	ch13	A		T32A13TRGINAPCK
				[TSEL0CR9] <INSEL36[2:0]>	ch13	B		T32A13TRGINBPCK
ch3	A	Internal trigger (Register A0 match)	T32A03TRGOUTCMPA0	***[TSEL0CR13]*** <INSEL53[2:0]>	ch3	B	Internal trigger input	T32A03TRGINBPCK
ch4	A	Internal trigger (Register A0 match)	T32A04TRGOUTCMPA0	***[TSEL0CR13]*** <INSEL55[2:0]>	ch4	B	Internal trigger input	T32A04TRGINBPCK
ch5	A	Internal trigger (Register A0 match)	T32A05TRGOUTCMPA0	***[TSEL0CR10]*** <INSEL40[2:0]>	ch5	B	Internal trigger input	T32A05TRGINBPCK
ch6	A	Internal trigger (Register A0 match)	T32A06TRGOUTCMPA0	***[TSEL0CR10]*** <INSEL42[2:0]>	ch6	B	Internal trigger input	T32A06TRGINBPCK
ch7	A	Internal trigger (Register A0 match)	T32A07TRGOUTCMPA0	***[TSEL0CR11]*** <INSEL44[2:0]>	ch7	B	Internal trigger input	T32A07TRGINBPCK
ch12	A	Internal trigger (Register A0 match)	T32A12TRGOUTCMPA0	***[TSEL0CR11]*** <INSEL46[2:0]>	ch0	A	Internal trigger input	T32A00TRGINAPCK
				[TSEL0CR11] <INSEL47[2:0]>	ch0	B		T32A00TRGINBPCK
				[TSEL0CR12] <INSEL48[2:0]>	ch1	A		T32A01TRGINAPCK
				[TSEL0CR12] <INSEL49[2:0]>	ch1	B		T32A01TRGINBPCK
ch12	B	Internal trigger (Register B0 match)	T32A12TRGOUTCMPB0	***[TSEL0CR12]*** <INSEL50[2:0]>	ch2	A	Internal trigger input	T32A02TRGINAPCK
				[TSEL0CR12] <INSEL51[2:0]>	ch2	B		T32A02TRGINBPCK
				[TSEL0CR13] <INSEL52[2:0]>	ch3	A		T32A03TRGINAPCK
				[TSEL0CR13] <INSEL53[2:0]>	ch3	B		T32A03TRGINBPCK

T32A				Trigger selector	T32A			
Channel	Timer	Function input	Signal name		Channel	Timer	Function output	Signal name
ch12	C	Internal trigger (Register C0 match)	T32A12TRGOUTCMPC0	-	ch0	C	Internal trigger input	T32A00TRGINCPCK
				-	ch1	C		T32A01TRGINCPCK
				-	ch2	C		T32A02TRGINCPCK
				-	ch3	C		T32A03TRGINCPCK
ch13	A	Internal trigger (Register A0 match)	T32A13TRGOUTCMPA0	***[TSEL0CR13]*** <INSEL54[2:0]>	ch4	A	Internal trigger input	T32A04TRGINAPCK
				[TSEL0CR13] <INSEL55[2:0]>	ch4	B		T32A04TRGINBPCK
				[TSEL0CR9] <INSEL39[2:0]>	ch5	A		T32A05TRGINAPCK
				[TSEL0CR10] <INSEL40[2:0]>	ch5	B		T32A05TRGINBPCK
ch13	B	Internal trigger (Register B0 match)	T32A13TRGOUTCMPB0	***[TSEL0CR10]*** <INSEL41[2:0]>	ch6	A	Internal trigger input	T32A06TRGINAPCK
				[TSEL0CR10] <INSEL42[2:0]>	ch6	B		T32A06TRGINBPCK
				[TSEL0CR10] <INSEL43[2:0]>	ch7	A		T32A07TRGINAPCK
				[TSEL0CR11] <INSEL44[2:0]>	ch7	B		T32A07TRGINBPCK
ch13	C	Internal trigger (Register C0 match)	T32A13TRGOUTCMPC0	-	ch4	C	Internal trigger input	T32A04TRGINCPCK
				-	ch5	C		T32A05TRGINCPCK
				-	ch6	C		T32A06TRGINCPCK
				-	ch7	C		T32A07TRGINCPCK
ch14	A	Internal trigger (Register A0 match)	T32A14TRGOUTCMPA0	-	ch14	B	Internal trigger input	T32A14TRGINBPCK
ch15	A	Internal trigger (Register A0 match)	T32A15TRGOUTCMPA0	-	ch15	B	Internal trigger input	T32A15TRGINBPCK
ch8	C	Internal trigger (Register C0 match)	T3208TRGOUTCMPC0	-	ch9	C	Internal trigger input	T32A09TRGINCPCK
ch10	C	Internal trigger (Register C0 match)	T32A10TRGOUTCMPC0	-	ch11	C	Internal trigger input	T32A11TRGINCPCK
ch12	C	Internal trigger (Register C0 match)	T32A12TRGOUTCMPC0	-	ch13	C	Internal trigger input	T32A13TRGINCPCK
ch14	C	Internal trigger (Register C0 match)	T32A14TRGOUTCMPC0	-	ch15	C	Internal trigger input	T32A15TRGINCPCK

Note: -: Not available.

Table 2.60 T32A Timer Output Trigger Connection

T32A				Trigger selector	T32A			
Channel	Timer	Function output	Signal name		Channel	Timer	Function input	Signal name
ch0	A	Timer output	T32A00OUTA	-	ch12	A	Another timer output	T32A12TRGINAPHCK
ch0	B	Timer output	T32A00OUTB	-	ch12	B	Another timer output	T32A12TRGINBPHCK
ch0	C	Timer output	T32A00OUTC	-	ch1	C	Another timer output	T32A01TRGINCPHCK
ch1	A	Timer output	T32A01OUTA	-	ch13	A	Another timer output	T32A13TRGINAPHCK
ch1	B	Timer output	T32A01OUTB	-	ch13	B	Another timer output	T32A13TRGINBPHCK
ch2	A	Timer output	T32A02OUTA	-	ch14	A	Another timer output	T32A14TRGINAPHCK
ch2	B	Timer output	T32A02OUTB	-	ch14	B	Another timer output	T32A14TRGINBPHCK
ch2	C	Timer output	T32A02OUTC	-	ch3	C	Another timer output	T32A03TRGINCPHCK
ch3	A	Timer output	T32A03OUTA	-	ch15	A	Another timer output	T32A15TRGINAPHCK
ch3	B	Timer output	T32A03OUTB	-	ch15	B	Another timer output	T32A15TRGINBPHCK
ch4	A	Timer output	T32A04OUTA	-	ch8	A	Another timer output	T32A08TRGINAPHCK
ch4	B	Timer output	T32A04OUTB	***[TSEL0CR11]*** <INSEL45[2:0]>	ch8	B	Another timer output	T32A08TRGINBPHCK
ch4	C	Timer output	T32A04OUTC	-	ch5	C	Another timer output	T32A05TRGINCPHCK
ch5	A	Timer output	T32A05OUTA	-	ch9	A	Another timer output	T32A09TRGINAPHCK
ch5	B	Timer output	T32A05OUTB	-	ch9	B	Another timer output	T32A09TRGINBPHCK
ch6	A	Timer output	T32A06OUTA	-	ch10	A	Another timer output	T32A10TRGINAPHCK
ch6	B	Timer output	T32A06OUTB	-	ch10	B	Another timer output	T32A10TRGINBPHCK
ch6	C	Timer output	T32A06OUTC	-	ch7	C	Another timer output	T32A07TRGINCPHCK
ch7	A	Timer output	T32A07OUTA	-	ch11	A	Another timer output	T32A11TRGINAPHCK
ch7	B	Timer output	T32A07OUTB	-	ch11	B	Another timer output	T32A11TRGINBPHCK
ch8	A	Timer output	T32A08OUTA	***[TSEL0CR11]*** <INSEL45[2:0]>	ch8	B	Another timer output	T32A08TRGINBPHCK
ch8	C	Timer output	T32A08OUTC	-	ch9	C	Another timer output	T32A09TRGINCPHCK
ch10	C	Timer output	T32A10OUTC	-	ch11	C	Another timer output	T32A11TRGINCPHCK
ch12	C	Timer output	T32A12OUTC	-	ch13	C	Another timer output	T32A13TRGINCPHCK
ch14	C	Timer output	T32A14OUTC	-	ch15	C	Another timer output	T32A15TRGINCPHCK

Note: -: Not available.

2.14.4.2. Synchronous Control Connection Specification

The timer synchronous connection specification of a T32A is shown in the following tables.

Table 2.61 T32A Synchronous Control Connection Specification (1/3)

Master				Slave			
Channel	Timer	Function output	Signal name	Channel	Timer	Function input	Signal name
ch0	A	Synchronous start output A	T32A00SYNCSTARTOUTA	ch0	B	Synchronous start B	T32A00SYNCSTARTB
				ch1	A	Synchronous start A	T32A01SYNCSTARTA
				ch1	B	Synchronous start B	T32A01SYNCSTARTB
		Synchronous stop output A	T32A00SYNCSTOPOUTA	ch0	B	Synchronous stop B	T32A00SYNCSTOPB
				ch1	A	Synchronous stop A	T32A01SYNCSTOPA
				ch1	B	Synchronous stop B	T32A01SYNCSTOPB
		Synchronous reload output A	T32A00SYNCRELOADOUTA	ch0	B	Synchronous reload B	T32A00SYNCRELOADB
				ch1	A	Synchronous reload A	T32A01SYNCRELOADA
				ch1	B	Synchronous reload B	T32A01SYNCRELOADB
ch0	C	Synchronous start output C	T32A00SYNCSTARTOUTC	ch1	C	Synchronous start C	T32A01SYNCSTARTC
		Synchronous stop output C	T32A00SYNCSTOPOUTC	ch1	C	Synchronous stop C	T32A01SYNCSTOPC
		Synchronous reload output C	T32A00SYNCRELOADOUTC	ch1	C	Synchronous reload C	T32A01SYNCRELOADC
ch2	A	Synchronous start output A	T32A02SYNCSTARTOUTA	ch2	B	Synchronous start B	T32A02SYNCSTARTB
				ch3	A	Synchronous start A	T32A03SYNCSTARTA
				ch3	B	Synchronous start B	T32A03SYNCSTARTB
		Synchronous stop output A	T32A02SYNCSTOPOUTA	ch2	B	Synchronous stop B	T32A02SYNCSTOPB
				ch3	A	Synchronous stop A	T32A03SYNCSTOPA
				ch3	B	Synchronous stop B	T32A03SYNCSTOPB
		Synchronous reload output A	T32A02SYNCRELOADOUTA	ch2	B	Synchronous reload B	T32A02SYNCRELOADB
				ch3	A	Synchronous reload A	T32A03SYNCRELOADA
				ch3	B	Synchronous reload B	T32A03SYNCRELOADB
ch2	C	Synchronous start output C	T32A02SYNCSTARTOUTC	ch3	C	Synchronous start C	T32A03SYNCSTARTC
		Synchronous stop output C	T32A02SYNCSTOPOUTC	ch3	C	Synchronous stop C	T32A03SYNCSTOPC
		Synchronous reload output C	T32A02SYNCRELOADOUTC	ch3	C	Synchronous reload C	T32A03SYNCRELOADC

Table 2.62 T32A Synchronous Control Connection Specification (2/3)

Master				Slave			
Channel	Timer	Function output	Signal name	Channel	Timer	Function input	Signal name
ch4	A	Synchronous start output A	T32A04SYNCSTARTOUTA	ch4	B	Synchronous start B	T32A04SYNCSTARTB
				ch5	A	Synchronous start A	T32A05SYNCSTARTA
				ch5	B	Synchronous start B	T32A05SYNCSTARTB
		Synchronous stop output A	T32A04SYNCSTOPOUTA	ch4	B	Synchronous stop B	T32A04SYNCSTOPB
				ch5	A	Synchronous stop A	T32A05SYNCSTOPA
				ch5	B	Synchronous stop B	T32A05SYNCSTOPB
		Synchronous reload output A	T32A04SYNCRELOADOUTA	ch4	B	Synchronous reload B	T32A04SYNCRELOADB
				ch5	A	Synchronous reload A	T32A05SYNCRELOADA
				ch5	B	Synchronous reload B	T32A05SYNCRELOADB
ch4	C	Synchronous start output C	T32A04SYNCSTARTOUTC	ch5	C	Synchronous start C	T32A05SYNCSTARTC
		Synchronous stop output C	T32A04SYNCSTOPOUTC	ch5	C	Synchronous stop C	T32A05SYNCSTOPC
		Synchronous reload output C	T32A04SYNCRELOADOUTC	ch5	C	Synchronous reload C	T32A05SYNCRELOADC
ch6	A	Synchronous start output A	T32A06SYNCSTARTOUTA	ch6	B	Synchronous start B	T32A06SYNCSTARTB
				ch7	A	Synchronous start A	T32A07SYNCSTARTA
				ch7	B	Synchronous start B	T32A07SYNCSTARTB
		Synchronous stop output A	T32A06SYNCSTOPOUTA	ch6	B	Synchronous stop B	T32A06SYNCSTOPB
				ch7	A	Synchronous stop A	T32A07SYNCSTOPA
				ch7	B	Synchronous stop B	T32A07SYNCSTOPB
		Synchronous reload output A	T32A06SYNCRELOADOUTA	ch6	B	Synchronous reload B	T32A06SYNCRELOADB
				ch7	A	Synchronous reload A	T32A07SYNCRELOADA
				ch7	B	Synchronous reload B	T32A07SYNCRELOADB
ch6	C	Synchronous start output C	T32A06SYNCSTARTOUTC	ch7	C	Synchronous start C	T32A07SYNCSTARTC
		Synchronous stop output C	T32A06SYNCSTOPOUTC	ch7	C	Synchronous stop C	T32A07SYNCSTOPC
		Synchronous reload output C	T32A06SYNCRELOADOUTC	ch7	C	Synchronous reload C	T32A07SYNCRELOADC
ch8	A	Synchronous start output A	T32A08SYNCSTARTOUTA	ch8	B	Synchronous start B	T32A08SYNCSTARTB
				ch9	A	Synchronous start A	T32A09SYNCSTARTA
				ch9	B	Synchronous start B	T32A09SYNCSTARTB
		Synchronous stop output A	T32A08SYNCSTOPOUTA	ch8	B	Synchronous stop B	T32A08SYNCSTOPB
				ch9	A	Synchronous stop A	T32A09SYNCSTOPA
				ch9	B	Synchronous stop B	T32A09SYNCSTOPB
		Synchronous reload output A	T32A08SYNCRELOADOUTA	ch8	B	Synchronous reload B	T32A08SYNCRELOADB
				ch9	A	Synchronous reload A	T32A09SYNCRELOADA
				ch9	B	Synchronous reload B	T32A09SYNCRELOADB
ch8	C	Synchronous start output C	T32A08SYNCSTARTOUTC	ch9	C	Synchronous start C	T32A09SYNCSTARTC
		Synchronous stop output C	T32A08SYNCSTOPOUTC	ch9	C	Synchronous stop C	T32A09SYNCSTOPC
		Synchronous reload output C	T32A08SYNCRELOADOUTC	ch9	C	Synchronous reload C	T32A09SYNCRELOADC

Table 2.63 T32A Synchronous Control Connection Specification (3/3)

Master				Slave			
Channel	Timer	Function output	Signal name	Channel	Timer	Function input	Signal name
ch10	A	Synchronous start output A	T32A10SYNCSTARTOUTA	ch10	B	Synchronous start B	T32A10SYNCSTARTB
				ch11	A	Synchronous start A	T32A11SYNCSTARTA
				ch11	B	Synchronous start B	T32A11SYNCSTARTB
		Synchronous stop output A	T32A10SYNCSTOPOUTA	ch10	B	Synchronous stop B	T32A10SYNCSTOPB
				ch11	A	Synchronous stop A	T32A11SYNCSTOPA
				ch11	B	Synchronous stop B	T32A11SYNCSTOPB
		Synchronous reload output A	T32A10SYNCRELOADOUTA	ch10	B	Synchronous reload B	T32A10SYNCRELOADB
				ch11	A	Synchronous reload A	T32A11SYNCRELOADA
				ch11	B	Synchronous reload B	T32A11SYNCRELOADB
ch10	C	Synchronous start output C	T32A10SYNCSTARTOUTC	ch11	C	Synchronous start C	T32A11SYNCSTARTC
		Synchronous stop output C	T32A10SYNCSTOPOUTC	ch11	C	Synchronous stop C	T32A11SYNCSTOPC
		Synchronous reload output C	T32A10SYNCRELOADOUTC	ch11	C	Synchronous reload C	T32A11SYNCRELOADC
ch12	A	Synchronous start output A	T32A12SYNCSTARTOUTA	ch12	B	Synchronous start B	T32A12SYNCSTARTB
				ch13	A	Synchronous start A	T32A13SYNCSTARTA
				ch13	B	Synchronous start B	T32A13SYNCSTARTB
		Synchronous stop output A	T32A12SYNCSTOPOUTA	ch12	B	Synchronous stop B	T32A12SYNCSTOPB
				ch13	A	Synchronous stop A	T32A13SYNCSTOPA
				ch13	B	Synchronous stop B	T32A13SYNCSTOPB
		Synchronous reload output A	T32A12SYNCRELOADOUTA	ch12	B	Synchronous reload B	T32A12SYNCRELOADB
				ch13	A	Synchronous reload A	T32A13SYNCRELOADA
				ch13	B	Synchronous reload B	T32A13SYNCRELOADB
ch12	C	Synchronous start output C	T32A12SYNCSTARTOUTC	ch13	C	Synchronous start C	T32A13SYNCSTARTC
		Synchronous stop output C	T32A12SYNCSTOPOUTC	ch13	C	Synchronous stop C	T32A13SYNCSTOPC
		Synchronous reload output C	T32A12SYNCRELOADOUTC	ch13	C	Synchronous reload C	T32A13SYNCRELOADC
ch14	A	Synchronous start output A	T32A14SYNCSTARTOUTA	ch14	B	Synchronous start B	T32A14SYNCSTARTB
				ch15	A	Synchronous start A	T32A15SYNCSTARTA
				ch15	B	Synchronous start B	T32A15SYNCSTARTB
		Synchronous stop output A	T32A14SYNCSTOPOUTA	ch14	B	Synchronous stop B	T32A14SYNCSTOPB
				ch15	A	Synchronous stop A	T32A15SYNCSTOPA
				ch15	B	Synchronous stop B	T32A15SYNCSTOPB
		Synchronous reload output A	T32A14SYNCRELOADOUTA	ch14	B	Synchronous reload B	T32A14SYNCRELOADB
				ch15	A	Synchronous reload A	T32A15SYNCRELOADA
				ch15	B	Synchronous reload B	T32A15SYNCRELOADB
ch14	C	Synchronous start output C	T32A14SYNCSTARTOUTC	ch15	C	Synchronous start C	T32A15SYNCSTARTC
		Synchronous stop output C	T32A14SYNCSTOPOUTC	ch15	C	Synchronous stop C	T32A15SYNCSTOPC
		Synchronous reload output C	T32A14SYNCRELOADOUTC	ch15	C	Synchronous reload C	T32A15SYNCRELOADC

2.14.4.3. T32A Timer Channel Reload Trigger Connection Specification

Table 2.64 T32A Reload Trigger Connection

T32A				Trigger selector	T32A			
Channel	Timer	Function output	Signal name		Channel	Timer	Function input	Signal name
ch9	A	Internal trigger (Register A0 match)	T32A09TRGOUTCMPA0	***[TSEL0CR9]*** <INSEL39[2:0]>	ch5	A	Internal trigger input	T32A05TRGINAPCK
				[TSEL0CR10] <INSEL40[2:0]>	ch5	B		T32A05TRGINBPCK
				-	ch9	B		T32A09TRGINBPCK
ch10	A	Internal trigger (Register A0 match)	T32A10TRGOUTCMPA0	***[TSEL0CR10]*** <INSEL41[2:0]>	ch6	A	Internal trigger input	T32A06TRGINAPCK
				[TSEL0CR10] <INSEL42[2:0]>	ch6	B		T32A06TRGINBPCK
				-	ch10	B		T32A10TRGINBPCK
ch11	A	Internal trigger (Register A0 match)	T32A11TRGOUTCMPA0	***[TSEL0CR10]*** <INSEL43[2:0]>	ch7	A	Internal trigger input	T32A07TRGINAPCK
				[TSEL0CR11] <INSEL44[2:0]>	ch7	B		T32A07TRGINBPCK
				-	ch11	B		T32A11TRGINBPCK

2.14.4.4. TSPI/UART/RMC - T32A Connection Specification

Table 2.65 T32A TSPI/UART/RMC - T32A Connection Specification

TSPI, UART, RMC		Trigger selector	T32A			
Function output	Signal name		Channel	Timer	Function input	Signal name
TSPI ch0 transmit complete trigger	TSPI0TXDEND	***[TSEL0CR11]*** <INSEL46[2:0]>	ch0	A	Internal trigger input	T32A00TRGINAPCK
UART ch0 transmission completion trigger	UART0TXTRG					
TSPI ch0 receive complete trigger	TSPI0RXDEND	***[TSEL0CR11]*** <INSEL47[2:0]>	ch0	B	Internal trigger input	T32A00TRGINBPCK
UART ch0 reception completion trigger	UART0RXTRG					
TSPI ch1 transmit complete trigger	TSPI1TXDEND	***[TSEL0CR12]*** <INSEL48[2:0]>	ch1	A	Internal trigger input	T32A01TRGINAPCK
UART ch1 transmission completion trigger	UART1TXTRG					
TSPI ch1 receive complete trigger	TSPI1RXDEND	***[TSEL0CR12]*** <INSEL49[2:0]>	ch1	B	Internal trigger input	T32A01TRGINBPCK
UART ch1 reception completion trigger	UART1RXTRG					
TSPI ch2 transmit complete trigger	TSPI2TXDEND	***[TSEL0CR12]*** <INSEL50[2:0]>	ch2	A	Internal trigger input	T32A02TRGINAPCK
UART ch2 transmission completion trigger	UART2TXTRG					
TSPI ch2 receive complete trigger	TSPI2RXDEND	***[TSEL0CR12]*** <INSEL51[2:0]>	ch2	B	Internal trigger input	T32A02TRGINBPCK
UART ch2 reception completion trigger	UART2RXTRG					
TSPI ch3 transmit complete trigger	TSPI3TXDEND	***[TSEL0CR13]*** <INSEL52[2:0]>	ch3	A	Internal trigger input	T32A03TRGINAPCK
UART ch3 transmission completion trigger	UART3TXTRG					
TSPI ch3 receive complete trigger	TSPI3RXDEND	***[TSEL0CR13]*** <INSEL53[2:0]>	ch3	B	Internal trigger input	T32A03TRGINBPCK
UART ch3 reception completion trigger	UART3RXTRG					
TSPI ch4 transmit complete trigger	TSPI4TXDEND	***[TSEL0CR13]*** <INSEL54[2:0]>	ch4	A	Internal trigger input	T32A04TRGINAPCK
UART ch4 transmission completion trigger	UART4TXTRG					
TSPI ch4 receive complete trigger	TSPI4RXDEND	***[TSEL0CR13]*** <INSEL55[2:0]>	ch4	B	Internal trigger input	T32A04TRGINBPCK
UART ch4 reception completion trigger	UART4RXTRG					
TSPI ch5 transmit complete trigger	TSPI5TXDEND	***[TSEL0CR9]*** <INSEL39[2:0]>	ch5	A	Internal trigger input	T32A05TRGINAPCK
UART ch5 transmission completion trigger	UART5TXTRG					
TSPI ch5 receive complete trigger	TSPI5RXDEND	***[TSEL0CR10]*** <INSEL40[2:0]>	ch5	B	Internal trigger input	T32A05TRGINBPCK
UART ch5 reception completion trigger	UART5RXTRG					
TSPI ch6 transmit complete trigger	TSPI6TXDEND	***[TSEL0CR10]*** <INSEL41[2:0]>	ch6	A	Internal trigger input	T32A06TRGINAPCK
TSPI ch6 receive complete trigger	TSPI6RXDEND	***[TSEL0CR10]*** <INSEL42[2:0]>	ch6	B	Internal trigger input	T32A06TRGINBPCK
TSPI ch7 transmit complete trigger	TSPI7TXDEND	***[TSEL0CR10]*** <INSEL43[2:0]>	ch7	A	Internal trigger input	T32A07TRGINAPCK
TSPI ch7 receive complete trigger	TSPI7RXDEND	***[TSEL0CR11]*** <INSEL44[2:0]>	ch7	B	Internal trigger input	T32A07TRGINBPCK
TSPI ch8 transmit complete trigger	TSPI8TXDEND	***[TSEL0CR8]*** <INSEL34[2:0]>	ch8	A	Internal trigger input	T32A08TRGINAPCK
TSPI ch8 receive complete trigger	TSPI8RXDEND					
RMC ch0 trigger output	RMC0TRG	***[TSEL0CR8]*** <INSEL35[2:0]>	ch13	A	Internal trigger input	T32A13TRGINAPCK
RMC ch1 trigger output	RMC1TRG	***[TSEL0CR9]*** <INSEL36[2:0]>	ch13	B	Internal trigger input	T32A13TRGINBPCK

2.14.4.5. T32A - ISD Connection Specification

Table 2.66 T32A - ISD Connection Specification

T32A				ISD		
Channel	**Timer**	**Function output**	**Signal name**	**Unit**	**Function input**	**Signal name**
ch9	A	Timer A output	T32A09OUTA	A	Timer trigger A for clock source	ISDACLKTRG
				B	Timer trigger B for clock source	ISDBCLKTRG
				C	Timer trigger C for clock source	ISDCCLKTRG

2.14.4.6. ELOSC Low-speed Clock - T32A Connection Specification

Table 2.67 T32A ELOSC low speed Clock - T32A connection specification

ELOSC		Trigger selector	T32A			
Function output	Signal name		Channel	Timer	Function input	Signal name
ELOSC low-speed clock	fs	***[TSEL0CR8]*** <INSEL34[2:0]>	ch8	A	Internal trigger input	T32A08TRGINAPCK

2.14.5. Pulse Count Support List for Each Product

In the T32A, as shown in the following table, correspondence of a pulse counter changes with products.

Table 2.68 T32A Pulse Count Support List

Channel	Product table (-: Not available)		
	M4GR	M4GQ	M4GN
ch0	2-phase pulse count 1-phase pulse count		
ch1	2-phase pulse count 1-phase pulse count		
ch2	2-phase pulse count 1-phase pulse count		
ch3	2-phase pulse count 1-phase pulse count		
ch4	2-phase pulse count 1-phase pulse count		
ch5	2-phase pulse count 1-phase pulse count		
ch6	2-phase pulse count 1-phase pulse count		
ch7	2-phase pulse count 1-phase pulse count		
ch8	2-phase pulse count 1-phase pulse count		-
ch9	2-phase pulse count 1-phase pulse count		-
ch10	2-phase pulse count 1-phase pulse count		-
ch11	2-phase pulse count 1-phase pulse count		-
ch12	2-phase pulse count 1-phase pulse count	-	
ch13	2-phase pulse count 1-phase pulse count	-	
ch14	-		
ch15	-		

2.14.6. DMA Request

The T32A has the DMA request shown in the following tables.

When there is mention of the register name in the trigger selector column of the tables, please select a request to use with a trigger selector.

Table 2.69 T32A DMA Request (1/3)

Channel	Request	Signal name	Trigger selector	DMA request channel (MDMAC unit A)		
					Single transfer	Burst transfer
ch0	DMA request at capture A0 register	T32A00DMAREQCAPA0	***[TSEL0CR0]*** <INSEL0[2:0]>	0	✓	-
	DMA request at capture C0 register	T32A00DMAREQCAPC0	***[TSEL0CR0]*** <INSEL1[2:0]>	1	✓	-
	DMA request at match A1 register	T32A01DMAREQCMPA1	***[TSEL0CR1]*** <INSEL4[2:0]>	4	✓	-
	DMA request at match C1 register	T32A00DMAREQCMPC1				
	DMA request at match B1 register	T32A00DMAREQCMPB1	***[TSEL0CR1]*** <INSEL5[2:0]>	5	✓	-
	DMA request at capture B0 register	T32A00DMAREQCAPB0				
ch1	DMA request at match A1 register	T32A01DMAREQCMPA1	***[TSEL0CR1]*** <INSEL6[2:0]>	6	✓	-
	DMA request at match C1 register	T32A01DMAREQCMPC1				
	DMA request at capture A0 register	T32A01DMAREQCAPA0				
	DMA request at capture C0 register	T32A01DMAREQCAPC0				
	DMA request at match B1 register	T32A01DMAREQCMPB1	***[TSEL0CR1]*** <INSEL7[2:0]>	7	✓	-
	DMA request at capture B0 register	T32A01DMAREQCAPB0				
ch2	DMA request at match A1 register	T32A02DMAREQCMPA1	***[TSEL0CR2]*** <INSEL8[2:0]>	8	✓	-
	DMA request at match C1 register	T32A02DMAREQCMPC1				
	DMA request at capture A0 register	T32A02DMAREQCAPA0				
	DMA request at capture C0 register	T32A02DMAREQCAPC0				
	DMA request at match B1 register	T32A02DMAREQCMPB1	***[TSEL0CR2]*** <INSEL9[2:0]>	9	✓	-
	DMA request at capture B0 register	T32A02DMAREQCAPB0				
ch3	DMA request at match A1 register	T32A03DMAREQCMPA1	***[TSEL0CR2]*** <INSEL10[2:0]>	10	✓	-
	DMA request at match C1 register	T32A03DMAREQCMPC1				
	DMA request at capture A0 register	T32A03DMAREQCAPA0				
	DMA request at capture C0 register	T32A03DMAREQCAPC0				
	DMA request at match B1 register	T32A03DMAREQCMPB1	***[TSEL0CR2]*** <INSEL11[2:0]>	11	✓	-
	DMA request at capture B0 register	T32A03DMAREQCAPB0				
ch4	DMA request at match A1 register	T32A04DMAREQCMPA1	***[TSEL0CR3]*** <INSEL12[2:0]>	12	✓	-
	DMA request at match C1 register	T32A04DMAREQCMPC1				
	DMA request at capture A0 register	T32A04DMAREQCAPA0				
	DMA request at capture C0 register	T32A04DMAREQCAPC0				
	DMA request at match B1 register	T32A04DMAREQCMPB1	***[TSEL0CR3]*** <INSEL13[2:0]>	13	✓	-
	DMA request at Capture B0 register	T32A04DMAREQCAPB0				
ch5	DMA request at match A1 register	T32A05DMAREQCMPA1	***[TSEL0CR3]*** <INSEL14[2:0]>	14	✓	-
	DMA request at match C1 register	T32A05DMAREQCMPC1				
	DMA request at capture A0 register	T32A05DMAREQCAPA0				
	DMA request at capture C0 register	T32A05DMAREQCAPC0				
	DMA request at match B1 register	T32A05DMAREQCMPB1	***[TSEL0CR3]*** <INSEL15[2:0]>	15	✓	-
	DMA request at capture B0 register	T32A05DMAREQCAPB0				

Note: ✓: Available, -: Not available.

Table 2.70 T32A DMA Request (2/3)

Channel	Request	Signal name	Trigger selector	DMA request channel (MDMAC unit A)		
					Single transfer	Burst transfer
ch6	DMA request at match A1 register	T32A06DMAREQCMPA1	***[TSEL0CR4]*** <INSEL16[2:0]>	16	✓	-
	DMA request at match C1 register	T32A06DMAREQCMPC1				
	DMA request at Capture A0 register	T32A06DMAREQCAPA0				
	DMA request at Capture C0 register	T32A06DMAREQCAPC0				
	DMA request at match B1 register	T32A06DMAREQCMPB1	***[TSEL0CR4]*** <INSEL17[2:0]>	17	✓	-
	DMA request at Capture B0 register	T32A06DMAREQCAPB0				
ch7	DMA request at match A1 register	T32A07DMAREQCMPA1	***[TSEL0CR4]*** <INSEL18[2:0]>	18	✓	-
	DMA request at match C1 register	T32A07DMAREQCMPC1				
	DMA request at Capture A0 register	T32A07DMAREQCAPA0				
	DMA request at Capture C0 register	T32A07DMAREQCAPC0				
	DMA request at match B1 register	T32A07DMAREQCMPB1	***[TSEL0CR4]*** <INSEL19[2:0]>	19	✓	-
	DMA request at Capture B0 register	T32A07DMAREQCAPB0				
ch8	DMA request at match A1 register	T32A08DMAREQCMPA1	***[TSEL0CR5]*** <INSEL20[2:0]>	20	✓	-
	DMA request at match C1 register	T32A08DMAREQCMPC1				
	DMA request at Capture A0 register	T32A08DMAREQCAPA0				
	DMA request at Capture C0 register	T32A08DMAREQCAPC0				
	DMA request at match B1 register	T32A08DMAREQCMPB1	***[TSEL0CR5]*** <INSEL21[2:0]>	21	✓	-
	DMA request at Capture B0 register	T32A08DMAREQCAPB0				
ch9	DMA request at match A1 register	T32A09DMAREQCMPA1	***[TSEL0CR5]*** <INSEL22[2:0]>	22	✓	-
	DMA request at match C1 register	T32A09DMAREQCMPC1				
	DMA request at Capture A0 register	T32A09DMAREQCAPA0				
	DMA request at Capture C0 register	T32A09DMAREQCAPC0				
	DMA request at match B1 register	T32A09DMAREQCMPB1	***[TSEL0CR5]*** <INSEL23[2:0]>	23	✓	-
	DMA request at Capture B0 register	T32A09DMAREQCAPB0				
	DMA request at Capture A1 register	T32A09DMAREQCAPA1				
	DMA request at Capture B1 register	T32A09DMAREQCAPB1				
ch10	DMA request at match A1 register	T32A10DMAREQCMPA1	***[TSEL0CR6]*** <INSEL24[2:0]>	24	✓	-
	DMA request at match C1 register	T32A10DMAREQCMPC1				
	DMA request at Capture A0 register	T32A10DMAREQCAPA0				
	DMA request at Capture C0 register	T32A10DMAREQCAPC0				
	DMA request at match B1 register	T32A10DMAREQCMPB1	***[TSEL0CR6]*** <INSEL25[2:0]>	25	✓	-
	DMA request at Capture B0 register	T32A10DMAREQCAPB0				
	DMA request at Capture A1 register	T32A10DMAREQCAPA1				
	DMA request at Capture B1 register	T32A10DMAREQCAPB1				
ch11	DMA request at match A1 register	T32A11DMAREQCMPA1	***[TSEL0CR6]*** <INSEL26[2:0]>	26	✓	-
	DMA request at match C1 register	T32A11DMAREQCMPC1				
	DMA request at Capture A0 register	T32A11DMAREQCAPA0				
	DMA request at Capture C0 register	T32A11DMAREQCAPC0				
	DMA request at match B1 register	T32A11DMAREQCMPB1	***[TSEL0CR6]*** <INSEL27[2:0]>	27	✓	-
	DMA request at Capture B0 register	T32A11DMAREQCAPB0				
	DMA request at Capture A1 register	T32A11DMAREQCAPA1				
	DMA request at Capture B1 register	T32A11DMAREQCAPB1				

Note: ✓: Available, -: Not available.

Table 2.71 T32A DMA Request (3/3)

Channel	Request	Signal name	Trigger selector	DMA request channel (MDMAC unit A)		
					Single transfer	Burst transfer
ch12	DMA request at match A1 register	T32A12DMAREQCMPA1	***[TSEL0CR7]*** <INSEL28[2:0]>	28	✓	-
	DMA request at match C1 register	T32A12DMAREQCMPC1				
	DMA request at capture A0 register	T32A12DMAREQCAPA0				
	DMA request at capture C0 register	T32A12DMAREQCAPC0				
	DMA request at match B1 register	T32A12DMAREQCMPB1	***[TSEL0CR7]*** <INSEL29[2:0]>	29	✓	-
	DMA request at capture B0 register	T32A12DMAREQCAPB0				
ch13	DMA request at match A1 register	T32A13DMAREQCMPA1	***[TSEL0CR7]*** <INSEL30[2:0]>	30	✓	-
	DMA request at match C1 register	T32A13DMAREQCMPC1				
	DMA request at capture A0 register	T32A13DMAREQCAPA0				
	DMA request at capture C0 register	T32A13DMAREQCAPC0				
	DMA request at match B1 register	T32A13DMAREQCMPB1	***[TSEL0CR7]*** <INSEL31[2:0]>	31	✓	-
	DMA request at capture B0 register	T32A13DMAREQCAPB0				

Note1: ✓: Available, -: Not available.

Note2: There is no DMA request for ch14 and ch15.

2.15. Real Time Clock (RTC)

2.15.1. Built-in List

The following table shows the built-in list for each product.

Table 2.72 RTC Built-in List

Product	Built-in RTC (✓: Available, -: N/A)
M4GR	✓
M4GQ	✓
M4GN	✓

2.15.2. Function Pin and Port

The functional pin is assigned to the following ports.

Table 2.73 RTC Function Pin and Port

Function pin		Port	Product table (✓: Available, -: N/A)		
			M4GR	M4GQ	M4GN
ALARM_N	Output	PG2	✓	✓	✓
RTCOUT	Output	PT3	✓	✓	✓

2.15.3. Count clock

The clock shown in the table below is used as the count clock.

Table 2.74 RTC Count Clock

Count clock
fs

2.16. Long Term Timer (LTTMR)

2.16.1. Built-in Channel

The built-in channel for each product is shown in the following table.

Table 2.75 LTTMR Built-in Channel

Product	LTTMR built-in channel (✓: Available, -: N/A)
	Channel 0
M4GR	✓
M4GQ	✓
M4GN	✓

2.16.2. Count Clock

The following clock is used as the count clock in the LTTMR.

Table 2.76 LTTMR Count Clock

Clock	Signal name
Internal high-speed oscillator 2 clock (Note)	f_{IHOSC2}

Note: The oscillation control register is ***[RLMLOSCCR]***<POSCEN>.

2.16.3. Internal Signal Connection Specification

2.16.3.1. CEC/RMC Connection

Table 2.77 LTTMR CEC/RMC Connection: Output

Channel	Function output		Input signal		
		Signal name	Peripheral function		Signal name
ch0	LTTMR0 interrupt	INTLTTMR0	CEC ch0	Timer trigger 0 for clock source	CEC0CLKTRG
			RMC ch0	Timer trigger 0 for clock source	TB0OUT
			RMC ch1	Timer trigger 1 for clock source	TB1OUT

2.17. Universal Asynchronous Receiver Transmitter (UART)

2.17.1. Built-in Channel

The built-in channel for each product is shown in the following table.
In TMPM4G Group (1), maximum communication speed of UART is 5.0 Mbps.

Table 2.78 UART Built-in Channel

Product	UART built-in channel (✓: Available, -: N/A)					
	ch0	ch1	ch2	ch3	ch4	ch5
M4GR	✓	✓	✓	✓	✓	✓
M4GQ	✓	✓	✓	✓	✓	-
M4GN	✓	✓	✓	-	-	-

2.17.2. Function Pin and Port

The functional pin is assigned to the port of the following table.
Please use exclusively the same functional pin currently assigned to plurality.

Table 2.79 UART Function Pin and Port

Channel	Function pin		Port	Product table (✓: Available, -: N/A)		
				M4GR	M4GQ	M4GN
ch0	UT0RXD	Input	PE2/PH4/PH5	✓/✓/✓	✓/✓/✓	✓/✓/✓
	UT0TXDA	Output	PE3/PH5/PH4	✓/✓/✓	✓/✓/✓	✓/✓/✓
	UT0CTS_N	Input	PE1/PH7/PH6	✓/✓/✓	✓/✓/✓	✓/✓/✓
	UT0RTS_N	Output	PE0/PH6/PH7	✓/✓/✓	✓/✓/✓	✓/✓/✓
ch1	UT1RXD	Input	PH0/PH1/PV4	✓/✓/✓	✓/✓/✓	✓/✓/-
	UT1TXDA	Output	PH1/PH0/PV5	✓/✓/✓	✓/✓/✓	✓/✓/-
	UT1CTS_N	Input	PH3/PH2/PV6	✓/✓/✓	✓/✓/✓	✓/✓/-
	UT1RTS_N	Output	PH2/PH3/PV7	✓/✓/✓	✓/✓/✓	✓/✓/-
ch2	UT2RXD	Input	PG0/PG1	✓/✓	✓/✓	✓/✓
	UT2TXDA	Output	PG1/PG0	✓/✓	✓/✓	✓/✓
	UT2CTS_N	Input	PG3/PG2	✓/✓	✓/✓	✓/✓
	UT2RTS_N	Output	PG2/PG3	✓/✓	✓/✓	✓/✓
ch3	UT3RXD	Input	PU6/PV0/PV1	✓/✓/✓	-/✓/✓	-/-/-
	UT3TXDA	Output	PU7/PV1/PV0	✓/✓/✓	-/✓/✓	-/-/-
	UT3CTS_N	Input	PU5/PV3/PV2	✓/✓/✓	-/✓/✓	-/-/-
	UT3RTS_N	Output	PU4/PV2/PV3	✓/✓/✓	-/✓/✓	-/-/-
ch4	UT4RXD	Input	PM0/PM1/PU1	✓/✓/✓	✓/✓/-	-/-/-
	UT4TXDA	Output	PM1/PM0/PU0	✓/✓/✓	✓/✓/-	-/-/-
	UT4CTS_N	Input	PM3/PM2/PU2	✓/✓/✓	✓/✓/-	-/-/-
	UT4RTS_N	Output	PM2/PM3/PU3	✓/✓/✓	✓/✓/-	-/-/-
ch5	UT5RXD	Input	PJ0/PJ1	✓/✓	-/-	-/-
	UT5TXDA	Output	PJ1/PJ0	✓/✓	-/-	-/-
	UT5CTS_N	Input	PJ3/PJ2	✓/✓	-/-	-/-
	UT5RTS_N	Output	PJ2/PJ3	✓/✓	-/-	-/-

Note: TMPM4G Group (1) does not have UTxTXDB pin.

2.17.3. Half Clock Mode Support List for Each Product

The half clock mode support is shown in the table below.
The TMPM4G Group (1) supports only 1-pin mode.

Table 2.80 UART Half Clock Mode (1-pin mode) Support List

Channel	Product table (✓: Available, -: N/A)		
	M4GR	M4GQ	M4GN
ch0	✓	✓	✓
ch1	✓	✓	✓
ch2	✓	✓	✓
ch3	✓	✓	-
ch4	✓	✓	-
ch5	✓	-	-

2.17.4. Clock for Prescaler

The clock shown in the table below is used as the prescaler clock for UART.

Table 2.81 UART Clock for Prescaler

Clock for prescaler
ΦT0m

2.17.5. DMA Request

The following table shows the DMA request in the UART
The request from MDMAC is always a single transfer request regardless of the fill level in the FIFO.

Table 2.82 UART DMA Request

Channel	Request		Trigger selector	DMA request channel (MDMAC unit A)		
		Signal name			Single transfer	Burst transfer
ch0	Reception DMA request	UART0RX_DMAREQ	***[TSEL0CR1]*** <INSEL7[2:0]>	7	✓	-
			[TSEL0CR4] <INSEL18[2:0]>	18	✓	-
	Transmission DMA request	UART0TX_DMAREQ	***[TSEL0CR2]*** <INSEL9[2:0]>	9	✓	-
			[TSEL0CR5] <INSEL20[2:0]>	20	✓	-
ch1	Reception DMA request	UART1RX_DMAREQ	***[TSEL0CR2]*** <INSEL11[2:0]	11	✓	-
			[TSEL0CR5] <INSEL22[2:0]>	22	✓	-
	Transmission DMA request	UART1TX_DMAREQ	***[TSEL0CR3]*** <INSEL13[2:0]>	13	✓	-
			[TSEL0CR5] <INSEL23[2:0]>	23	✓	-
ch2	Reception DMA request	UART2RX_DMAREQ	***[TSEL0CR4]*** <INSEL19[2:0]>	19	✓	-
			[TSEL0CR6] <INSEL24[2:0]>	24	✓	-
	Transmission DMA request	UART2TX_DMAREQ	***[TSEL0CR5]*** <INSEL21[2:0]>	21	✓	-
			[TSEL0CR6] <INSEL25[2:0]>	25	✓	-
ch3	Reception DMA request	UART3RX_DMAREQ	***[TSEL0CR7]*** <INSEL28[2:0]>	28	✓	-
	Transmission DMA request	UART3TX_DMAREQ	***[TSEL0CR7]*** <INSEL29[2:0]>	29	✓	-
ch4	Reception DMA request	UART4RX_DMAREQ	***[TSEL0CR0]*** <INSEL0[2:0]>	0	✓	-
	Transmission DMA request	UART4TX_DMAREQ	***[TSEL0CR0]*** <INSEL1[2:0]>	1	✓	-
ch5	Reception DMA request	UART5RX_DMAREQ	***[TSEL0CR7]*** <INSEL30[2:0]>	30	✓	-
	Transmission DMA request	UART5TX_DMAREQ	***[TSEL0CR7]*** <INSEL31[2:0]>	31	✓	-

Note: ✓: Available, -: Not available.

2.17.6. Internal Signal Connection Specification

The UART has the transmission function started by a trigger signal.
The trigger signal is selected from among the trigger sources in the following tables by the trigger selector.

2.17.6.1. Trigger Transmission Signal Connection Specification

Table 2.83 UART Trigger Transmission Signal Connection Specification: Input

Channel	Signal name	Input trigger signal	
			Signal name
ch0	UART0TRGIN	T32A ch0 internal trigger (Register A1 match)	T32A00TRGOUTCMPA1
ch1	UART1TRGIN	T32A ch1 internal trigger (Register A1 match)	T32A01TRGOUTCMPA1
ch2	UART2TRGIN	T32A ch2 internal trigger (Register A1 match)	T32A02TRGOUTCMPA1

Table 2.84 UART Internal Signal Connection Specification: Output

Channel	Function output		Output destination		
		Signal name	Trigger selector		Signal name
ch0	Transmission completion trigger	UART0TXTRG	***[TSEL0CR11]*** <INSEL46[2:0]>	T32A ch0 timer A	T32A00TRGINAPCK
	Reception completion trigger	UART0RXTRG	***[TSEL0CR11]*** <INSEL47[2:0]>	T32A ch0 timer B	T32A00TRGINBPCK
ch1	Transmission completion trigger	UART1TXTRG	***[TSEL0CR12]*** <INSEL48[2:0]>	T32A ch1 timer A	T32A01TRGINAPCK
	Reception completion trigger	UART1RXTRG	***[TSEL0CR12]*** <INSEL49[2:0]>	T32A ch1 timer B	T32A01TRGINBPCK
ch2	Transmission completion trigger	UART2TXTRG	***[TSEL0CR12]*** <INSEL50[2:0]>	T32A ch2 timer A	T32A02TRGINAPCK
	Reception completion trigger	UART2RXTRG	***[TSEL0CR12]*** <INSEL51[2:0]>	T32A ch2 timer B	T32A02TRGINBPCK
ch3	Transmission completion trigger	UART3TXTRG	***[TSEL0CR13]*** <INSEL52[2:0]>	T32A ch3 timer A	T32A03TRGINAPCK
	Reception completion trigger	UART3RXTRG	***[TSEL0CR13]*** <INSEL53[2:0]>	T32A ch3 timer B	T32A03TRGINBPCK
ch4	Transmission completion trigger	UART4TXTRG	***[TSEL0CR13]*** <INSEL54[2:0]>	T32A ch4 timer A	T32A04TRGINAPCK
	Reception completion trigger	UART4RXTRG	***[TSEL0CR13]*** <INSEL55[2:0]>	T32A ch4 timer B	T32A04TRGINBPCK
ch5	Transmission completion trigger	UART5TXTRG	***[TSEL0CR9]*** <INSEL39[2:0]>	T32A ch5 timer A	T32A05TRGINAPCK
	Reception completion trigger	UART5RXTRG	***[TSEL0CR10]*** <INSEL40[2:0]>	T32A ch5 timer B	T32A05TRGINBPCK

2.18. Full Universal Asynchronous Receiver Transmitter (FUART)

2.18.1. Built-in Channel

The built-in channel for each product is shown in the following table.
In the TMPM4G Group (1), Maximum Communication speed of FUART is 2.5 Mbps.

Table 2.85 FUART Built-in Channel

Product	FUART built-in channel (✓: Available, -: N/A)	
	ch0	ch1
M4GR	✓	✓
M4GQ	✓	✓
M4GN	✓	-

2.18.2. Function Pin and Port

The functional pin is assigned to the port of the following table.
Please use exclusively the same functional pin currently assigned to plurality.

Table 2.86 FUART Function Pin and Port

Channel	Function pin		Port	Product table (✓: Available, -: N/A)		
				M4GR	M4GQ	M4GN
ch0	FUT0RXD	Output	PG5/PJ5	✓/✓	✓/-	✓/-
	FUT0TXD	Input	PG4/PJ4	✓/✓	✓/-	✓/-
	FUT0CTS_N	Input	PG7	✓	✓	✓
	FUT0RTS_N	Output	PG6	✓	✓	✓
	FUT0IROUT	Output	PG4	✓	✓	✓
	FUT0IRIN	Input	PG5	✓	✓	✓
ch1	FUT1RXD	Output	PJ7/PM6	✓/✓	-/✓	-/-
	FUT1TXD	Input	PJ6/PM7	✓/✓	-/✓	-/-
	FUT1CTS_N	Input	PM4	✓	✓	-
	FUT1RTS_N	Output	PM5	✓	✓	-
	FUT1IROUT	Output	PM7	✓	✓	-
	FUT1IRIN	Input	PM6	✓	✓	-

2.18.3. Clock for Prescaler

The clock shown in the table below is used as the prescaler clock for FUART.

Table 2.87 FUART Clock for Prescaler

Clock for prescaler
ΦT0m

2.18.4. DMA Request

The following table shows the DMA request in the FUART.
The request from MDMAC is always a single transfer request regardless of the fill level in the FIFO.

Table 2.88 FUART DMA Request

Channel	Request		Trigger selector	DMA request channel (MDMAC unit A)		
		Signal name			Single transfer	Burst transfer
ch0	Reception DMA request	FUART0RX_DMAREQ	***[TSEL0CR4]*** <INSEL17[2:0]>	17	✓	-
	Transmission DMA request	FUART0TX_DMAREQ	***[TSEL0CR3]*** <INSEL15[2:0]>	15	✓	-
ch1	Reception DMA request	FUART1RX_DMAREQ	***[TSEL0CR0]*** <INSEL2[2:0]>	2	✓	-
	Transmission DMA request	FUART1TX_DMAREQ	***[TSEL0CR0]*** <INSEL3[2:0]>	3	✓	-

Note: ✓: Available, -: Not available.

2.19. I²C Interface (I2C)

2.19.1. Built-in Channel

The built-in channel for each product is shown in the following table.
In TMPM4G Group (1), the I2C supports Standard-mode and Fast-mode.

Table 2.89 I2C Built-in Channel

Product	I2C built-in channel (✓: Available, -: N/A)				
	ch0	ch1	ch2	ch3	ch4
M4GR	✓	✓	✓	✓	✓
M4GQ	✓	✓	✓	✓	✓
M4GN	✓	✓	✓	-	-

2.19.2. Function Pin and Port

The functional pin is assigned to the port of the following table.
Please use exclusively the same functional pin currently assigned to plurality.

Table 2.90 I2C Function Pin and Port

Channel	Function pin		Port	Product table (✓: Available, -: N/A)		
				M4GR	M4GQ	M4GN
ch0	I2C0SCL	I/O	PG3	✓	✓	✓
	I2C0SDA	I/O	PG2	✓	✓	✓
ch1	I2C1SCL	I/O	PF3	✓	✓	✓
	I2C1SDA	I/O	PF2	✓	✓	✓
ch2	I2C2SCL	I/O	PG5/PV4	✓/✓	✓/✓	✓/-
	I2C2SDA	I/O	PG4/PV5	✓/✓	✓/✓	✓/-
ch3	I2C3SCL	I/O	PJ7/PM1	✓/✓	-/✓	-/-
	I2C3SDA	I/O	PJ6/PM0	✓/✓	-/✓	-/-
ch4	I2C4SCL	I/O	PJ2/PM7	✓/✓	-/✓	-/-
	I2C4SDA	I/O	PJ3/PM6	✓/✓	-/✓	-/-

2.19.3. Clock for Prescaler

The I2C use the clock of following table as a prescaler clock.

Table 2.91 I2C Clock for Prescaler

Clock for prescaler
fsysm

2.19.4. Communication Speed

The communication speed of each channel is shown in the table below.

Table 2.92 I2C Communication Speed

Channel	Communication speed (✓: Available, -: N/A)	
	Standard-mode (up to 100kbps)	Fast-mode (up to 400kbps)
ch0	✓	✓
ch1	✓	✓
ch2	✓	✓
ch3	✓	✓
ch4	✓	✓

2.19.5. Wakeup Function

TMPM4G Group (1) does not support I2C wakeup function.

2.19.6. Noise Filter Selection

The channel 0 to 4 do not include an analog filter. Always use the digital filter.

Table 2.93 I2C Filter Selection

Channel	Filter selection: ***[I2CxOP]***<NFSEL>
ch0	Digital (0)
ch1	Digital (0)
ch2	Digital (0)
ch3	Digital (0)
ch4	Digital (0)

2.19.7. DMA Request

The following table shows the DMA request in the I2C.

Table 2.94 I2C DMA Request

Channel	Request		Trigger selector	DMA request channel (MDMAC unit A)		
		Signal name			Single transfer	Burst transfer
ch0	Receiving DMA request	I2C0RXDMAREQ	***[TSEL0CR1]*** <INSEL7[2:0]>	7	✓	-
	Transmitting DMA request	I2C0TXDMAREQ	***[TSEL0CR2]*** <INSEL9[2:0]>	9	✓	-
ch1	Receiving DMA request	I2C1RXDMAREQ	***[TSEL0CR2]*** <INSEL11[2:0]>	11	✓	-
	Transmitting DMA request	I2C1TXDMAREQ	***[TSEL0CR3]*** <INSEL13[2:0]>	13	✓	-
ch2	Receiving DMA request	I2C2RXDMAREQ	***[TSEL0CR4]*** <INSEL17[2:0]>	17	✓	-
	Transmitting DMA request	I2C2TXDMAREQ	***[TSEL0CR3]*** <INSEL15[2:0]>	15	✓	-
ch3	Receiving DMA request	I2C3RXDMAREQ	***[TSEL0CR0]*** <INSEL0[2:0]>	0	✓	-
	Transmitting DMA request	I2C3TXDMAREQ	***[TSEL0CR0]*** <INSEL1[2:0]>	1	✓	-
ch4	Receiving DMA request	I2C4RXDMAREQ	***[TSEL0CR0]*** <INSEL2[2:0]>	2	✓	-
	Transmitting DMA request	I2C4TXDMAREQ	***[TSEL0CR0]*** <INSEL3[2:0]>	3	✓	-

Note: ✓: Available, -: Not available.

2.20. I²C Interface Version A (EI2C)

2.20.1. Built-in Channel

The built-in channel for each product is shown in the following table.
In TMPM4G Group (1), the EI2C supports Standard-mode, Fast-mode and Fast-mode Plus.

Table 2.95 EI2C Built-in Channel

Product	EI2C built-in channel (✓: Available, -: N/A)				
	ch0	ch1	ch2	ch3	ch4
M4GR	✓	✓	✓	✓	✓
M4GQ	✓	✓	✓	✓	✓
M4GN	✓	✓	✓	-	-

2.20.2. Function Pin and Port

The functional pin is assigned to the port of the following table.
Please use exclusively the same functional pin currently assigned to plurality.

Table 2.96 EI2C Function Pin and Port

Channel	Function pin		Port	Product table (✓: Available, -: N/A)		
				M4GR	M4GQ	M4GN
ch0	EI2C0SCL	I/O	PG3	✓	✓	✓
	EI2C0SDA	I/O	PG2	✓	✓	✓
ch1	EI2C1SCL	I/O	PF3	✓	✓	✓
	EI2C1SDA	I/O	PF2	✓	✓	✓
ch2	EI2C2SCL	I/O	PG5/PV4	✓/✓	✓/✓	✓/-
	EI2C2SDA	I/O	PG4/PV5	✓/✓	✓/✓	✓/-
ch3	EI2C3SCL	I/O	PJ7/PM1	✓/✓	-/✓	-/-
	EI2C3SDA	I/O	PJ6/PM0	✓/✓	-/✓	-/-
ch4	EI2C4SCL	I/O	PJ2/PM7	✓/✓	-/✓	-/-
	EI2C4SDA	I/O	PJ3/PM6	✓/✓	-/✓	-/-

2.20.3. Clock for Prescaler

The EI2C use the clock of following table as a prescaler clock.

Table 2.97 EI2C Clock for Prescaler

Clock for prescaler
fsysm

2.20.4. Communication Speed

The communication speed of each channel is shown in the table below.

Table 2.98 EI2C Communication Speed

Channel	Communication speed (✓: Available, -: N/A)		
	Standard-mode (up to 100kbps)	Fast-mode (up to 400kbps)	Fast-mode Plus (up to 1Mbps)
ch0	✓	✓	✓
ch1	✓	✓	✓
ch2	✓	✓	-
ch3	✓	✓	-
ch4	✓	✓	-

2.20.5. Wakeup Function

TMPM4G Group (1) does not support EI2C wakeup function.

2.20.6. Noise Filter Selection

Table 2.99 EI2C Filter Selection

Channel	Filter selection: ***[I2CxACR0]***<NFSEL>
ch0	Digital (0)/Analog (1)
ch1	Digital (0)/Analog (1)
ch2	Digital (0)
ch3	Digital (0)
ch4	Digital (0)

2.20.7. DMA Request

The following table shows the DMA request in the EI2C.

Table 2.100 EI2C DMA Request

Channel	Request		Trigger selector	DMA request channel (MDMAC unit A)		
		Signal name			Single transfer	Burst transfer
ch0	Receiving DMA request	I2C0ARXDMAREQ	***[TSEL0CR1]*** <INSEL7[2:0]>	7	✓	-
	Transmitting DMA request	I2C0ATXDMAREQ	***[TSEL0CR2]*** <INSEL9[2:0]>	9	✓	-
ch1	Receiving DMA request	I2C1ARXDMAREQ	***[TSEL0CR2]*** <INSEL11[2:0]>	11	✓	-
	Transmitting DMA request	I2C1ATXDMAREQ	***[TSEL0CR3]*** <INSEL13[2:0]>	13	✓	-
ch2	Receiving DMA request	I2C2ARXDMAREQ	***[TSEL0CR4]*** <INSEL17[2:0]>	17	✓	-
	Transmitting DMA request	I2C2ATXDMAREQ	***[TSEL0CR3]*** <INSEL15[2:0]>	15	✓	-
ch3	Receiving DMA request	I2C3ARXDMAREQ	***[TSEL0CR0]*** <INSEL0[2:0]>	0	✓	-
	Transmitting DMA request	I2C3ATXDMAREQ	***[TSEL0CR0]*** <INSEL1[2:0]>	1	✓	-
ch4	Receiving DMA request	I2C4ARXDMAREQ	***[TSEL0CR0]*** <INSEL2[2:0]>	2	✓	-
	Transmitting DMA request	I2C4ATXDMAREQ	***[TSEL0CR0]*** <INSEL3[2:0]>	3	✓	-

Note: ✓: Available, -: Not available.

2.21. Serial Peripheral Interface (TSPI)

2.21.1. Built-in Channel

The built-in channel for each product is shown in the following table.

In the TMPM4G Group (1), maximum communication speed of TSPI is 25 Mbps for channel 0 to 3 and 10Mbps for channel 4 to 8.

Table 2.101 TSPI Built-in Channel

Product	TSPI built-in channel (✓: Available, -: N/A)								
	ch0	ch1	ch2	ch3	ch4	ch5	ch6	ch7	ch8
M4GR	✓	✓	✓	✓	✓	✓	✓	✓	✓
M4GQ	✓	✓	✓	✓	✓	✓	✓	✓	-
M4GN	✓	✓	✓	✓	✓	-	-	-	-

2.21.2. Function Pin and Port

The functional pin is assigned to the port of the following tables.
Please use exclusively the same functional pin currently assigned to plurality.

Table 2.102 TSPI Function Pin and Port (1/2)

Channel	Function pin		Port	Product table (✓: Available, -: N/A)		
				M4GR	M4GQ	M4GN
ch0	TSPI0CSIN	Input	PA0	✓	✓	✓
	TSPI0CS0	Output	PA0	✓	✓	✓
	TSPI0CS1	Output	PA4	✓	✓	✓
	TSPI0CS2	Output	PA5	✓	✓	✓
	TSPI0CS3	Output	PA6	✓	✓	✓
	TSPI0RXD	Input	PA2	✓	✓	✓
	TSPI0TXD	Output	PA3	✓	✓	✓
	TSPI0SCK	I/O	PA1	✓	✓	✓
ch1	TSPI1CSIN	Input	PL0	✓	✓	✓
	TSPI1CS0	Output	PL0	✓	✓	✓
	TSPI1CS1	Output	PK4	✓	✓	✓
	TSPI1CS2	Output	PK5	✓	✓	✓
	TSPI1CS3	Output	PK6	✓	✓	✓
	TSPI1RXD	Input	PL2	✓	✓	✓
	TSPI1TXD	Output	PL3	✓	✓	✓
	TSPI1SCK	I/O	PL1	✓	✓	✓
ch2	TSPI2CSIN	Input	PA7/PF7	✓/✓	✓/✓	✓/✓
	TSPI2CS0	Output	PA7/PF7	✓/✓	✓/✓	✓/✓
	TSPI2CS1	Output	PA3	✓	✓	✓
	TSPI2CS2	Output	-	-	-	-
	TSPI2CS3	Output	-	-	-	-
	TSPI2RXD	Input	PA5	✓	✓	✓
	TSPI2TXD	Output	PA4	✓	✓	✓
	TSPI2SCK	I/O	PA6	✓	✓	✓
ch3	TSPI3CSIN	Input	PK1/PK7	✓/✓	✓/✓	✓/✓
	TSPI3CS0	Output	PK1/PK7	✓/✓	✓/✓	✓/✓
	TSPI3CS1	Output	PL3	✓	✓	✓
	TSPI3CS2	Output	-	-	-	-
	TSPI3CS3	Output	-	-	-	-
	TSPI3RXD	Input	PK5	✓	✓	✓
	TSPI3TXD	Output	PK4	✓	✓	✓
	TSPI3SCK	I/O	PK6	✓	✓	✓

Table 2.103 TSPI Function Pin and Port (2/2)

Channel	Function pin		Port	Product table (✓: Available, -: N/A)		
				M4GR	M4GQ	M4GN
ch4	TSPI4CSIN	Input	PD0	✓	✓	✓
	TSPI4CS0	Output	PD0	✓	✓	✓
	TSPI4CS1	Output	-	-	-	-
	TSPI4CS2	Output	-	-	-	-
	TSPI4CS3	Output	-	-	-	-
	TSPI4RXD	Input	PD2	✓	✓	✓
	TSPI4TXD	Output	PD3	✓	✓	✓
	TSPI4SCK	I/O	PD1	✓	✓	✓
ch5	TSPI5CSIN	Input	PV7	✓	✓	-
	TSPI5CS0	Output	PV7	✓	✓	-
	TSPI5CS1	Output	-	-	-	-
	TSPI5CS2	Output	-	-	-	-
	TSPI5CS3	Output	-	-	-	-
	TSPI5RXD	Input	PV4	✓	✓	-
	TSPI5TXD	Output	PV5	✓	✓	-
	TSPI5SCK	I/O	PV6	✓	✓	-
ch6	TSPI6CSIN	Input	PM3	✓	✓	-
	TSPI6CS0	Output	PM3	✓	✓	-
	TSPI6CS1	Output	-	-	-	-
	TSPI6CS2	Output	-	-	-	-
	TSPI6CS3	Output	-	-	-	-
	TSPI6RXD	Input	PM1	✓	✓	-
	TSPI6TXD	Output	PM0	✓	✓	-
	TSPI6SCK	I/O	PM2	✓	✓	-
ch7	TSPI7CSIN	Input	PM4	✓	✓	-
	TSPI7CS0	Output	PM4	✓	✓	-
	TSPI7CS1	Output	-	-	-	-
	TSPI7CS2	Output	-	-	-	-
	TSPI7CS3	Output	-	-	-	-
	TSPI7RXD	Input	PM6	✓	✓	-
	TSPI7TXD	Output	PM7	✓	✓	-
	TSPI7SCK	I/O	PM5	✓	✓	-
ch8	TSPI8CSIN	Input	PW0	✓	-	-
	TSPI8CS0	Output	PW0	✓	-	-
	TSPI8CS1	Output	-	-	-	-
	TSPI8CS2	Output	-	-	-	-
	TSPI8CS3	Output	-	-	-	-
	TSPI8RXD	Input	PW2	✓	-	-
	TSPI8TXD	Output	PW3	✓	-	-
	TSPI8SCK	I/O	PW1	✓	-	-

2.21.3. Transfer Mode Support List for Each Product

The transfer modes which can be used with the product as TSPI is shown in the following table differ.

Table 2.104 TSPI Transfer Mode Support List

Channel	Mode support (-: Not supported)		
	M4GR	M4GQ	M4GN
ch0	SPI mode SIO mode		
ch1	SPI mode SIO mode		
ch2	SPI mode SIO mode		
ch3	SPI mode SIO mode		
ch4	SPI mode SIO mode		
ch5	SPI mode SIO mode		-
ch6	SPI mode SIO mode		-
ch7	SPI mode SIO mode		-
ch8	SPI mode SIO mode	-	-

2.21.4. *[TSPIxCR2]*<RXDLY> Setting Value

Set the setting value of TSPI control register 2 (***[TSPIxCR2]***<RXDLY[2:0]>) for AC timing adjustment.

Refer to the AC electrical characteristics of the serial peripheral interface in "Data sheet" and set according to the AC timing.

2.21.5. Clock for Prescaler

The clock shown in the table below is used as the prescaler clock for TSPI.

Table 2.105 TSPI Clock for Prescaler

TSPI channel	Clock for prescaler
ch0 to 5	ΦT0h
ch6 to 8	ΦT0m

2.21.6. DMA Request

The following table shows the DMA request in the TSPI.
The request from MDMAC is always a single transfer request regardless of the fill level in the FIFO.

Table 2.106 TSPI DMA Request

Channel	Request		Trigger selector	DMA request channel			
		Signal name				Single transfer	Burst transfer
ch0	Receive DMA request	TSPI0RX_DMA	-	HDMAC unit A	0	✓	✓
	Transmit DMA request	TSPI0TX_DMA			1	✓	✓
ch1	Receive DMA request	TSPI1RX_DMA	-	HDMAC unit B	0	✓	✓
	Transmit DMA request	TSPI1TX_DMA			1	✓	✓
ch2	Receive DMA request	TSPI2RX_DMA	-	HDMAC unit A	2	✓	✓
	Transmit DMA request	TSPI2TX_DMA			3	✓	✓
ch3	Receive DMA request	TSPI3RX_DMA	-	HDMAC unit B	2	✓	✓
	Transmit DMA request	TSPI3TX_DMA			3	✓	✓
ch4	Receive DMA request	TSPI4RX_DMA	-	HDMAC unit A	4	✓	✓
	Transmit DMA request	TSPI4TX_DMA			5	✓	✓
ch5	Receive DMA request	TSPI5RX_DMA	-	HDMAC unit B	4	✓	✓
	Transmit DMA request	TSPI5TX_DMA			5	✓	✓
ch6	Receive DMA request	TSPI6RX_DMA	***[TSEL0CR0]*** <INSEL0[2:0]>	MDMAC unit A	0	✓	×
	Transmit DMA request	TSPI6TX_DMA	***[TSEL0CR0]*** <INSEL1[2:0]>		1	✓	×
ch7	Receive DMA request	TSPI7RX_DMA	***[TSEL0CR0]*** <INSEL2[2:0]>		2	✓	×
	Transmit DMA request	TSPI7TX_DMA	***[TSEL0CR0]*** <INSEL3[2:0]>		3	✓	×
ch8	Receive DMA request	TSPI8RX_DMA	***[TSEL0CR1]*** <INSEL4[2:0]>		4	✓	×
	Transmit DMA request	TSPI8TX_DMA	***[TSEL0CR1]*** <INSEL5[2:0]>		5	✓	×

Note: ✓: Available, ×: Not available, -: No trigger selector

2.21.7. Internal Signal Connection Specification

2.21.7.1. Trigger Transmission Signal Connection Specification

The TSPI has the transmission function started by a trigger signal.

Table 2.107 TSPI Trigger Transmission Signal Connection Specification: Input

Channel	Signal name	Trigger source	
			Signal name
ch0	TSPI0TRG	T32A ch0 timer register A1 match trigger	T32A00TRGOUTCMPA1
ch1	TSPI1TRG	T32A ch1 timer register A1 match trigger	T32A01TRGOUTCMPA1
ch2	TSPI2TRG	T32A ch2 timer register A1 match trigger	T32A02TRGOUTCMPA1
ch3	TSPI3TRG	T32A ch3 timer register A1 match trigger	T32A03TRGOUTCMPA1
ch4	TSPI4TRG	T32A ch4 timer register A1 match trigger	T32A04TRGOUTCMPA1

Note: TSPI ch5 to ch8 have no connections.

2.22. Synchronous Serial Interface (TSSI)

2.22.1. Built-in Channel

The built-in channel for each product is shown in the following table.
In the TMPM4G Group (1), maximum communication speed of TSSI is 10Mbps.

Table 2.108 TSSI Built-in Channel

Product	TSSI built-in channel (✓: Available, -: N/A)	
	Channel 0	Channel 1
M4GR	✓	✓
M4GQ	✓	-
M4GN	✓	-

2.22.2. Function Pin and Port

The functional pin is assigned to the port of the following table.

Table 2.109 TSSI Function Pin and Port

Channel	Function pin		Port	Product table (✓: Available, -: N/A)		
				M4GR	M4GQ	M4GN
ch0	TSSI0TCK	Input	PD2	✓	✓	✓
	TSSI0TFS	Output	PD3	✓	✓	✓
	TSSI0TXD	Output	PD4	✓	✓	✓
	TSSI0RCK	Output	PD7	✓	✓	✓
	TSSI0RFS	Output	PD6	✓	✓	✓
	TSSI0RXD	I/O	PD5	✓	✓	✓
ch1	TSSI1TCK	Input	PU2	✓	- (Note)	-
	TSSI1TFS	Output	PU3	✓	- (Note)	-
	TSSI1TXD	Output	PU4	✓	-	-
	TSSI1RCK	Output	PU7	✓	-	-
	TSSI1RFS	Output	PU6	✓	-	-
	TSSI1RXD	I/O	PU5	✓	-	-

Note: The function pin is existing, but it has no corresponding function.

2.22.3. Clock for Divider

The clock shown in the table below is used as the divider clock for TSSI.

Table 2.110 TSSI Clock for Divider

Clock for divider
ΦT0m

2.22.4. DMA Request

The following table shows the DMA request in the TSSI.

Table 2.111 TSSI DMA Request

Channel	Request		Trigger selector	DMA request channel (MDMAC unit A)		
		Signal name			Single transfer	Burst transfer
ch0	Receive DMA request	TSSI0RXDMAREQ	***[TSEL0CR4]*** <INSEL19[2:0]>	19	✓	-
	Transmit DMA request	TSSI0TXDMAREQ	***[TSEL0CR5]*** <INSEL21[2:0]>	21	✓	-
ch1	Receive DMA request	TSSI1RXDMAREQ	***[TSEL0CR6]*** <INSEL26[2:0]>	26	✓	-
	Transmit DMA request	TSSI1TXDMAREQ	***[TSEL0CR6]*** <INSEL27[2:0]>	27	✓	-

Note: ✓: Available, -: Not available.

2.23. I²S Interface (I2S)

2.23.1. Built-in Channel

The built-in channel for each product is shown in the following table.

Table 2.112 I2S Built-in Channel

Product	I2S built-in channel (✓: Available, -: N/A)	
	ch0	ch1
M4GR	✓	✓
M4GQ	✓	✓
M4GN	✓	✓

2.23.2. Function Pin and Port

The functional pin is assigned to the port of the following table.
Please use exclusively the same functional pin currently assigned to plurality.

Table 2.113 I2S Function Pin and Port

Channel	Function pin		Port	Product table (✓: Available, -: N/A)		
				M4GR	M4GQ	M4GN
ch0	I2S0LRCK	I/O	PB4/PD4	✓/✓	✓/✓	✓/✓
	I2S0BCK	I/O	PB5/PD5	✓/✓	✓/✓	✓/✓
	I2S0DI	Input	PB6/PD6	✓/✓	✓/✓	✓/✓
	I2S0DO	Output	PB7/PD7	✓/✓	✓/✓	✓/✓
	I2S0MCLK	I/O	PB0	✓	✓	✓
ch1	I2S1LRCK	I/O	PC3/PE7	✓/✓	✓/✓	-/✓
	I2S1BCK	I/O	PC2/PE6	✓/✓	✓/✓	-/✓
	I2S1DI	Input	PC1/PE5	✓/✓	✓/✓	-/✓
	I2S1DO	Output	PC0/PE4	✓/✓	✓/✓	-/✓
	I2S1MCLK	I/O	PG6	✓	✓	✓

2.23.3. Source Clock for Master Clock Generation Circuit

The clock shown in the table below is used as source clock for the master clock generation circuit of I2S.

Table 2.114 I2S Source Clock for Master Clock Generation Circuit

Source clock for master clock generation circuit
ΦT0m

2.23.4. DMA Request

The following table shows the DMA request in the I2S.

Table 2.115 I2S DMA Request

Channel	Request		Trigger selector	DMA request channel (MDMAC unit A)		
		Signal name			Single transfer	Burst transfer
ch0	Receiving DMA request	I2S0RXDMAREQ	***[TSEL0CR0]*** <INSEL0[2:0]>	0	✓	-
	Transmitting DMA request	I2S0TXDMAREQ	***[TSEL0CR0]*** <INSEL1[2:0]>	1	✓	-
ch1	Receiving DMA request	I2S1RXDMAREQ	***[TSEL0CR0]*** <INSEL2[2:0]>	2	✓	-
	Transmitting DMA request	I2S1TXDMAREQ	***[TSEL0CR0]*** <INSEL3[2:0]>	3	✓	-

Note: ✓: Available, -: Not available.

2.23.5. Internal Signal Connection Specification

2.23.5.1. FIFO Threshold Signal Connection Specification

I2S requests FIR to start calculation by the FIFO threshold signal.

Table 2.116 I2S FIFO Threshold Signal Connection Specification: Output

Channel	Function output		Output destination		
		Signal name	Trigger selector		Signal name
ch0	Receive FIFO threshold signal	I2S0RXFIFOTH	***[TSEL0CR14]*** <INSEL56[2:0]>	FIR arithmetic start trigger signal	FIRSTARTTRG
	Transmit FIFO threshold signal	I2S0TXFIFOTH			
ch1	Receive FIFO threshold signal	I2S1RXFIFOTH			
	Transmit FIFO threshold signal	I2S1TXFIFOTH			

2.24. FIR calculation Circuit (FIR)

2.24.1. Built-in List

The following table shows the built-in list for each product.

Table 2.117 FIR Built-in List

Product	built-in FIR (✓: Available, -: N/A)
M4GR	✓
M4GQ	✓
M4GN	✓

2.24.2. DMA Request

The following table shows the DMA request in the FIR.

Table 2.118 FIR DMA Request

Request		Trigger selector	DMA request channel (MDMAC unit A)		
	Signal name			Single transfer	Burst transfer
Input data write request	FIRDATAWRDMAREQ	***[TSEL0CR1]*** <INSEL4[2:0]>	4	✓	-
Arithmetic result data read request	FIRDATARDDMAREQ	***[TSEL0CR1]*** <INSEL5[2:0]>	5	✓	-

Note: ✓: Available, -: Not available.

2.24.3. Internal Signal Connection Specification

2.24.3.1. Arithmetic Start Trigger Signal

The FIR has the function to start calculation by the trigger signal from the I2S.
Select the trigger signal from the trigger sources is shown in the table below with the trigger selector.

Table 2.119 FIR Arithmetic Start Trigger Signal Connection Specification: Input

Function input		Trigger selector	Trigger source	
	Signal name			Signal name
Arithmetic start trigger signal	FIRSTARTTRG	***[TSEL0CR14]*** <INSEL56[2:0]>	I2S ch0	I2S0RXFIFOTH
			I2S ch0	I2S0TXFIFOTH
			I2S ch1	I2S0RXFIFOTH
			I2S ch1	I2S0TXFIFOTH

2.25. Serial Memory Interface (SMIF)

2.25.1. Built-in Channel

The built-in channel for each product is shown in the following table.

Table 2.120 SMIF Built-in Channel

Product	SMIF built-in channel (✓: Available, -: N/A)
	ch0
M4GR	✓
M4GQ	✓
M4GN	✓

2.25.2. Function Pin and Port

The functional pin is assigned to the port of the following table.

Table 2.121 SMIF Function Pin and Port

Channel	Function pin		Port	Product table (✓: Available, -: N/A)		
				M4GR	M4GQ	M4GN
ch0	SMI0CS1_N	Output	PK0	✓	✓	✓
	SMI0D0	I/O	PK2	✓	✓	✓
	SMI0D1	I/O	PK3	✓	✓	✓
	SMI0D2	I/O	PK4	✓	✓	✓
	SMI0D3	I/O	PK5	✓	✓	✓
	SMI0D4	I/O	PL0	✓	✓	✓
	SMI0D5	I/O	PL1	✓	✓	✓
	SMI0D6	I/O	PL2	✓	✓	✓
	SMI0D7	I/O	PL3	✓	✓	✓
	SMI0CLK	Output	PK6	✓	✓	✓
	SMI0CS0_N	Output	PK7	✓	✓	✓

2.25.3. Capacity of Primary and Secondary Buffer

The table below shows the primary and secondary buffer capacities of SMIF in the TMPM4G Group (1).

Table 2.122 SMIF Capacity of Buffer

Channel	Primary buffer	Secondary buffer
ch0	32 bytes	256 bytes

2.25.4. DMA Request

The following table shows the DMA request in the SMIF.

Table 2.123 SMIF DMA Request

Channel	Request		DMA request channel (HDMAC unit A)		
		Signal name		Single transfer	Burst transfer
ch0	SMIF interrupt	INTSMI0	6	-	✓

Note: ✓: Available, -: Not available

2.26. Consumer Electronics Control Circuit (CEC)

2.26.1. Built-in Channel

The built-in channel for each product is shown in the following table.

Table 2.124 CEC Built-in Channel

Product	CEC built-in channel (✓: Available, -: N/A)
	ch0
M4GR	✓
M4GQ	✓
M4GN	✓

2.26.2. Function Pin and Port

The functional pin is assigned to the port of the following table.

Table 2.125 CEC Function Pin and Port

Channel	Function pin		Port	Product table (✓: Available, -: N/A)		
				M4GR	M4GQ	M4GN
ch0	CEC0	I/O	PT2	✓	✓	✓

2.26.3. Sampling Clock

The following clock can be used as the sampling clock for CEC.

Table 2.126 CEC Sampling Clock

Channel	Clock		Clock source	
		Signal name		Signal name
ch0	Low-speed clock	fs	External-low speed oscillator	fs
	Timer trigger 0 for clock source	CEC0CLKTRG	LTTMR0 interrupt	INTLTTMR0

Note: The sampling clock should be selected by ***[CECxFSSEL]***<CECCLK>.

2.27. Remote Control Signal Preprocessor (RMC)

2.27.1. Built-in Channel

The built-in channel for each product is shown in the following table.

Table 2.127 RMC Built-in Channel

Product	RMC built-in channel (✓: Available, -: N/A)	
	ch0	ch1
M4GR	✓	✓
M4GQ	✓	✓
M4GN	✓	-

2.27.2. Function Pin and Port

The functional pin is assigned to the port of the following table.

Table 2.128 RMC Function Pin and Port

Channel	Function pin		Port	Product table (✓: Available, -: N/A)		
				M4GR	M4GQ	M4GN
ch0	RXIN0	Input	PT3	✓	✓	✓
ch1	RXIN1	Input	PT4	✓	✓	-

2.27.3. Sampling Clock

The following clock can be used as the sampling clock for RMC.

Table 2.129 RMC Sampling Clock

Channel	Clock		Clock source	
		Signal name		Signal name
ch0	Low-speed clock	fs	External-low speed oscillator	fs
	Timer trigger 0 for clock source	TB0OUT	LTTMR0 interrupt	INTLTTMR0
ch1	Low-speed clock	fs	External-low speed oscillator	fs
	Timer trigger 1 for clock source	TB1OUT	LTTMR0 interrupt	INTLTTMR0

Note: The sampling clocks should be selected by ***[RMC0FSSEL]***<RMCCLK> and ***[RMC1FSSEL]*** <RMCCLK>.

2.27.4. Internal Signal Connection Specification

2.27.4.1. T32A Connection

Table 2.130 RMC T32A Connection Specification

Channel	Function output		Output destination		
		Signal name	Trigger selector		Signal name
ch0	Trigger output	RMC0TRG	***[TSEL0CR8]*** <INSEL35[2:0]>	T32A13 timer A internal trigger input	T32A13TRGINAPCK
ch1	Trigger output	RMC1TRG	***[TSEL0CR9]*** <INSEL36[2:0]>	T32A13 timer B internal trigger input	T32A13TRGINBPCK

2.28. Digital Noise Filter Circuit (DNF)

2.28.1. Built-in Unit

The built-in unit for each product is shown in the following table.

Table 2.131 DNF Built-in Unit

Product	DNF built-in unit (✓: Available, -: N/A)	
	unit A	unit B
M4GR	✓	✓
M4GQ	✓	✓
M4GN	✓	✓

2.28.2. External Interrupt Pin and DNF

The DNF supports the external interrupt pins as shown in the following tables.

Table 2.132 External Interrupt Pin and DNF (unit A)

External interrupt pin	Port	Unit	Setting register name	Product table (✓: Available, -: N/A)		
				M4GR	M4GQ	M4GN
INT00a	PK7	Unit A	***[DNFAENCR]***<NFEN0>	✓	✓	✓
INT01a	PL0		***[DNFAENCR]***<NFEN1>	✓	✓	✓
INT02a	PA0		***[DNFAENCR]***<NFEN2>	✓	✓	✓
INT03a	PA7		***[DNFAENCR]***<NFEN3>	✓	✓	✓
INT04a	PB0		***[DNFAENCR]***<NFEN4>	✓	✓	✓
INT05a	PB1		***[DNFAENCR]***<NFEN5>	✓	✓	✓
INT06a	PB6		***[DNFAENCR]***<NFEN6>	✓	✓	✓
INT07a	PB7		***[DNFAENCR]***<NFEN7>	✓	✓	✓
INT08a	PG0		***[DNFAENCR]***<NFEN8>	✓	✓	✓
INT09a	PG1		***[DNFAENCR]***<NFEN9>	✓	✓	✓
INT10a	PK0		***[DNFAENCR]***<NFEN10>	✓	✓	✓
INT11a	PK1		***[DNFAENCR]***<NFEN11>	✓	✓	✓
INT12a	PC0		***[DNFAENCR]***<NFEN12>	✓	✓	-
INT13a	PC1		***[DNFAENCR]***<NFEN13>	✓	✓	-
INT14a	PC6		***[DNFAENCR]***<NFEN14>	✓	✓	-
INT15a	PC7		***[DNFAENCR]***<NFEN15>	✓	✓	-

Table 2.133 External Interrupt Pin and DNF (unit B)

External interrupt pin	Port	Unit	Setting register name	Product table (✓: Available, -: N/A)		
				M4GR	M4GQ	M4GN
INT00b	PT3	Unit B	***[DNFBENCR]***<NFEN0>	✓	✓	✓
INT01b	PT4		***[DNFBENCR]***<NFEN1>	✓	✓	-
INT02b	PT5		***[DNFBENCR]***<NFEN2>	✓	✓	-
INT03b	PL6		***[DNFBENCR]***<NFEN3>	✓	-	-
INT04b	PF0		***[DNFBENCR]***<NFEN4>	✓	✓	✓
INT05b	PF7		***[DNFBENCR]***<NFEN5>	✓	✓	✓
INT06b	PU2		***[DNFBENCR]***<NFEN6>	✓	-	-
INT07b	PU3		***[DNFBENCR]***<NFEN7>	✓	-	-
INT08b	PU4		***[DNFBENCR]***<NFEN8>	✓	-	-
INT09b	PU5		***[DNFBENCR]***<NFEN9>	✓	-	-
INT10b	PP6		***[DNFBENCR]***<NFEN10>	✓	✓	✓
INT11b	PP7		***[DNFBENCR]***<NFEN11>	✓	✓	✓
INT12b	PL4		***[DNFBENCR]***<NFEN12>	✓	-	-
INT13b	PL5		***[DNFBENCR]***<NFEN13>	✓	-	-
INT14b	PM3		***[DNFBENCR]***<NFEN14>	✓	✓	-
INT15b	PM4		***[DNFBENCR]***<NFEN15>	✓	✓	-

2.28.3. Sampling Source Clock

The following clock can be used as the sampling source clock for DNF.

Table 2.134 DNF Sampling Source Clock

Sampling source clock
fc

2.29. Interval Sensor Detection Circuit (ISD)

2.29.1. Built-in Unit

The built-in unit for each product is shown in the following table.

Table 2.135 ISD Built-in Unit

Product	ISD built-in unit (✓: Available, -: N/A)		
	unit A	unit B	unit C
M4GR	✓	✓	✓
M4GQ	✓	✓	-
M4GN	✓	-	-

2.29.2. Function Pin and Port

The functional pin is assigned to the port of the following table.

Table 2.136 ISD Function Pin and Port

Unit	Function pin		Port	Product table (✓: Available, -: N/A)		
				M4GR	M4GQ	M4GN
Unit A	ISDAIN0	Input	PE4	✓	✓	✓
	ISDAIN1	Input	PE5	✓	✓	✓
	ISDAIN2	Input	PE6	✓	✓	✓
	ISDAIN3	Input	PE7	✓	✓	✓
	ISDAOUT	Output	PK0	✓	✓	✓
Unit B	ISDBIN0	Input	PV0	✓	✓	-
	ISDBIN1	Input	PV1	✓	✓	-
	ISDBIN2	Input	PV2	✓	✓	-
	ISDBIN3	Input	PV3	✓	✓	-
	ISDBOUT	Output	PK1	✓	✓	- (Note)
Unit C	ISDCIN0	Input	PW4	✓	-	-
	ISDCIN1	Input	PW5	✓	-	-
	ISDCIN2	Input	PW6	✓	-	-
	ISDCIN3	Input	PW7	✓	-	-
	ISDCOUT	Output	PY4	✓	- (Note)	- (Note)

Note: The function pin is existing, but it has no corresponding function.

2.29.3. Reference Clock

The ISD circuit can select the following clocks as a reference clock.

Table 2.137 ISD Reference Clock

Unit	Clock input		Clock source	
		Signal name		Signal name
A	Low-speed clock	fs	External low-speed oscillator	fs
	Timer trigger for clock source	ISDACLKTRG	T32A ch9 timer A output	T32A09OUTA
B	Low-speed clock	fs	External low-speed oscillator	fs
	Timer trigger for clock source	ISDBCLKTRG	T32A ch9 timer A output	T32A09OUTA
C	Low-speed clock	fs	External low-speed oscillator	fs
	Timer trigger for clock source	ISDCCLKTRG	T32A ch9 timer A output	T32A09OUTA

Note: The sampling clock should be selected by ***[ISDxCLKCR]***<SC> in each unit.

2.29.4. Internal Signal Connection Specification

The following table shows the internal signals connected to the ISD.

Table 2.138 ISD Internal Signal Connection Specification

Master			Slave		
Unit	Link operation output		Unit	Link operation input	
		Signal name			Signal name
Unit A	Output timing connection to Slave unit	ISDASDO	Unit B	Output timing connection from Master unit	ISDBSDI
			Unit C	Output timing connection from Master unit	ISDCSDI
	Detection timing connection to Slave unit	ISDATMO	Unit B	Detection timing connection form Master unit	ISDBTMI
			Unit C	Detection timing connection form Master unit	ISDCTMI

2.30. Boundary Scan (BSC)

2.30.1. Built-in List

The following table shows the built-in list for each product.

Table 2.139 BSC Built-in List

Product	Built-in BSC (✓: Available, -: N/A)
M4GR	✓ (Note1)
M4GQ	✓ (Note2)
M4GN	-

Note1: VFBGA177 package product only.
Note2: VFBGA145 package product only.

2.30.2. JTAG Interfaces List for Each Product

Table 2.140 JTAG Interfaces List for Each Product

Debug pin		Port	Product table (✓: Available, -: N/A)		
			M4GR	M4GQ	M4GN
TMS	Input	PH4	✓	✓	✓
TCK	Input	PH5	✓	✓	✓
TDO	Output	PH6	✓	✓	✓
TDI	Input	PH3	✓	✓	✓
TRST_N	Input	PH7	✓	✓	✓
BSC	Input	-	✓ (Note1)	✓ (Note2)	-

Note1: LQFP176 package product is not supported.
Note2: LQFP144 package product is not supported.

2.30.3. Boundary-scan Order

The following tables show the order of the boundary scan for the processor signals in the product.

Table 2.141 Boundary-scan Order (1/4)

Order	Function name or port name	Support (✓: Supported, -: Not supported)	
		M4GR (177-pin product only)	M4GQ (145-pin product only)
-	TDI	✓	✓
1	PH2	✓	✓
2	PH1	✓	✓
3	PH0	✓	✓
4	PG7	✓	✓
5	PG6	✓	✓
6	PG5	✓	✓
7	PG4	✓	✓
8	PL3	✓	✓
9	PL2	✓	✓
10	PL1	✓	✓
11	PL0	✓	✓
12	PK7	✓	✓
13	PK6	✓	✓
14	PK5	✓	✓
15	PK4	✓	✓
16	PK3	✓	✓
17	PK2	✓	✓
18	PK1	✓	✓
19	PK0	✓	✓
20	PV3	✓	✓
21	PV2	✓	✓
22	PV1	✓	✓
23	PV0	✓	✓
24	PT4	✓	✓
25	PW7	✓	-
26	PW6	✓	-
27	PW5	✓	-
28	PW4	✓	-
29	PM3	✓	✓
30	PM2	✓	✓
31	PM1	✓	✓
32	PM0	✓	✓
33	PL5	✓	-
34	PL4	✓	-
35	PG0	✓	✓
36	PG1	✓	✓
37	PG2	✓	✓
38	PG3	✓	✓
39	PN0	✓	✓
40	PN1	✓	✓

Table 2.142 Boundary-scan Order (2/4)

Order	Function name or port name	Support (✓: Supported, -: Not supported)	
		M4GR (177-pin product only)	M4GQ (145-pin product only)
41	PN2	✓	✓
42	PN3	✓	✓
43	PN4	✓	✓
44	PN5	✓	✓
45	PN6	✓	✓
46	PN7	✓	✓
47	PP0	✓	✓
48	PP1	✓	✓
49	PP2	✓	✓
50	PP3	✓	✓
51	PP4	✓	✓
52	PP5	✓	✓
53	PP6	✓	✓
54	PP7	✓	✓
55	PR0	✓	✓
56	PR1	✓	✓
57	PR2	✓	✓
58	PR3	✓	✓
59	PR4	✓	✓
60	PR5	✓	✓
61	PR6	✓	✓
62	PR7	✓	✓
63	PT0	✓	✓
64	PT1	✓	✓
65	PL7	✓	-
66	PL6	✓	-
67	PJ3	✓	-
68	PJ2	✓	-
69	PJ1	✓	-
70	PJ0	✓	-
71	PT2	✓	✓
72	PF0	✓	✓
73	PF1	✓	✓
74	PF2	✓	✓
75	PF3	✓	✓
76	PF4	✓	✓
77	PF5	✓	✓
78	PF6	✓	✓
79	PF7	✓	✓
80	PC7	✓	✓

Table 2.143 Boundary-scan Order (3/4)

Order	Function name or port name	Support (✓: Supported, -: Not supported)	
		M4GR (177-pin product only)	M4GQ (145-pin product only)
81	PC6	✓	✓
82	PC5	✓	✓
83	PC4	✓	✓
84	PC3	✓	✓
85	PC2	✓	✓
86	PC1	✓	✓
87	PC0	✓	✓
88	PB7	✓	✓
89	PB6	✓	✓
90	PB5	✓	✓
91	PB4	✓	✓
92	PB3	✓	✓
93	PB2	✓	✓
94	PB1	✓	✓
95	PB0	✓	✓
96	PA7	✓	✓
97	PA6	✓	✓
98	PA5	✓	✓
99	PA4	✓	✓
100	PA3	✓	✓
101	PA2	✓	✓
102	PA1	✓	✓
103	PA0	✓	✓
104	PY4	✓	✓
105	PT3	✓	✓
106	PU0	✓	-
107	PU1	✓	-
108	PU2	✓	-
109	PU3	✓	-
110	PU4	✓	-
111	PU5	✓	-
112	PU6	✓	-
113	PU7	✓	-
114	PY3	✓	✓
115	PY2	✓	✓
116	PY0	✓	✓
117	PY1	✓	✓
118	PD0	✓	✓
119	PD1	✓	✓
120	PD2	✓	✓

Table 2.144 Boundary-scan Order (4/4)

Order	Function name or port name	Support (✓: Supported, -: Not supported)	
		M4GR (177-pin product only)	M4GQ (145-pin product only)
121	PD3	✓	✓
122	PD4	✓	✓
123	PD5	✓	✓
124	PD6	✓	✓
125	PD7	✓	✓
126	PE0	✓	✓
127	PE1	✓	✓
128	PE2	✓	✓
129	PE3	✓	✓
130	PE4	✓	✓
131	PE5	✓	✓
132	PE6	✓	✓
133	PE7	✓	✓
134	PJ7	✓	-
135	PJ6	✓	-
136	PJ5	✓	-
137	PJ4	✓	-
138	PT5	✓	✓
139	PW3	✓	-
140	PW2	✓	-
141	PW1	✓	-
142	PW0	✓	-
143	PV7	✓	✓
144	PV6	✓	✓
145	PV5	✓	✓
146	PV4	✓	✓
147	PM7	✓	✓
148	PM6	✓	✓
149	PM5	✓	✓
150	PM4	✓	✓
-	TDO	✓	✓

2.31. Trimming Circuit (TRM)

2.31.1. Built-in List

The following table shows the built-in list for each product.

Table 2.145 TRM Built-in List

Product	Built-in TRM (✓: Available, -: N/A)
M4GR	✓
M4GQ	✓
M4GN	✓

2.31.2. Trimming Target Oscillator

The object oscillator of the TRM is an oscillator shown in the following table.

Table 2.146 Trimming Target Oscillator

Object oscillator	Oscillator name
Internal high-speed oscillator 1	IHOSC1

2.32. External Bus Interface (EBIF)

2.32.1. Built-in List

The following table shows the built-in list for each product.

Table 2.147 EBIF Built-in List

Product	Built-in EBIF (✓: Available, -: N/A)
M4GR	✓
M4GQ	✓
M4GN	✓

2.32.2. Function Pin and Port

The functional pin is assigned to the port of the following table.

Table 2.148 EBIF Function Pin and Port

Function pin			Port	Product table (✓: Available, -: N/A)		
Separated bus	Multiplexed bus			M4GR	M4GQ	M4GN
EA00 to EA07	-	Output	PA0 to PA7	✓	✓	✓
EA08 to EA15	-	Output	PB0 to PB7	✓	✓	✓
			PE7 to PE0	✓	✓	✓
EA16 to EA23	EA16 to EA23	Output	PC0 to PC7	✓	✓	-
			PE7 to PE0	✓	✓	✓
ED00 to ED15	EAD00 to EAD15	I/O	PD0 to PD7 and PE0 to PE7	✓	✓	✓
-	EALE	Output	PG0	✓	✓	✓
ERD_N		Output	PF0	✓	✓	✓
EWR_N		Output	PF1	✓	✓	✓
ECS0_N		Output	PK2	✓	✓	✓
ECS1_N		Output	PK3	✓	✓	✓
ECS2_N		Output	PF4	✓	✓	-
ECS3_N		Output	PF5	✓	✓	-
EBELL_N		Output	PF6	✓	✓	✓
EBELH_N		Output	PF7	✓	✓	✓
EWAIT_N		Input	PG1	✓	✓	✓
EEXBCLK		Output	PY4	✓	✓	✓

3. Revision History

Table 3.1 Revision History

Revision	Date	Description
1.0	2021-02-25	- First release
1.1	2023-09-15	- 2.10.2. System clock The section is added.
1.2	2024-05-31	- Preface Related Document IP symbols of the Flash memory and serial memory interface are changed.

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